PRESS RELEASE

LETI DEVELOPS 3D NETWORK-ON-CHIP TO IMPROVE HIGH-PERFORMANCE COMPUTING

Fabrication-ready Hardware-plus-software Communications Solution Boosts Performance, Reduces Energy Consumption

SAN FRANCISCO – July 12, 2016 – Leti, a CEA Tech institute, today announced it has developed a new on-chip communications system to improve high-performance computing (HPC) that is faster and more energy efficient than current solutions and is compatible with 3D architectures.

Leti researchers, working in the frame of IRT Nanoelec, boosted computing power and slashed energy consumption by stacking chips on top of each other in a single enclosure, or by placing the chips side by side on a silicon interposer. The chips, which have progressed from demonstrator to fabrication-ready, exchange data via a new communications network that is part of the network on chip (NoC) called 3D-NoC.

3D-NoC technology has been demonstrated with a homogeneous 3D circuit that is comprised of regular tiles assembled using a 4x4x2 NoC. It also features robust and fault-tolerant asynchronous 3D links, and provides 326 MFlit/s @ 0.66 pJ/bit. It was fabricated in a CMOS 65nm technology using 1,980 TSVs in a Face2Back configuration.

This second generation 3D-NoC technology has been integrated in the INTACT circuit developed in the frame of IRT Nanoelec. The 3D circuit, currently in foundry, combines a series of chiplets fabricated at the FDSOI 28nm node and co-integrated on a 65nm CMOS interposer. The active interposer embeds several lower-cost functions, such as communication through the NoC and system I/Os, power conversion, design for testability and integrated passive components.

Moreover, the chip requires 20 times less energy for data transmission than chips placed on an electronic circuit board. This new IP is compatible with standard remote direct-memory-access-type software used for data transmission and has likely industrial uses in virtual-server migration applications.

“The steady rise in the number of applications that require high-performance computing creates a demand for new hardware-plus-software communications solutions that improve both performance and energy consumption,” said Denis Dutoit, Leti strategic marketing manager. “This new technology brick makes it possible to transfer data between processors via a network-on-chip delivering more powerful, energy-efficient computing.”

Leti will host its annual workshop during Semicon West on “Sensing your Future with Leti” at 5 p.m., July 12, at the W Hotel. Registration is here.

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Leti scientists will be available at booth #2028 in the South Hall during Semicon West to discuss this announcement and other recent research developments and initiatives.

About Leti (France)

As one of three advanced-research institutes within the CEA Technological Research Division, CEA Tech-Leti serves as a bridge between basic research and production of micro- and nanotechnologies that improve the lives of people around the world. It is committed to creating innovation and transferring it to industry. Backed by its portfolio of 2,800 patents, Leti partners with large industrials, SMEs and startups to tailor advanced solutions that strengthen their competitive positions. It has launched 54 startups. Its 8,500m² of new-generation cleanroom space feature 200mm and 300mm wafer processing of micro and nano solutions for applications ranging from space to smart devices. With a staff of more than 1,800, Leti is based in Grenoble, France, and has offices in Silicon Valley, Calif., and Tokyo. Follow us at www.leti.fr and @CEA_Leti.

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