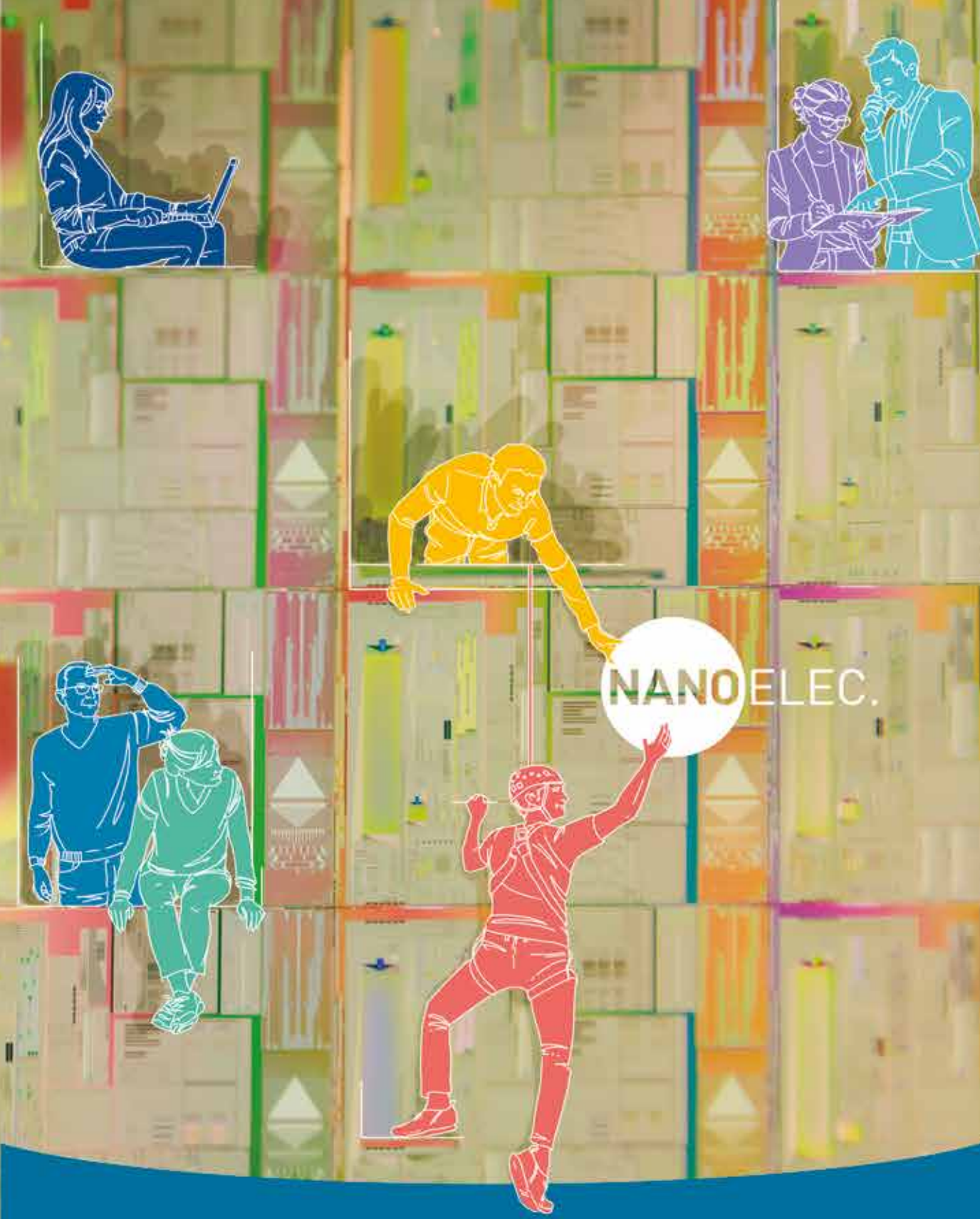
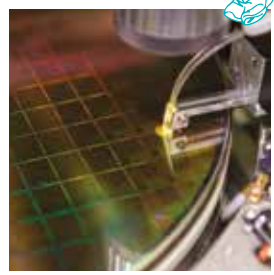
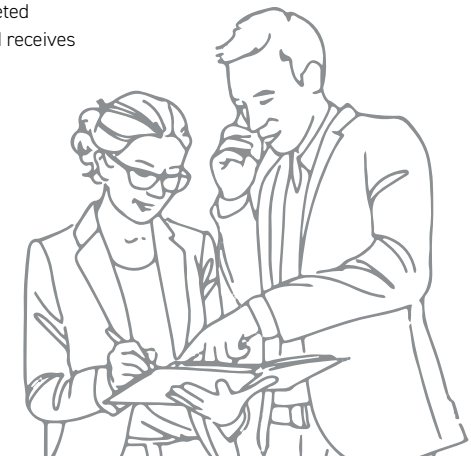


Scientific & Technical highlights

2023 EDITION





DIGITAL TRUST

PULSE

CHARAC-TERIZATION

TECHNOLOGY DISSEMINATION

HUMAN CAPITAL & TRAINING DESIGN

SUSTAINABLE DEVELOPMENT

Exploring the of electronics

IRT Nanoelec runs multi-partner programs to make the electronics industry more competitive and greener, and thus contribute to the sustainable development of society.

The Nanoelec technological research institute (IRT) is a consortium of private and public sector players, backed by CEA. Our mission is to help companies create value and enable their products to stand out on the digital transition stage.

Nanoelec contributes to the competitiveness of the electronics industry, particularly in France. Based in Grenoble, the institute is a world-class hub for research, innovation and production in its field.

Our R&D programs are built jointly by representatives from the academic and industrial worlds.

They deal with the design and development of new processes, systems and components in the following fields:
- photons & imaging: photonic sensors, new-generation displays and smart image sensors,
- digital trust: cybersecurity for connected objects, and characterization and irradiation of components and systems by means of large instruments.

Nanoelec also runs training design and technological dissemination programs for SMEs with the support of the Auvergne Rhone-Alpes region and local authorities. We implement open innovation techniques as well as more conventional technological development methods.

Given the pervasive nature of digital technologies, Nanoelec is in contact with actors from all sectors ranging from goods to services, industry, infrastructures, and consumer products, as well as transportation, environment and health.

Nanoelec is a member of FIT, a hub of technological research institutes (IRTs) and energy transition institutes (ITEs) set up by the French Government and financed by the Investments for the Future program (PIA). The network of institutes was created to pool academic and industrial players who could run collaborative R&D and innovation projects aimed at boosting the competitiveness of the French economy. •

future

"ANTICIPATING FUTURE HUMAN AND TECHNICAL NEEDS IN ELECTRONICS."

Anticipating future human and technological needs

MICROELECTRONICS INNOVATION

- → Carry out world-class collaborative R&D to enable innovative components and embedded systems: image & photons, and digital trust
- → Develop and transfer these technologies to enable the electronic circuits of the future
- → Give industry players access to development, prototyping and advanced characterization and education & training resources

TECHNOLOGY DISSEMINATION

- → Help businesses in the field of information and communication technologies meet the challenges of IoT through digital trust and security
- → Provide expertise to help SMEs from various industrial sectors build new products and services with innovative components and embedded software
- → Promote cooperation between SMEs, mid-caps and large companies
- → Focus on collaborative innovation to unveil new applications comprising environmental and social impact assessments

DEVELOPMENT OF HUMAN CAPITAL

- → Attract young people to jobs in electronics that contribute to sustainable development
- → Work with partners on parity and workplace equality
- → Design training courses to meet current needs
- → Anticipate future skill requirements in the sector: attractiveness for HR, sustainability, cross-skills, social and sustainable communities for innovation

"WORKING TOGETHER TO CARRY OUT RESPONSIBLE RESEARCH AND DEVELOPMENT PROGRAMS TO HELP BUSINESSES CREATE VALUE."

A consortium of **22** **PUBLIC & PRIVATE** members *as of Dec. 2022*

53 M€ *yearly average 2015-2022*

311 associated partners including **229** SMEs *since 2012*

619 scientific or technical publications & communications *since 2015*

235 patents & **53** software filed *since 2012*

223 full-time jobs *yearly average 2015-2022*

A new funding phase for the institute

BY HUGHES METRAS
Director of Technological Research Institute IRT Nanoelec

In 2022, Nanoelec celebrated its 10th anniversary. Our 22-partner consortium, made up of trusted, like-minded professionals, is contributing to the competitiveness of the microelectronics industry. The wide-ranging group of complementary players is currently focused on application oriented programs: smart image sensors new generations of microled displays; silicon photonic sensors; trust and digital security for embedded systems. We also carry out programs on educational engineering and technological dissemination.

As part of our institute's evaluation in 2022, the French National Research Agency (ANR) conducted an impact analysis, which revealed business value creation in all our technological programs, through either investments or the launch of new products. The evaluators took note of the strong commitment of all Nanoelec's partners since the institute was created; they confirmed our high level of excellence

This excellence prompted the government to confirm a new funding phase for the institute until 2025. I wish to commend program teams and directors for the quality of their research.

The following report includes many highlights pertaining to scientific production and to our partners' technological results. I will mention a few for the purpose of illustration: Nanoelec's research in post-quantum cryptography has gained significant international visibility as the result of our publications in the framework of the NIST (US) initiatives in the field; actively involved in our Displed program, Aledia is completing its production plant near Grenoble; and, as part of our Photonic Sensors program, startup Scintil Photonics has raised 15 million euros.

For the past 10 years[1], Nanoelec has conducted research projects with more than 300 partners, and has tackled technological challenges in multilateral collaborations, a distinctive approach compared with more common bilateral agreements between an R&D organization and an industrial entity.

Since 2020, we have strived to apply a sustainable development approach in our activities. Not only do we integrate eco-design and life cycle analyses in R&D phases, we also focus on initiatives that promote gender parity, and ensure the attractiveness of the microelectronics industry. Our 2022 contest, Women in Technological Research, helped to shed light on highly accomplished female scientists, as well as women who contribute to innovation in their daily work through other professions such as management, communication, and project management. Their commitment contributes significantly to employer attractiveness, which is vital to ensure a sustainable microelectronics industry.

—

↑
Hughes Metras, Director, and Sandrine Maubert, Deputy-Director of the institute, at the 2022 general assembly of Nanoelec and the celebration of its 10th anniversary.

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1. Particularly as a result of Minalogic's active involvement in the Easytech initiative.

CONTENTS

"THE ANR EVALUATORS TOOK NOTE OF THE STRONG COMMITMENT OF ALL NANOELEC'S PARTNERS SINCE 2012."

↗
Hughes Metras, Director of IRT Nanoelec
© P.Jayet/CEA

Grenoble joins the mega-fabs

"SOCIETY HAS BEGUN TO REALIZE THE CHALLENGES OF CLIMATE CHANGE AND ENERGY TRANSITION; THE SEMICONDUCTOR INDUSTRY IS ADAPTING."

↗
Sébastien Dauvé, Director of CEA-Leti and President of Nanoelec Steering Committee

© C. Tresca/CEA

BY SÉBASTIEN DAUVÉ,
President of Nanoelec
Steering Committee

The global market for electronic components currently tops 500 billion dollars[1]; it is expected to double by 2030. The Covid crisis has also demonstrated the essential role played by components in modern economies.

Hardware supports transitions

Electronic chips are a key enablers of the digital transition across all industry fields: growth is driven primarily by the acceleration of digitalization in consumer, healthcare and industrial sectors, the advent of artificial intelligence, and of course, the automotive industry.

Electronic chips are also vital for the energy transition and its related electrification requirements across the globe. As an illustration, we can mention the industrial transfer based on research conducted as part of the Nanoelec/PowerGaN program. STMicroelectronics has deployed a pilot line for the production of conversion components in Tours, France.

Significant events in the past three years

Despite its vitality, the electronics market is affected by major events, as is the rest of society. With regards to supply chains, companies have shifted from a 'just in time' to a 'just in case' strategy. In addition, automobile manufacturers have teamed up with leaders in digital technology.

Society has begun to realize the challenges of climate change and energy transition; the semiconductor industry is adapting[2]: frugal energy use, environmental and societal responsibility. Finally, geopolitical shifts prompt numerous questions regarding sovereignty. As far as we are concerned, how shall we maintain an industrial expertise and how will we succeed in relocatingproduction sites for electronic components.

A territorial ecosystem and a value chain approach

Two highly significant announcements will have a strong impact on our R&D and innovation activities within the Grenoble ecosystem and beyond. *The European Chip Act* provides a means for us to increase R&D collaborations at a European scale in order to reduce supply chain shortages and tensions, strengthen design and manufacturing capacities, and, in the long term, maintain our industry's competitive edge. The European-wide goal is to reach 20% of the global production of chips.

In France, as a result of the electronics-oriented agenda of the France 2030 plan, Crolles, in the Grenoble area will join the selective club of mega-fabs with a capacity of more than a million wafers per year[3].

Tenth anniversary

For the past 10 years, Nanoelec has successfully tackled some of the key challenges of the microelectronics industry by relying on the complementarity of stakeholders in its ecosystem, and on its value chain approach. Every year, more than 200 women and men — technicians, engineers, researchers and support personnel — are involved in Nanoelec programs with a focus on heterogeneous integration technologies and embedded systems. We are commited to provide them with bold and attractive projects!

—

1. In 2020, 1,000 billion microchips were manufactured across the globe; Europe produced merely 10%.

2. The Semiconductor Climate Consortium is focused on the challenges of climate change and works to speed industry value chain efforts to reduce greenhouse gas emissions in member company operations and in other sectors of our value chain. *https://www.semi.org/en/industry-groups/semiconductor-climate-consortium*

3. In July 12, 2022, the French government introduced a major plan to support the electronics industry. As part of the France 2030 investment plan, and endowed with 5 billion euros, the plan will enable the creation of 5,700 direct jobs. *https://www.entreprises.gouv.fr/fr/actualites/france-2030/france-2030-presentation-de-la-strategie-pour-l-electronique*

POWERGAN SYMPOSIUM

In March 2022, to conclude the Nanoelec/PowerGaN program, close to 200 experts from both industry and academia got together in Paris (in person and online) at a symposium organized with IRT Saint Exupéry and ITE Vedecom. Numerous industrial players from the power component application sectors were represented. STMicroelectronics presented its industrial and commercial roadmap for the coming years. •

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Highlights


© Pixabay

JANUARY 22

Sustainable electronics for smart buildings

An immersive two-day workshop for students from business and engineering schools, and industrial experts, organized by the Nanoelec/Human Capital & Training Design program. →

FEBRUARY 22

Equality & parity

Nanoelec became member of two associations: Parity for Science in Grenoble and Women Engineers.

Artificial intelligence

February 12 | Cross-program workshop on artificial intelligence, with the participation of Minalogic competitiveness cluster and IRT SystemX.

MARCH 22

Women in Engineering

March 8 | Nanoelec launched the "2022 Nanoelec award for women in technological research" to mark the institute's 10th anniversary. As part of International Women's Day, Nanoelec conducted a public webinar: "Jobs in Engineering" with association Women Engineers. ↓

Education & training

March 10 | Webinar that provided an overview of the Nanoelec partner Captronic's training offer.

Design and architecture

March 13 | At the international DATE conference, Nanoelec broadcasted an online one-day event including a plenary keynote, guest speakers, and regular presentations from CEA, Qualcomm, Georgia Tech, Stanford University, ETHZ (Switzerland), Fraunhofer Institute, University of Seville, Prophesee, STMicroelectronics, NTU (Singapore), Boston University, University of Manchester, Stony Brook University, Notre Dame University, META Group (Facebook), Siemens EDA, Intel. ↓

PowerGan

March 15 | National symposium for the conclusion of Nanoelec/PowerGaN, which focuses on electrical power conversion with GaN Material, by Nanoelec, ITE Vedecom & IRT Saint Exupéry.


© P.Jayet/CEA

APRIL 22

System Lab for smart building

April 5 | At the Campus Numérique in Lyon, session for SMEs, ETIs and innovative startups in the Auvergne Rhône-Alpes region: presentation of System Lab, an open platform for exploring new scenarios for using multispectral optical sensors.

April 28 | Regional workshop System Lab in Gardanne (Bouches du Rhône) with Captronic.

MAY 2022

Open hardware

May 3 | Annual Risc-V week in Paris, with Nanoelec.

Effects of radiation

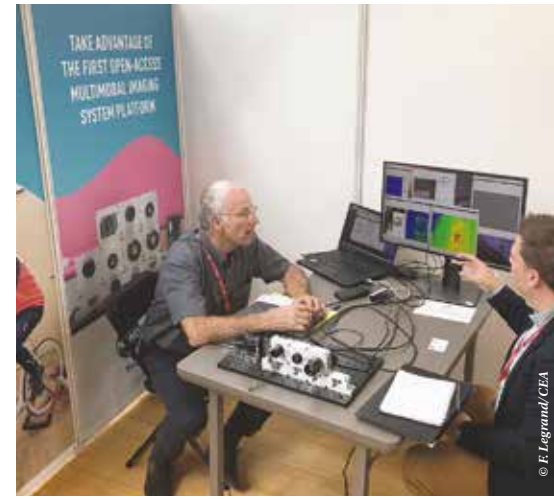
May 4 | Grad[Next], a workshop on radiation facilities and testing of semiconductor devices & industry systems, was organized by Nanoelec, Cern, ILL, ESRF, Iroc Technology, CNRS/LPSC, Radsag & Radecs.

France strives to improve next generations of displays

May 6 | The Nanoelec/Displed program was presented in a public conference by CEA and Aledia experts.

May 17 | System Lab booth at Global Industrie (Paris) with Captronic.

May 31 | Nanoelec/Technological Diffusion: System Lab + Easytech presented on a booth at Minalogic Business Meeting (Grenoble).



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JUNE 22

System Lab

June 2 | System Lab presented at the regional technological transfer platform in Bordeaux.

Responsibility & social impact

June 9 | Business webinar: CEA Community on the Societal Impact of Technologies by Michel Ida (CEA).

Gender quest

June 16 | Webinar open to all: La science taille XX elles, with association Parity in Science.

Leti Innovation Days

June 21-23 | Forum Area event: Leti Innovation Days in Grenoble with more than 25 mini-conferences for companies.

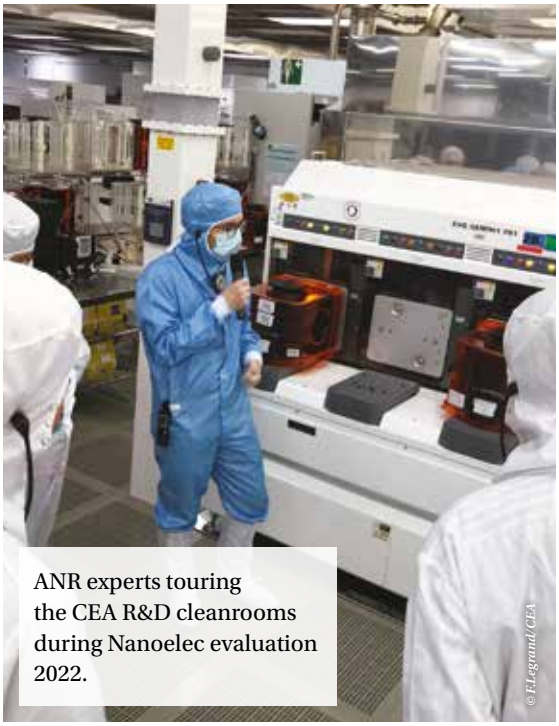
June 23 | Nanoelec contest Women in Technological Research: nominee presentations before the jury panel and the public. Organized in the frame of the International Days for Women in Engineering.

© Vincent Moncorgé Photothèque CNRS Association Femmes & Sciences

JULY 22

Parity in science

"Science taille XX Elles" exhibition presented by Nanoelec at CEA-Leti.



ANR experts touring the CEA R&D cleanrooms during Nanoelec evaluation 2022.

AUGUST

Outdoor photo & video campaign →

for Nanoelec awards for women in technological research.


© F. Legrand/CEA

Green Electronics

August 28 | Nanoelec: partner of SICT Doctoral School on Sustainable Electronics, with UGA.

↓


© F. Legrand/CEA

System Lab

September 6 & 9 | System Lab presented at the Colloque Francophone de Traitement du Signal et des Images @ Nancy.

September 6 & 7 | System Lab at their stand & demonstration at Mems & Imaging Sensors Summit @ Grenoble.

↓

SEPTEMBER

EU Digitalization →

September 12-13 | Horizon Europe EARASHI (Embodied AI/ Robotics Applications for a Safe, Human-oriented Industry): project launch with Nanoelec/Pulse.

© DR

September 14 & 15 | System Lab on a booth presented at Sido Lyon.

↓

Industry attractiveness

September 23 | Webinar open to all: "Talking about your job with youngsters" with association Women Engineers.

↓

OCTOBER

World Electronics Forum

October 5 | Nanoelec partnered with international annual forum: World Electronics Forum (Grenoble).

National Science Fest Campain

October 8 | Conference open to the public on Blockchain & Digital Identification (Grenoble).

Embedded AI

October 18 | Business seminar: Embedded AI with Captronic, CEA and Mines St Etienne (Gardanne).

Digitizing SMEs in EU

October 24 | Final workshop of DigiFed European project, with Nanoelec.

NOVEMBER

Digitizing SMEs in EU

November 6-9 | Nanoelec participated in annual international summit High Level Forum (Finland).

November 9 | Nanoelec partnered with CSAW'22.

November 22 | Annual Nanoelec/Carac colloquium.

System Lab

November 22 | Conference and demonstration given at SEPEM @ Grenoble, November 2022.

DECEMBER 22

Innovation Forum

December 8 | Webinar open to the public and the press: preview of the 2022 iForum, with La Metro (Grenoble-region community), CCI etc.

General Assembly

December 13 | General assembly and the 10th anniversary of Nanoelec.

System Lab

December 8&9 | Stand and demonstration in SIDO Paris.

JANUARY 23

Sustainable Electronics

January 27 | Nanoelec/ Human Capital & Training Design program conducted a seminar: Technology usages: how does sustainable development influence decision making? With contributions from Schneider Electric, Grenoble-Ecole de management, Grenoble INP-UGA and CEA.

FEBRUARY 23

Photonics West

February 2 | Presentation of III-V material integration on Si photonics platforms through direct bounding (wafer-to-wafer & die-to-wafer). As part of a Nanoelec initiative, the process is available for 200- and 300mm wafers. It is CMOS compatible and ready for large-scale integration.

Industry Attractiveness

Two webinars on the attractiveness of the microelectronics industry: “Ninth-grade internships: How to spark interest in technology jobs” & “A learning kit for jobs in smart electronics”.

MARCH 23

Industry attractiveness

March 2 | Forty representatives from Nanoelec core partners gathered for an initial collective discussion on commitment, education and recruitment.

International Women's Day

March 7 | In association with Y.Spot and CEA, Nanoelec conducted a round table: How to attract innovative female talent? Participants included high-ranking female managers from CEA, GEM, HP France, Lynred, UGA & Nanoelec.

Photonic Sensors

March 8 | CEA-Leti & Nanoelec booth at international Optical Fiber Communication conference (OFC), USA.

Women in Engineering

March 27 | Nanoelec exhibition Women in Technological Research presented at the Laue-Langevin Institute.

APRIL 23

Nanoelec ambassadors

April 18 | Nanoelec exhibition Women in Technological Research presented at the La Casemate, the center for scientific culture in Grenoble, as part of the 50 Audacieuses event.

3D integration: design & architecture

April 19 | Annual Nanoelec workshop at the DATE international conference.

System Lab

April 26 | Imagers, sports and health colloquium at CEA/Y.Spot (Grenoble).

MAY 23

Industry attractiveness

May 11 | Local forum on the attractiveness of the microelectronics industry organized by Minalogic and Nanoelec. 150 attendees.

Women in Engineering

May 30 | Portraits of Nanoelec female ambassadors by students from Pablo Picasso Middle School (Echirolles) were presented at La Casemate, the center for scientific culture in Grenoble.

FROM 3D INTEGRATION TO IMAGES

Progress in the semiconductor industry is divided into two classes: Moore's Law, where chips are manufactured with advanced technologies of 16 nanometers and smaller (this is the case for the processors at the heart of smartphones, tablets, PCs, and servers), and the More than Moore's approach, which uses mature manufacturing technologies of 20 nanometers and larger (this is the case for most components such as microcontrollers, power management circuits, sensors, power electronics, and radio-frequency circuits).

As the microelectronics industry continues to face challenges to further miniaturize components, according to Moore's Law, the More than Moore approach is also becoming more widespread. At Nanoelec in particular, we are building on 10 years of R&D on three-dimensional architectures, which now enable us to address very ambitious applications prospects.

3D integration, which consists in interconnecting electronic chips in 3 dimensions, is a promising solution for addressing the growing need for functionality, density and performance in future integrated circuits. However, to allow the rapid emergence of this technology in industry, an overall approach is needed, taking account of technological development and the design of new circuit architectures, the development of design and testing tools as well as reliability.

From 2012 to 2020, the academic and industrial teams working under the Nanoelec/3D Integration program focused on developing a comprehensive platform compatible with the full design cycle of new products. They dealt with technology for hybrid bonding wafer-to-wafer or die-to-wafer, but also design, electronic design automation (EDA) tools, testing and reliability.

In her talk at the Semi 3D & system Summit, Sylvie Joly[1], Partnerships Manager for 3D integration & packaging at the Silicon Components Division of CEA-Leti and attached to Nanoelec, stated five challenges in hybrid bonding. *"Supply chain integration, interconnection alignment, inter-die spacing reduction, efficient electrical connections, processing throughput are the challenges we are seriously working on",* she comments.
These challenges are all addressed through the partners of the Nanoelec programs focusing on applications: one devoted to image display technologies (Displed) and the other to sensing (Smart Imager).

1. **Joly S.** Hybrid Bonding from Hype to Reality: How Will Hybrid Bonding DTW Pave the Way to Large Set of Applications? *3D & system Summit 2022.*

SMART IMAGER

↗
Eric Ollier, Optical Project Manager at CEA-Leti and Director of Nanoelec/ Smart Imagers program

© P.Jayet/CEA

From imaging to visioning

Mastering smart imagers industrial process flow would be a competitive advantage for Nanoelec's industrial partners.

© pixabay

SMART IMAGER PROGRAM AT A GLANCE

→ Vision

The transition from imagers to vision sensors is generating new market opportunities

→ Ambition

To provide key HW and SW building blocks, to validate them through demonstrations ranging from test vehicles and proofs of concept to the prototyping of a smart, multi-layer imager

→ Mission

Stacking/3D technologies, embedded AI and data management, New architectures

→ Partners

CEA, Lynred, Prophesee, Siemens EDA, STMicroelectronics, Grenoble INP-UGA

The Nanoelec/Smart Imager program is committed to providing relevant and real-time environment analysis by vision. It could be the greatest technical challenge at Nanoelec for the coming years.

The aim of IRT Nanoelec's Smart Imager program is to develop the technologies needed for the next generation of imagers, which will allow the transition from image generation to the analysis of the information included in these images, on the very sensor itself, in order to perceive a scene, understand the situation and intervene on it. This transition represents a very real disruption and a paradigm shift, with the computing and memory issues becoming preponderant, in addition to image generation. This revolution implies the use of artificial intelligence on the image sensor itself.

The consortium's goal is to develop 3D stacking technologies in order to implement artificial intelligence functions on the sensor itself. This is why we are working both on the components and on the software, to transition our image sensor concepts from image generation to data generation, enabling a situation to be analyzed.

Our program is very close to two other activities at Nanoelec: the System Lab initiative, on the search for new multi-spectrum imaging applications, and Displed, -new generations of displays- on the simulation & design tools for hybrid bonding components and technologies for 3D architectures.

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Technology, architecture & applications

Transforming digital vision with cutting-edge 3D-stack camera sensors, global shutter and iToF

↑
STMicroelectronics recently launched the VD55H1, a low-noise, low-power indirect time-of-flight (iToF) sensor array of 672 x 804 pixels (0.54 Mpixels). *© STMicroelectronics*

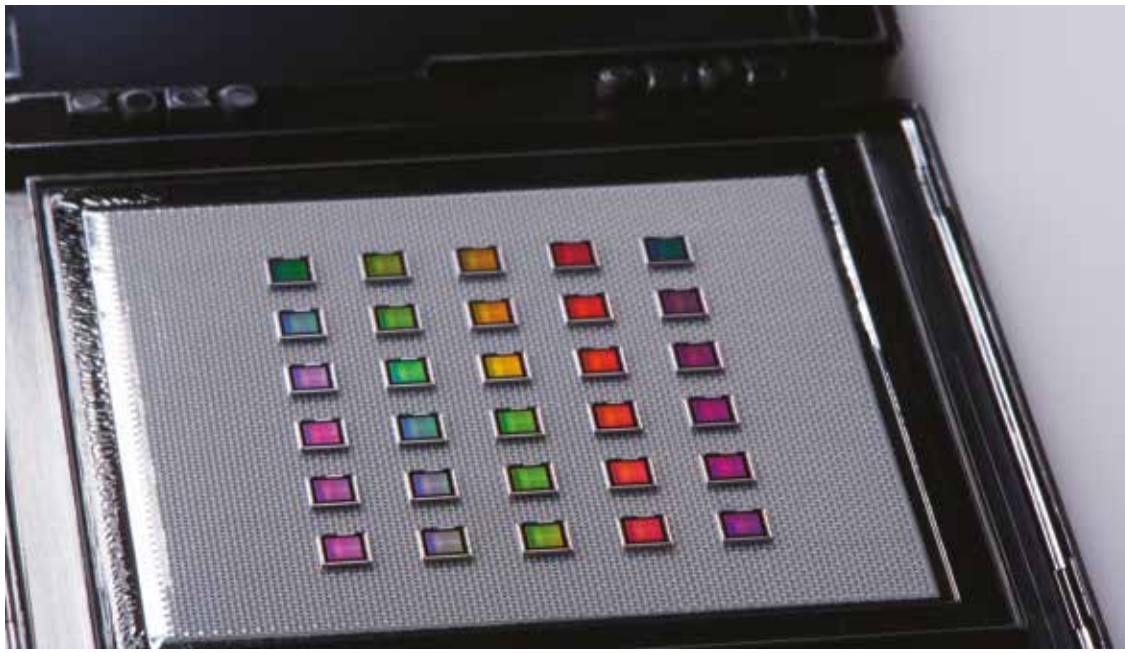
STMicroelectronics is developing a whole range of new image sensors with unprecedented performance thanks to the 3D integration developed within Nanoelec.

3D architecture technologies are industrialized by STMicroelectronics in its four major imager application markets: automotive, industry, personal electronics and computers & peripherals. The international group is now proposing a full range of products based on these technologies developed within Nanoelec.

"The work done within Nanoelec continues to support ST Crolles' technology roadmaps and to contribute to exploring future product architectures for the Imaging Division. 3D-stacking technology is now offered in foundry mode for selected partners", underlines Nicolas Roux, Product Line Manager at STMicroelectronics for Imaging Camera sensors.

STMicroelectronics provides Global Shutter type image sensors based on BSI (backside illumination technology) using 3D building blocks developed after several years within Nanoelec, including the Harmony demonstrator in 2018. "*And very recently, teams involved in Nanoelec succeeded in demonstrating the possibility of combining fine pitch Cu-Cu hybrid bonding technology with high density (HD) TSV"*, says Eric Mazaleyrat, Technology Scouting and Innovation Director at STMicroelectronics. *"The device is made with three different stacked structures, built on 300mm wafers, and has very good characterization performance. Thus, STMicrolectronics is both developing products and looking forward to upcoming results from Nanoelec to keep its competitive edge in commercial competition in the field of smart imaging."*

The group recently launched the VD55H1, a low-noise, low-power



↑
STMicroelectronics sensors VD55G0 and VD56G3 benefited from Nanoelec technologies to serve multiple applications in the field of low-power computer vision. © *STMicroelectronics*

indirect time-of-flight (iToF) sensor array of 672 x 804 pixels (0.54 Mpixels). *"This imager is manufactured using advanced backside illuminated stacked slice technology, based precisely on developments made within Nanoelec. The VD55H1 comprises an image sensor "bonded" onto a 40nm CMOS circuit"*, says David Maucotel, Business Line manager. *"In 2022, this product was evaluated by several customers who have started integration into their own platform. By comparison with comparable devices on the market, we offer moderate energy consumption, a low noise level and reduced chip size. The VD55H1 currently offers the best cost/resolution compromise on the market with a pixel size of 4.6µm."*

These time-of-flight (iToF) sensors provide smartphones and consumer electronic devices with advanced 3D vision and depth measurement capability, to build a 3-dimensional map of a scene, or human face, with a resolution of more than half a million points. Indirect Time-of-Flight measures the distance of each point from the sensor, from close distance up to five meters.

"BIOMETRY AND SECURITY THROUGH FACE RECOGNITION BECOME MORE ROBUST THANKS TO THE HIGH RESOLUTION AND GREAT ACCURACY OF 3D IMAGES CAPTURED BY VD55H1…"

They are suitable for both augmented reality and virtual reality applications, such as room scanning, video games gesture and depth/color image fusion, or 3D avatar captures. They can also improve photographic performance in most recent smartphones: the "Bokeh" effect (portrait mode, background blurring), automatic selection of the camera and video segmentation, and faster picture shooting in low light (Laser Autofocus). Biometry and security through face recognition become more robust thanks to the high resolution and great accuracy of 3D images captured by VD55H1, which improve the user experience in various applications such as phone face unlock, phone payment, access control in general, and high-resolution scene capture for robotics and industrial vision.

ST and Nanoelec 3D-stack technology are also suited to the recent image-sensor portfolio, with leading-edge pixel array (top die), while keeping more silicon area on the bottom die to increase digital-processing capabilities and features. Pixel resolution can be increased, with high sensitivity and low crosstalk.

Two new sensors VD55G0 (640 x 600 pixels) and VD56G3 (1.5 Mpixels) have benefited from these combined technologies and can now serve multiple applications in the field of low-power computer vision, AR/VR headsets, or face authentication. •

Technology, architecture & applications

The physical limits of resolution

↑
During his presentation at the Nanoelec General Assembly in December 2022, Xavier Brenière, head of the applications laboratory at Lynred illustrates the link between the two Nanoelec programs: Smart Imager and System Lab.

© Cédrine Tresca/CEA

Integrating signal processing into the sensor itself will give access to improved image quality and lower electrical consumption.

XAVIER BRENIÈRE, head of the application laboratory at Lynred, tells all.

Your primary motivation in Nanoelec is to improve resolution and on larger formats. Why is this a paradox?

The advanced technologies to which we have access under the Nanoelec/Smart Imager program are enabling the size of pixels in a camera to be gradually reduced, both in visible and infrared. But paradoxically, when the pixel pitch reaches the wavelength to be captured, the physics changes, with diffraction taking precedence over absorption, so there is not necessarily a direct gain in resolution.

Visible imagers are therefore reaching this limit, is this also the case of infrared imagers?

In the visible spectrum, we are nearing pixel pitches of almost 0.5 microns, for wavelengths of between 0.4 and 0.8 microns. Similarly, with bolometers, Lynred is achieving pitches of 8.5 microns for a detected wavelength range of 8 to 14 microns.

Could one hope to improve resolution further simply by reducing the pixel pitch?

Not directly, but this raises interesting questions of physics: by further reducing the pitch, could one take advantage of this pixel over-sampling, the plasmonic function or more advanced functions. This is a very interesting field of research for both the visible spectrum and infrared.

3D stacking will enable signal processing to be integrated into the sensor itself, to improve image quality, facilitate its interpretation or object recognition, while reducing the system's overall electrical consumption.

The work done in 2022 under the Nanoelec/Smart Imager program enabled you to consolidate several technical points and envisage future socio-economic benefits. What are they?

From the technology viewpoint, we have completed the definition of a 3D technological stack compatible with our two product families: cooled diodes and bolometers, which have totally different structures. We have defined the stacking sequence and checked the strength of hybrid bonding, in particular for cooling cycles at cryogenic temperatures.

Progress has also been made in exploring options for the final architecture including the processing of pixel signals, memory and algorithmic image processing.

Lynred is involved in two Nanoelec programs. What are you hoping for?

With Smart Imager, we are addressing major technological challenges. Nanoelec enables us to invest for the medium/long term: we envisage that 3D stacking technology and the associated architectures will appear in our products by the 2030 timeframe. In addition, the System Lab initiative enables us to continue the process with research opening up new applications possibilities, to which these technological advances are opening the door. •

Technology, architecture & applications

Dynamic response and frugality of event-based image sensors

Based in Paris and Grenoble, Prophesee is developing event-based sensors.

JEAN-LUC JAFFARD, Senior Advisor for innovation at Prophesee, explains what his company is looking for in the Nanoelec/Smart Imager program.

The traditional approach to imaging consists in taking a series of images, right?

This is done full frame and at high frequency: the sensation of movement is thus recreated. There are two main drawbacks in this method. Firstly, it generates a large amount of data to be processed and it consumes energy. Moreover, it is impossible to know what is happening between two image acquisitions.

How is the Prophesee imaging approach truly disruptive?

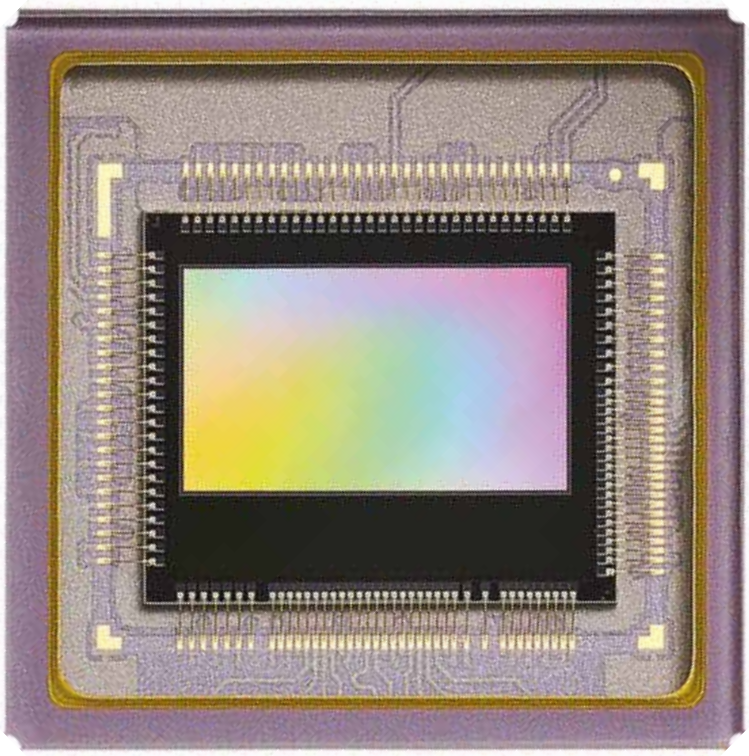
Our approach is more audacious but far harder to implement: we are developing sensors which only react when there is a change in contrast: if nothing happens, they generate nothing. Only those pixels which perceived a change are lit: if a spot of light reaches a single pixel, this pixel will be capable to detecting it at high speeds corresponding to several million events per second.

Why is this hard to do?

When you try to make sensors which only detect changes, you need "smart" pixels. In a traditional sensor, there are 3, 4 or 5 components per pixel, whereas in an event-based sensor, we have 80 to 100 components per pixel.

So how do you reduce the size of the event-based pixels and integrate them at the heart of these necessary components?

The challenge is to maximize the information processing inside the pixel. To be able to manufacture small pixels (to increase image resolution) and directly integrate the smart data functions, 3D integration is the path we are exploring within the Nanoelec/Smart Imager program. •



↗ **Prophesee event-based sensor.** © *Prophesee*

Test chips & performance assessment

First demonstration of 2-layers test vehicle

For the Smart Imager program, a CEA-Leti team demonstrates wafer level Face-To-Back (F2B) 3D integration combining fine pitch Cu-Cu hybrid bonding with high density TSV.

CMOS Imagers have adopted 3D integration with Back-Side Illumination (BSI) technology, with two layers stacked using wafer-to-wafer hybrid bonding technologies. The industry implements such technology for current CMOS imager sensors for various applications including the consumer market, allowing form factor reduction, pixel resolution increase, high performances and low energy consumption. This technology enables the assembly of optimized CMOS image pixel technology onto a CMOS layer dedicated to imager logic acquisition and data processing.

In April 2022, at the VLSI-TSA International Symposium in Taiwan, a team from CEA, working within Nanoelec, presented new 3D design and technology solutions developed in order to build a 3-layers Smart Imager[2]. *"We demonstrated our expertise in 3D technologies capable to enable manufacturing of 3-layers smart imagers: hybrid bonding technology for the assembly of multi wafers with sub-micron pitch capability and also High Density Through Silicon Via (TSV) with diameters less than 1 micron"*, says Stéphane Nicolas, project leader in the field of 3D heterogeneous integration at CEA-Leti, one of the authors of the study. In addition, the team proposed a Place & Route methodology with the associated PDKIT to take advantage of 3D fine pitch interconnects. The methodology refers to Design Technology Co-Optimization (DTCO) capabilities. This activity is key to develop new methodologies and design tools enabling innovative 3D stacked architectures, in order to offer AI processing at the edge within the image sensor itself targeting innovative AI and Machine Learning applications.

At the ECTC 2023 Conference, the same team presented the test vehicle demonstrated in 2022. *"We have successfully fabricated a 2-Layers Face-To-Back (F2B) test vehicle (TV) by combining fine pitch Cu-Cu hybrid bonding technology with high density (HD) TSV"*, says Stéphane Nicolas. Morphological characterizations carried out recently highlighted the integrity of the 3D structure. Furthermore, the results of electrical tests on Kelvin and Daisy-Chain structures demonstrated the electrical continuity between all the layers. These results validates the technological integration flow and the compatibility of HD-TSV with fine pitch hybrid bonding. This key building block that is mandatory to demonstrate the feasibility of 3-layers imagers. •

1. Vivet P., Arnaud L., Borel S., Bresson N., Assous M., Nicolas S., Mauguen G., Moreau S., Altieri M., Billoint O., Thuriès S. & Ollier E. Advanced 3D Design and Technologies for 3-Layer Smart Imager. *2022 International Symposium on VLSI Technology, Systems and Applications (VLSI-TSA), 1-2. https://doi.org/10.1109/VLSI-TSA54299.2022.9771026*

2. S.Borel, S. M. Assous, M., Moreau, S., Vélard, R. Recent Progress in the Development of High-Density TSV for 3-Layers CMOS Image Sensors & Suarez-BErru, J-J. Nicolas, S., Bresson, N., Assous, M., Borel, S. Demonstration of a Wafer Level Face-To-Back (F2B) Fine Pitch Cu-Cu Hybrid Bonding with High Density TSV for 3D Integration Applications : two conferences presented at IEEE 73rd Electronic Components and Technology *Conference, Orlando, Florida, May 30 - June 2, 2023*

↑
Cross-sectional SEM micrographs of HD TSV in a dense environment.
© CEA

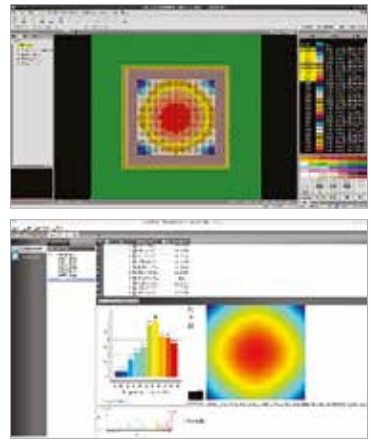
↑
Javier Suarez presenting "Demonstration of a Wafer Level Face-To-Back (F2B) Fine Pitch Cu-Cu Hybrid Bonding with High Density TSV for 3D Integration Applications" at IEEE ECTC Conference 2023.
© Joly/CEA

Design & design tools

Optimizing the architecture of the future 3-layer sensor

About electronic design automation (EDA), through participation in Nanoelec's Smart Imager program, Siemens EDA[3] contributes to establish reference flows for the design and verification of the integrated circuits that will be created by the IRT partners.

The participation of Siemens EDA in Nanoelec *"enabled us to obtain state-of-the-art circuits to validate the design and verification flows used with its tools and enjoy strong interaction with the CEA design teams"*, says Jean-Marc Talbot, Senior Solution & Strategic Partnerships Director at Siemens EDA. The market for CMOS imagers is growing rapidly and Siemens has had major customers in this sector for many years. The work carried out in Nanolec as part of industrial R&D is demonstrating the performance and efficiency of Siemens' commercial tools for this type of integrated circuit, and contributing to the development and testing of new tools by taking advantage of the CEA's R&D environment and measurement capabilities to ensure that simulation and experimental results match. *"We are also incorporating feedback from the community to continuously improve the performance of our design tools when used on the most advanced demonstrators and platforms"*, adds Jean-Marc Talbot.



↑
Results of the thermal analysis with the Sahara tool of an architecture for the future 3-layer imager developed under Nanoelec/Smart Imager.

© Siemens EDA

Regarding the future 3-layer imagers, Siemens EDA implements a number of flows and tools, including its Symphony mixed digital-analogue verification platform for verifying multilayer imagers, its Catapult high-level synthesis tool in conjunction with the CEA's N2D2 tool to automatically generate the RTL of the imager's IA layer, and the simulation of the power consumption of digital and analogue circuits using the mPower tool, 3D placement-routing using the Aprisa tool, etc. New tools to take account of electromigration phenomena and chip-package interactions are also being developed and tested.

The thermal effects associated with the operation of the future 3-layer imager and its package are also studied. *"The project Sahara software prototype processes the simulated heat dissipation and hot spots on a die and its package"*, explains Lee Wang, head of development of SAHARA prototype, which will become a product in 2023. Lee Wang also took part in the Nanoelec Awards 2022 "for women in technology research".

Sahara is an example of a long-term collaboration with the CEA that has enabled Nanoelec to move from prototype software to a product. There will be others in Nanoelec phase 3.
"This study enabled us to create the methodology and acquire the know-how to perform a thermal analysis of a complete 3D device, including the integrated circuits and their package, with the Siemens Sahara tool", adds Lee Wang. The thermal analysis proposed methodology enables to analyze the impact particular with the addition of the third imager layer, and iterate on the parameters of the thermal model, such as technology parameters, package, power budget, and circuit architecture, as often as necessary to optimize the architecture of the sensor before it is manufactured. •

3. The Siemens Electronic Design Automation SARL - Siemens EDA company, the world leader in design, verification and manufacturing-aid tools for integrated circuits, packages and PCBs, is one of the founding members of IRT Nanoelec.

Design & design tools

Heterogeneous Packaging Design and Verification Workflows

"Chiplet architecture is an answer to semiconductor scaling challenges", says Anthony Mastroianni, Advanced Packaging Solutions Director, Siemens EDA in a keynote speech at the DATE'22 Conference[4].

"Cost and yield are driving alternatives to monolithic solutions; it provides low latency at high bandwidth for data movement; In addition, fabrication flow by heterogeneous integration provides a path forwards."

Showing the heterogeneous integration product design process, he presented strategies for System Technology Co-Optimization (STCO) and 3D IC Test tools & methodology. •

4. Mastroianni, A. *2022, March 18* Heterogeneous Packaging Design & Verification Workflows. DATE'22. https://date22.date-conference.com/workshop/w02

Lee Wang, in charge of developing the Project SAHARA software prototype which will become a product in 2023. Lee Wang also took part in the Nanoelec Award 2022 "for women in technology research".

Design & design tools

Building a worldwide overview of 3D integration

The yearly international workshop on 3D integration at the DATE conference attracted 50 experts.

3D technologies are becoming more and more pervasive in digital architectures, as a strong enabler for heterogeneous integration. Considering the large amount of data required and the associated memory capacity, Machine Learning and AI accelerators could benefit from 3D integration not only for High Performance Computing (HPC), but also for edge and embedded AI within image sensors. *"3D integration and associated architectures are opening up a broad spectrum of system solutions, from chiplet-based partitioning for High Performance Computing to various sensors such as fully integrated image sensors embedding AI features, but also with the close 3D coupling of computing & memory enabling an efficient In-Memory-Computing paradigm"*, says Pascal Vivet, Scientific Director at CEA-List and Deputy Director of the Nanoelec/Smart Imager Program who every year organizes a dedicated workshop at the Date conference[5]. Date is the annual reference event for electronic system design automation & testing in Europe.

"In 2022, our 3D Integration workshop attracted 50 experts from both academia and industry, interested in this exciting and rapidly evolving field, in order to update each other on the latest state-of-the-art, exchange ideas, and discuss future challenges. We discussed Heterogeneous 3D Architectures and Sensors", says Pascal Vivet.

↑
Pascal Vivet (CEA-List), Deputy Director of the Nanoelec/Smart Imager Program organizes a dedicated workshop at the DATE conference every year.

© P.Jayet/CEA

The workshop was co-sponsored by Nanoelec. Keynote and invited speeches were provided by experts from CEA, Qualcom, Georgia Tech, Stanford University, ETH-Zurich (Switzerland), Fraunhofer Institute, University of Seville, Prophesee, STMicroelectronics, NTU (Singapore), Boston Univ., Univ. of Manchester, Notre Dame Univ, META Group (Facebook), Siemens EDA, Intel. •

"THE CLOSE 3D COUPLING OF COMPUTING & MEMORY ENABLING AN EFFICIENT IN-MEMORY-COMPUTING PARADIGM"

5. "3D Integration: Heterogeneous 3D Architectures and Sensors" *Workshop at DATE'22 conference* https://date22.date-conference.com/workshop/w02

Silicon Technology

Towards reliable hybrid bonds for 3D stacked IC

Direct hybrid bonding is the solution of interest for advanced 3D stacked Integrated Circuits (IC) with very short interconnect pitches.

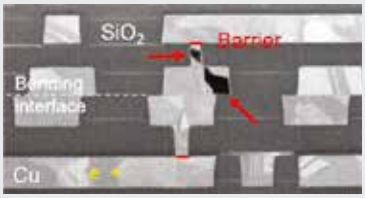
3D integration technologies emerged less than 10 years ago as viable solutions for meeting IC requirements such as higher performance, increased functionality, lower power consumption, and a smaller footprint. Some examples of 3D integration in products are CMOS Image Sensors (CIS), memories and interposers.

"Presently, to ensure vertical electrical connections, Through-Silicon-Vias (TSV) are integrated into most of these products, because they allow die-level assembly, and simplify some aspects of testing and packaging, but the main drawback of TSV is the Keep Out Zone (KOZ) combined with a Cu pillar pitch typically limited to 20-40µm", explains Stéphane Moreau, Research-Engineer in Reliability of 3D integration at CEA-Leti. *"For some applications, such as CMOS image sensors and memories, smaller pitches (< 10µm) are required for the vertical die-to-die connections; so direct hybrid bonding technology is the solution. While hybrid bonding based products are already on the market, few studies are being published with data about robustness/reliability"*, says Stéphane Moreau who reviewed reliability threats for hybrid bonding-based interconnects at the VLSI22 Symposium[6].

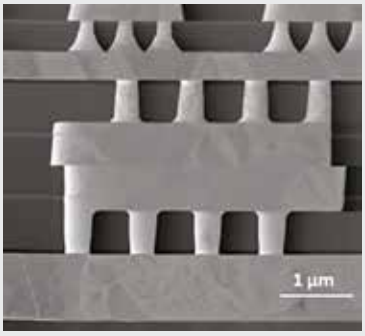
The potential threats identified by the scientific community are moisture ingress, thermomechanical stresses, electromigration, Cu diffusion, dielectric breakdown. In particular, two topics have been studied in depth: electromigration (times-to-failure, failure analyses, acceleration model) and copper diffusion (electrical and analytical characterizations). In the light of the scientific community results, even if the hybrid bonding-based interconnect is a new way to interconnect two tiers, its behavior against common reliability threats are very similar to that of the BEoL.

Given the published works, even if hybdrid bonding module could raise specific reliability issues, all the lights are green for mass production with micrometric pitches, which is consistent with the fact that this technology is already implemented in some products. On the contrary, for sub-micrometric pitches some questions remain topical: dielectric reliability including Cu diffusion, electromigration. In addition, robustness/reliability of heterogeneous stacking (different materials or dies) must be investigated in depth. Engineers and researchers are still working on these topics to find tricks to solve the potential reliability issues. •

6. Moreau S. *2022, June 12* Reliability Threats of Hybrid Bonding-Based Interconnects: Toward Mass-Production. *VLSI22 : 2022 IEEE Symposium on VLSI Technology and Circuits (VLSI Technology and Circuits), USA.*



↑ **Electronic imaging of hybrid bonding failed structure (void in Cu material) after an accelerated electromigration test: (presented at IRPS 2023 Conference)**



↑ **Electronic imaging of Hybrid bonding structure without defect.**

Silicon Technology

Characterizing connectors

Quality of the Cu pad connectors is an issue for a 3D stack IC.

In the Nanoelec/Smart Imager program, Cu pads as small as 300nm are used with hybrid bonding technology to reach extremely high interconnect density between 3D electronic chips. Successful bonding relies directly on the thermomechanical displacement of Cu above the oxide matrix. *"Hence, the control of this technology relies on a profound understanding of the thermomechanical behavior of 300nm Cu pads"*, explains Bassel Ayoub, PhD student working at STMicroelectronics, CEA-Leti and the University of Bordeaux, in a paper published in Microelectronic Engineering[7].

X-ray synchrotron Laue micro-diffraction was used to monitor the strain state and orientation of individual Cu pads in-situ during heat treatment. The experiment was conducted on the ESRF 32 beamline. *"A clear relationship between Cu pad microstructure and their mechanical behavior as a function of temperature up to 400 °C has been established"*, says Bassel Ayoub. *"With smaller pad sizes, the microstructure plays an important role in hybrid bonding."* •

7. Ayoub B., Moreau S., Lhostis S., Frémont H., Mermoz S., Souchier E., Deloffre E., Escoubas S., Cornelius T. *W., & Thomas, O. (2022)* In-situ characterization of thermomechanical behavior of copper nano-interconnect for 3D integration. *Microelectronic Engineering, 261, 111809. https://doi.org/10.1016/j.mee.2022.111809*

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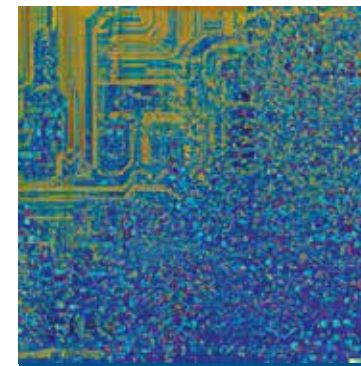
Setup used by Basel Ayoub and ESRF 32 beamline
© ESRF



How Henri Matisse would have painted an electronic circuit? Open AI Dall.e provides an answer.

© created with Open AI Dall.e, 2023

DISPLED

François Templier, Strategic Marketing manager for displays at CEA and Director of the Nanoelec/ Displed program

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CONTENTS

Towards Display Technology Leadership in Europe

The Nanoelec/Displed program prepares real breakthroughs in the display industry value chain as well as new image functionalization.

DISPLED PROGRAM AT A GLANCE

→ Vision

A unique opportunity for a French & European ecosystem on large display technologies for immersive applications

→ Ambition

To design and demonstrate key microLED technologies for high-end, immersive/ interactive displays

→ Mission

To develop process flows for microLED, Smart-pixel fabrication and mass transfer onto the display

→ Partners

Aledia, CEA, EVGroup, SET

The aim of the Displed program is to bring display production back to France.

MicroLED displays are coming, with the promise of better image quality, but with very real technical and industrial challenges. The smart-pixel, combining microLEDs with a CMOS driver at wafer level, will help solve some of them: better driving performance, simplified mass transfer, ...
The Nanoelec/Displed program is highly innovative, particularly in providing a compact, full-CMOS driven RGB microLED pixel (the smart-pixel), which is fabricated using a unique wafer-to-wafer direct hybrid bonding technique.

The aim of the program is to demonstrate the industrial scale feasibility of the Smart Pixel concept.

The project is based on creating a value chain with a focus on specific steps: assembly of microLED wafers and CMOS wafers, technologies for mass transfer of smart pixel components to a substrate. The technical hurdles relate to the technical and economic viability of the concept: transfer of very small chips on a very large scale and at very high speed. The project is built around five main work packages: wafer assembly using 200mm technology, scaling to 300mm technologies and development of packaging and mass transfer solutions for Smart Pixels. Finally, the work will undergo a demonstration phase, and a final activity focuses on the exploration of flexible, immersive, solutions for very high-end displays.

In 2022, we obtained the very first results of our pilot initiative on life cycle analysis as applied to the early R&D phase on smart-Pixel. The first proof-of-concept has been produced on a 2D-Led blue smart-pixel. We investigated two mass transfer solutions (full-wafer laser debonding of 110x110µm² dies and picking of dies as small as 75µm). We also achieved a breakthrough for 3D Integration with NanoCleave layer release technology. At the same time, our key partner Aledia has nearly completed the construction of its first production building in Champagnier.

—

Building the smart pixels

Aledia's first nanowire LED platform is now reaching promising performance levels

Philippe Gilet, CTO of Aledia (Core partner of the Nanoelec/Displed program), gave a talk at Display Week[1] (May 2022, San Jose, USA).

↑
Philippe Gilet, CTO of Aledia, presenting the very first results of the Nanoelec/Displed program to a delegation of the French National Research Agency, in September 2022.

© F.Legrand/CEA

Philippe Gilet unveiled the very first results on GaN nanowire technology for mass production of high-performance innovative displays in Europe. *"A huge display market is looking for next-generation technology"*, he reminded his international audience, presenting the promising advantages of MicroLEDs when compared with the current LCD and OLED technology[2].

"The size of the market for consumer displays alone is estimated at $120 Billion/year. Gan-on-Silicon technology will allow us to propose disruptive breakthroughs on displays: brighter, more efficient (longer battery life), new architecture for electronic integration as well as Native-RGB monolithic integration on one chip with only GaN", he adds.

The company has 220 staff and is ISO 9001 certified and benefits from more than 200 patent families. The presentation highlighted how, at low current density, small-size chips (less expensive) with 3D MicroLEDs are more efficient than with 2D MicroLEDs made on sapphire substrate. *"Aledia's 3D microLED technology enables large-area silicon to be used. We would make use of low cost and high manufacturability foundries.*

This will also allows us of easiest integration of the electronics. In 2022, Aledia demonstrated an first result on RGB active matrix display on an 8-inch silicon wafer for a blue wire-LED. Measured brightness was up to 5500 nits on a full screen (compared to <1000 nits for OLEDs and conventional displays)", says Philippe Gilet. Aledia's first nanowire LED platform is now reaching ac-

1. Philippe Gilet, "GaN Nanowire Technology : Moving to Product", *Society for Information Display, Display Week, May 8-13th 2022, San Jose, USA*

2. MicroLED uses microscopic light-emitting diodes to create images. It is a type of LED display that offers many advantages over traditional LED and LCD displays, including greater brightness, better contrast, wider color range, and lower power consumption.

ceptable performance levels. *"This platform will allow the production of LED chips ranging from 100µm down to 2µm with no efficiency change. We are on track for ramp-up production in 2023 on 200mm Si, evolving to 300mm Silicon to meet high volume demands from end 2024."*

At the International Micro/Mini LED Display Conference[3] (April 2022, Taipei, Taiwan), Philippe Gilet underlines that an emerging consensus from all major display players makes MicroLEDs 'THE' next display technology. Competition will be stiff but WireLED technology developed by Aledia in collaboration with the CEA under the Nanoelec/Displed program presents huge advantages and perfectly fits the display specification requirements. •

3. Philippe Gilet, "Moving microLED manufacturing to 300mm wafer size", *Touch Taiwan, 27-29th April 2022, Taipei, Taiwan.*

Building the smart pixels

First results on Smart-Pixel Life Cycle Analysis

Environmental impacts must be taken into account when developing any new technology. This applies to the display industry design work carried out by the Nanoelec/Displed program.

This year the SmartPixel Life Cycle Analysis (LCA) began. *"The overall objective of this study is to assess the environmental impacts of this kind of display manufacturing, considering not only climate change but also all the sixteen environmental impacts recommended by the Product Environmental Footprint method (PEF). Hence, the aim of this study is for the first time to propose a methodology based on LCA"*, explains Antonin Holo, LCA engineer at CEA-Leti, which carried out the study.

An initial set of results has been obtained, for all sixteen environmental impact categories of the PEF 3.0 method recommended by the European Commission. *"For example, the contribution of the epitaxy step could be seen with regard to every environmental impact. Etching, deposition and stripping process-family contributions were also underlined, given their large share of each of the selected environmental impacts"*, Antonin Holo reports.

Since there are no databases for microelectronics at the component scale, or the literature is outdated and does not reflect current trends, this LCA will produce new and previously unseen results. These new LCA results are used on an in-house eco-design tool, allowing comparison of new technologies with reference technology. It relies on a similar tool designed by CEA-Liten for photovoltaic R&D[4]. The fabrication flow parameters can be easily altered in order to obtain an overview of how this changes the sixteen environmental impacts addressed.

Among other results of interest is the demonstration of the impact of the electricity type (carbonated vs. nuclear) on CO_2 generation for smart pixel fabrication. *"In fact, the biggest factor impacting our carbon footprint in this process is the contribution of CMOS. If we source it from Asia, the impact on the climate is high; if we buy it from a country with a low-carbon energy mix, the balance is more favorable"*, explains Sandrine Chabaud, Safety and Environment Manager at Aledia. •

"IN FACT, THE BIGGEST FACTOR IMPACTING OUR CARBON FOOTPRINT IN THIS PROCESS IS THE CONTRIBUTION OF CMOS."

4. Nouha Gazbourg, "Systemic integration of Eco-design in photovoltaic technologies R&D", *UGA PhD Report on a doctoral thesis prepared at CEA-Liten, Feb. 2019.*

Building the smart pixels

An unprecedented eco-innovation method applicable as of the R&D phases

The methodology and the tool used for the Ecodispled project are directly adapted from the work done by CEA-Liten. Nouha Gazbour, research-engineer, and eco-innovation manager at CEA-Liten and at the Ines.2s ITE (energy transition institute), originated this development, initially intended for the eco-design of photovoltaic panels.

Why is addressing environmental issues in R&D projects still an emerging phenomenon?

Two main reasons can be postulated: on the one hand, evaluating the environmental impact is relatively complex for an immature technology currently under development (low Technology Readiness Level (TRL)), as its fabrication characteristics and processes are not yet all known; on the other, there are problems with the tools identified which limit their adoption by the R&D organizations (complex to learn how to use them, analysis of the pertinence of the results).

The work of my thesis, at the French National Institute for Solar Energy (CEA and Savoie Mont Blanc University), aimed to develop a methodology to allow lasting integration of eco-design into the R&D organizations, to support their industrial partners in their innovation and competitiveness efforts.[5]

How do you use LCA[6] in your approach?

The method developed is based on the principle of estimating the degree of technical, economic and environmental developments in a new technology (low TRL) via a reference database. LCA is the primary tool for construction of this database, in order to provide reliable results, despite the low TRL.

↑
Nouha Gazbour, research-engineer, eco-innovation manager at CEA-Liten and at the Ines.2s ITE

To what extent is this tool usable by all engineers in the PV field?

To ensure long-term adoption of this approach as of the R&D phase, the method was implemented in a computer tool for crystalline silicon photovoltaic systems, which represent more than 90% of the current PV market. The tool works by differentiation with an LCA on a reference process: you change a parameter in the process and observe the corresponding change in the environmental impact parameter.

To what extent can this tool, initially developed for PV, be transposed to other technologies, including microelectronics?

A similar methodology and tool are currently being deployed for battery technologies, hydrogen production and the recycling of materials. The microelectronics field is well represented, with the work being done under Nanoelec by Antonin Holo, LCA engineer at CEA-Leti.

This work reinforces the deployment of eco-design in the sector and the inclusion of the environmental impact of the technologies as of the very first TRL levels. It will help guide the technological choices well upstream of industrialization and deployment of the technology, so as to reduce the environmental footprint of future video screens. •

5. Nouha Gazbour, "Systemic integration of eco-design in photovoltaic technologies R&D", *Doctoral thesis presented on 14 February 2019 at Grenoble-Alpes University.*

6. Lifecycle analysis (LCA) is a method for systematic and quantified evaluation of the potential environmental impacts of a product, service or process, throughout its lifecycle. It is able to evaluate the impacts on the environment, through parameters such as depletion of natural resources, greenhouse gas emissions, water and air pollution, waste, etc.

Mass transfer of smart pixels

Next-generation 3D semiconductor packaging

One of the major steps in the process required to control the full production of a microLED display is the mass transfer of the smart pixels to the physical substrate of the display.

This step requires high fidelity and a very fast flow given that a display is composed of millions of pixels. Two core partners of Nanoelec are paving the way for mass transfer through step-by-step improvements to their wafer-to-wafer and die-to-wafer bonding tools: SET and EVGroup are key international players for more-than-Moore enabling technologies.
The breakthroughs they achieve with the support of Nanoelec represent important milestones in accelerating the deployment of heterogeneous integration in next-generation 3D semiconductor packaging, by direct hybrid bonding[7]. Such technologies are required for cutting-edge applications not only for displays but also for artificial intelligence, autonomous driving, augmented/virtual reality and 5G, all of which require the development of high-bandwidth, high-performance and low-power devices, without increasing production costs.

7. Direct hybrid bonding is a permanent bond that combines a dielectric bond (SiOx) with embedded metal to form interconnections. It requires a design with face-to-face connection of the wafers and processing with ultra flat surfaces.

Full-wafer laser debonding of dies

↑
EVG continues to grow while keeping all the production and development of its tools in Austria, in Europe, and remains committed to this strategy. The projected business growth will result in several hundred additional jobs. EVG now has more than 1200 employees worldwide and almost 1000 at its headquarters in Austria. Laurent Michaud, EVGroup engineer based in Grenoble, presented the Gemini EVG machine for 3D bonding R&D in the Nanoelec/Displed and Smart Imager Programs.

© F.Legrand/CEA

In 2021 and 2022, the Austrian supplier EVG confirmed the positive impact of Nanoelec developments on its product lines.

"The bonding sub-systems that have been developed are integrated into equipment designed, fabricated, and sold by the company", says Markus Wimplinger, Corporate Technology Development & IP Director at EV Group. This is done with an impact evaluated by the company management at several hundred million euros on advanced semiconductor markets such as memories and processors.

→ 38

"The work performed in the Displed program is enabling EVGroup to extend its roadmap in the field of heterogeneous integration based on equipment and processes for the collective manipulation of chips on wafers", Markus Wimplinger adds.

In 2022, EVG announced a breakthrough for 3D Integration with NanoCleave™ layer release technology. *"IR laser cleave technology enables nanometer-precision layer transfer through silicon, eliminating glass substrates for advanced packaging and enabling thin-layer 3D stacking. Having access to a state-of-the-art sample through a program like Displed is key to developing and improving this technology"*, explains Markus Wimplinger.

In 2021, EVG unveiled the EVG®40 NT2 automated metrology system, which provides overlay and critical dimension (CD) measurements for wafer-to-wafer (W2W), die-to-wafer (D2W) and die-to-die (D2D) bonding as well as maskless lithography applications. *"Given that EVG does not have the capability to prepare adequate test material in-house for such applications, the partnership with CEA-Leti within IRT Nanoelec is very important, as it connects us with world-leading capabilities from the other partners in this consortium. Moreover, this collaboration gives EVG access to the required materials and technologies and also enables us to perform cutting-edge research and development"*, adds Markus Wimplinger.

New milestones were reached, such as die-to-wafer fusion and hybrid bonding with 100-percent die transfer yield on a multi-die 3D system-on-a-chip. This achievement was carried out at EVG's heterogeneous Integration Competence Center™ (HICC) with a GEMINI®FB automated hybrid bonding system. The design and performance of this tool were improved thanks to previous work done with Nanoelec. •

Mass transfer of smart pixels

Picking of dies as small as 75µm

↗ **Core partner of Nanoelec, SET (Smart Equipment Technology), is a world leading supplier of high accuracy Flip-Chip Bonders.**
© SET Corporation S.A.

SET, a French instrumentation SME evaluated a vacuum tool made by CEA, on its own flip chip bonder in its cleanroom. *"After optimization, it appeared to be well handled by the equipment, and the vacuum is sufficient to manipulate micro-components as small as 75µm"*, says Pascal Metzger, CEO of SET, a core partner of Nanoelec.

With regard to the mass transfer of microLEDs, SET is working with the other Nanoelec/Displed partners on the feasibility of a concept, which is a prerequisite for an industrial machine that will be essential for the deployment of a screen production line in France and Europe. *"With the Nanoelec ecosystem, we feel we have a good lead in the field of direct bonding, particularly in terms of assembly precision and yield"*, Pascal Metzger adds.

SET has been at Semicon Europe in Munich, Germany, in November 2022. Silicon dies pictured on the booth have been assembled onto the wafer by Cu-Cu hybrid bonding process with the NEO HB equipment installed in CEA-Leti cleanroom, in the frame of Nanoelec/Displed. •

↗
The SET/NEO HB machine (ex-FC1) installed in the CEA clean room.
© Aubert/CEA

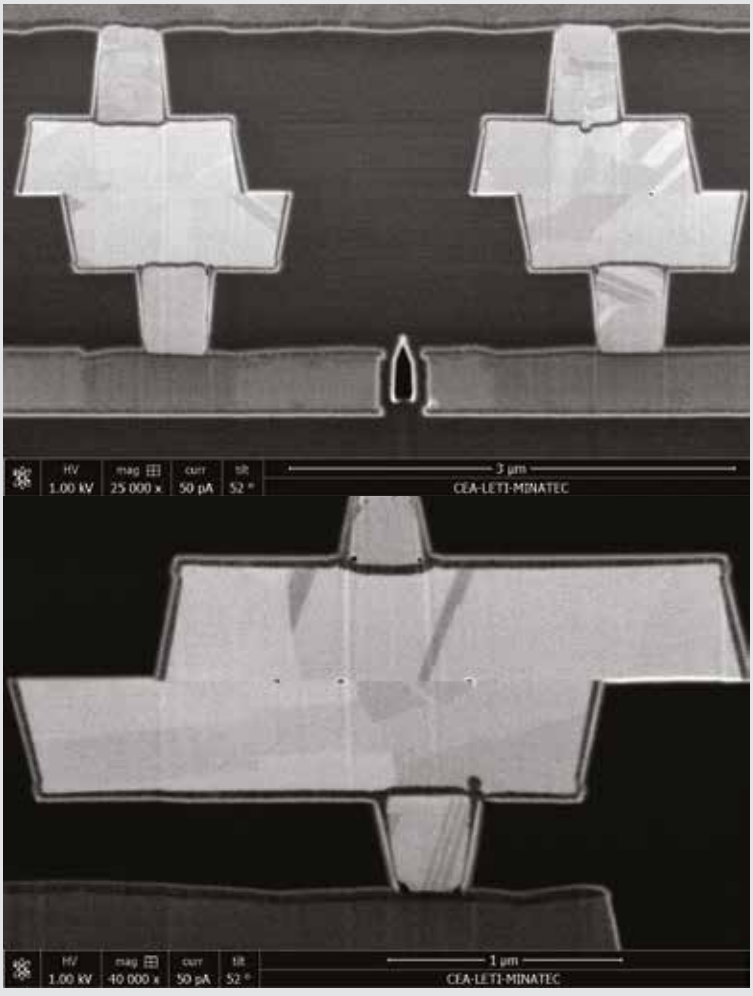
Mass transfer of smart pixels

Proof of concept for fabrication of CMOS-driven MicroLED displays

In December 2022, François Templier, CEA-Leti & Nanoelec/ Displed program director and Christophe Dubarry, a research scientist at the Silicon Component Department of CEA-Leti and a major contributor to the Nanoelec/Displed program, were invited to talk at the International Display Workshops IDW'22 in Fukuoka, Japan[9].

They reviewed challenges and solutions for the fabrication of CMOS-driven Microled Displays from classical flip-chip to fully monolithic.
"These technologies address different challenges, the connection pitch being one of them since it determines the pixel pitch. A huge number of companies and institutions are involved, which is bringing about significant progress. Overall, MicroLED and CMOS integration technologies can be leveraged to fabricate microLED displays of all sizes and types, from AR/MR microdisplays to smartphone, to TV, to outdoor panels", says Christophe Dubarry after the talk and the associated paper.

"From our viewpoint, within Nanoelec, we are developing a novel approach including direct transfer of a Gan epilayer to a CMOS active matrix. Our proof of concept has been demonstrated on 200mm wafers by direct bonding. We obtained operating MicroLEDs after the transfer process and post processing (patterning). A record pixel-pitch GaN microLED array reaches 3µm and we measured the required electrical characteristics", adds Christophe Dubarry.



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Under the Nanoelec/Displed program, CEA-Leti achieved interconnection by direct hybrid bonding with a pitch of 3 microns (FIB-SEM X-section of Copper /silicon oxide hybrid bonding area).
© CEA

These technologies address different challenges. MicroLED and CMOS integration technologies can be leveraged to fabricate microLED displays of all sizes and types, from AR/MR microdisplays to smartphones, TV displays and outdoor panels. •

9. IDW Japan: F. Templier and Ch. Dubarry, "Challenges and Solutions for the Fabrication of CMOS-driven Microled Displays" *Invited paper, International Display Workshops 2022 (IDW'22), Fukuoka, Japan, Dec 14-16 2022, (2022)*

Building the factory scale

Epitaxy

In 2022, a new Epi manufacturing tool was installed at Aledia premise in Echirolles[10], and major work was carried out in order to reach the same performance as that obtained on the CEA VA epitaxy tool.

Production building almost completed

In 2022, Aledia finalized the installation of their pilot line at Echirolles[11].

"This site was fully operational at the end of 2022 and will allow us to speed up our development and start sampling for customers in 2023", said Philippe Gilet, CTO of Aledia. The company also continued the construction of its production site in Champagnier[12]; the first equipment will be installed in 2023; the first building will cover 5000 m^2 and few hundred jobs will be created.

"Aledia's know-how is nanowires. We implant them on silicon gallium nitride to develop three types of products. The first product we address is a mono-color 2D product, what we call "blu", explains Muriel Dupont, head of R&D activities at Aledia. By integrating the know-how developed with Nanoelec, Aledia intends to develop RGB smartpixels on the same CMOS wafer in order to acquire expertise in a more powerful technology in terms of image quality. *"Of course, all of this will require considerable volume, we are currently working on 200mm silicon wafers but our goal is to be able to develop 300mm technology to ensure large production volumes at a competitive cost"*, Muriel Dupont adds. •

10. 11. 12. Grenoble Metropolitan Area

↑
Muriel Dupont, head of R&D activities at Aledia, during the Nanoelec 2022 General Assembly
© Cédrine Tresca/CEA

Building the factory scale

Production building almost completed

↑
Clean rooms ready to receive equipment in the new Aledia facility.
© Aledia

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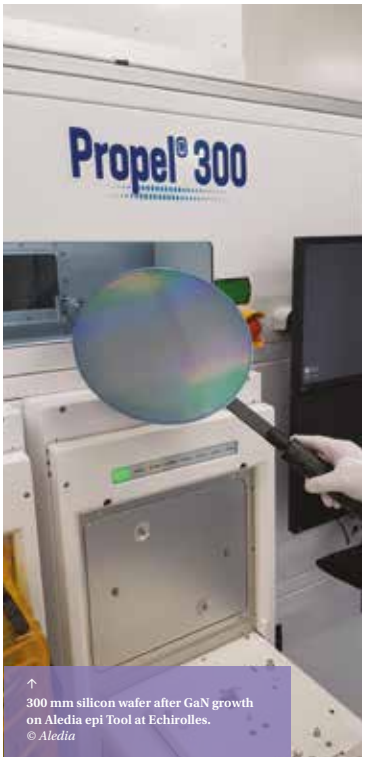
Aledia is building its new facility at Champagnier, in the Grenoble area.
© Aledia



↑
Utilities in the basement of the new clean rooms at Aledia.
© Aledia

↑
300 mm silicon wafer after GaN growth on Aledia epi Tool at Echirolles.
© Aledia

Microled receives an award

François Templier, senior expert at CEA-Leti and director of the Nanoelec/Displed program, and Marc Rabarot, engineer at CEA-Leti, won CEA's 'My invention in 3 minutes'[13] Challenge: their invention relates to the microLED display technology and unlocks the pixel size limitation.

13. At the final in Paris in June 2022, for the 'technology transfer' category

In a microLED display, each pixel is composed of a tiny LED that emits its own light. Unlike LCD displays, which use a backlight and color filters to produce images, microLED displays emit light directly from each pixel, allowing for more precise and vibrant colors, deeper blacks, and higher contrast ratios.

"Unlike OLED technology, which is made up of an organic material, micro-LEDs are made up of Gallium Nitride (GaN) and are fixed in a particular state at 900°C. Micro-LEDs can thus withstand very high current densities and therefore display a very intense light peak. This component is thermally very stable, which also ensures a very long lifetime", recalls François Templier.

"The next step is to fabricate a series of elementary units and transfer them onto a receiving substrate containing only lines and columns", explains François Templier. Each elementary unit consists of all-in-one RGB MicroLEDs on a CMOS driving circuit. Each unit is then transferred to one pixel of the receiving substrate.

"The first advantage of this approach is on the performance side: CMOS driving provides the best device performance, highest integration, and is therefore the best solution for the extremely demanding conditions of microLED driving. Another advantage is that it leaves space free in the pixel, which can then embed functions other than purely light emission (image sensing, actuation, and other) opening up a wide field of new applications and markets", says François Templier.

"CMOS DRIVING PROVIDES THE BEST DEVICE PERFORMANCE, HIGHEST INTEGRATION, AND IS THEREFORE THE BEST SOLUTION FOR THE EXTREMELY DEMANDING CONDITIONS OF MICROLED DRIVING."

The Microled breakthrough technology brings advances in multiple applications including smart lighting, augmented reality in integrated smart glasses and large/transparent, flexible 3D displays.
Would it be enough to reproduce the shimmering colors of Henri Matisse's paintings? Here is a TV Display in the Henri Matisse style.

© created with Open AI/Dall.e

PHOTONIC SENSORS

↗
Stéphanie Gaugiran (CEA), Head of the New Photonic Applications Department at CEA-Leti & Director of the Nanoelec/Photonic Sensors Program

© UtopikPhoto/CEA

Innovative building blocks to address high volume markets

The global market for optical sensors is already worth more than 20 billion dollars, with a target annual growth rate in excess of 10% for the coming decade.

PHOTONIC SENSORS PROGRAM AT A GLANCE

→ Vision

New sensor opportunities based on large-scale 300mm silicon photonic technologies

→ Ambition

Enrich our photonic prototyping and industrial platforms with key building blocks enabling new sensors to address Medtech, Environment, Consumer goods, Mobility (Lidars) and Computing

→ Mission

- Miniaturize sensors
- Diversify the fields of application
- Manage the integration of thousands of functions on the same chip
- Increase technology readiness level using CAD tools and enrich our device library including performance corners, fabrication process flow

→ Partners

Almae, CEA, CNRS, Siemens EDA, STMicroelectronics

The "Photonic Sensors" program aims to expand the scope of the silicon photonics platform developed by Nanoelec since 2012 through the integration of innovative building blocks to address high volume optical sensor markets (Consumer Electronics, Industrial, Automotive & Transportation, Smart city, Cybersecurity, Food & Beverage, and Medical Care).

Key Technologies will address the development and demonstrations for integrated Lidars targeting consumer and automotive applications, inertial sensors and biochemical sensors for health and environmental applications.

In 2022, we demonstrated a 256-channel Optical Phased Array at 1,550nm consuming only 0.54W. We updated the Silphide and PIC 50G architecture design kits. We produced complete and functional LED structures at 700nm on 300mm wafer overcoming the N-doping obstacle, and demonstrated III-V epitaxy bonding on PIC with oxide gate in the 5-15nm range. We also carried out the first functional integration of the DAN1 laser (III-V/SI hybrid components) on 200mm wafers.

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Photonic applications

Industry standard manufacturing of Lidars

Stéphane Monfray is senior principal engineer at STMicroelectronics, in charge of the development of disruptive technologies. Within Nanoelec, he supervises the development of manufacturing on the 300mm photonic platform for components for Lidar type applications.

↑
Stéphane Monfray is senior principal engineer at STMicroelectronics, in charge of the development of disruptive technologies.
© Cédrine Tresca/CEA

What is your objective regarding Lidar development?

As a long-range 3D imaging component, the Lidar is among the various solutions to speed up the arrival of self-driving vehicles.

However, their widespread deployment for a mass market such as automotive remains a challenge. Why?

Technologically speaking, 3D long-range imaging is required and the solutions today available are often voluminous and costly because they are based on mechanical rotary systems. With Nanoelec, using the potential of photonics, we are hoping to develop compact systems, with no moving parts, that are efficient and reliable enough to meet the extremely demanding requirements of intense and low unit cost industrial production capable of supplying the automotive sector.

You are developing miniaturized Lidars based on OPA (Optical Phased Arrays). What are they?

An OPA[1] is a light source distributed over an array of channels in which the phase of the light is electrically controlled by an electronic chip. All these rays of light converge on an array of output channels. According to the phase shift applied between the input and output channels, you generate interference coupling, in other words the light beam can perform an angular scan of an entire zone in front of the sensor. The idea is therefore to have a light source with scanning, but which is completely integrated on a chip produced on industrial standard 300mm silicon wafers.

1. In photonics-electronics, OPA (optical phased array) refers to arrays of lasers or SLMs with addressable phase and amplitude elements smaller than a wavelength of light.

The component on-board a vehicle could scan the scene at long range and with sufficient beam resolution to precisely image a field of several tens or even several hundreds of meters of distance.

Within Nanoelec, the first OPA demonstrator was produced in 2022 on the 300mm photonics platform of STMicroelectronics. How is it performing?

This year we did indeed produce a 256-channel demonstrator which enabled us to achieve particularly precise beam resolution (less than 0.2 degrees) for an angular scan of plus or minus 30 degrees. We thus achieve resolution from few centimeters to several tens of meters.

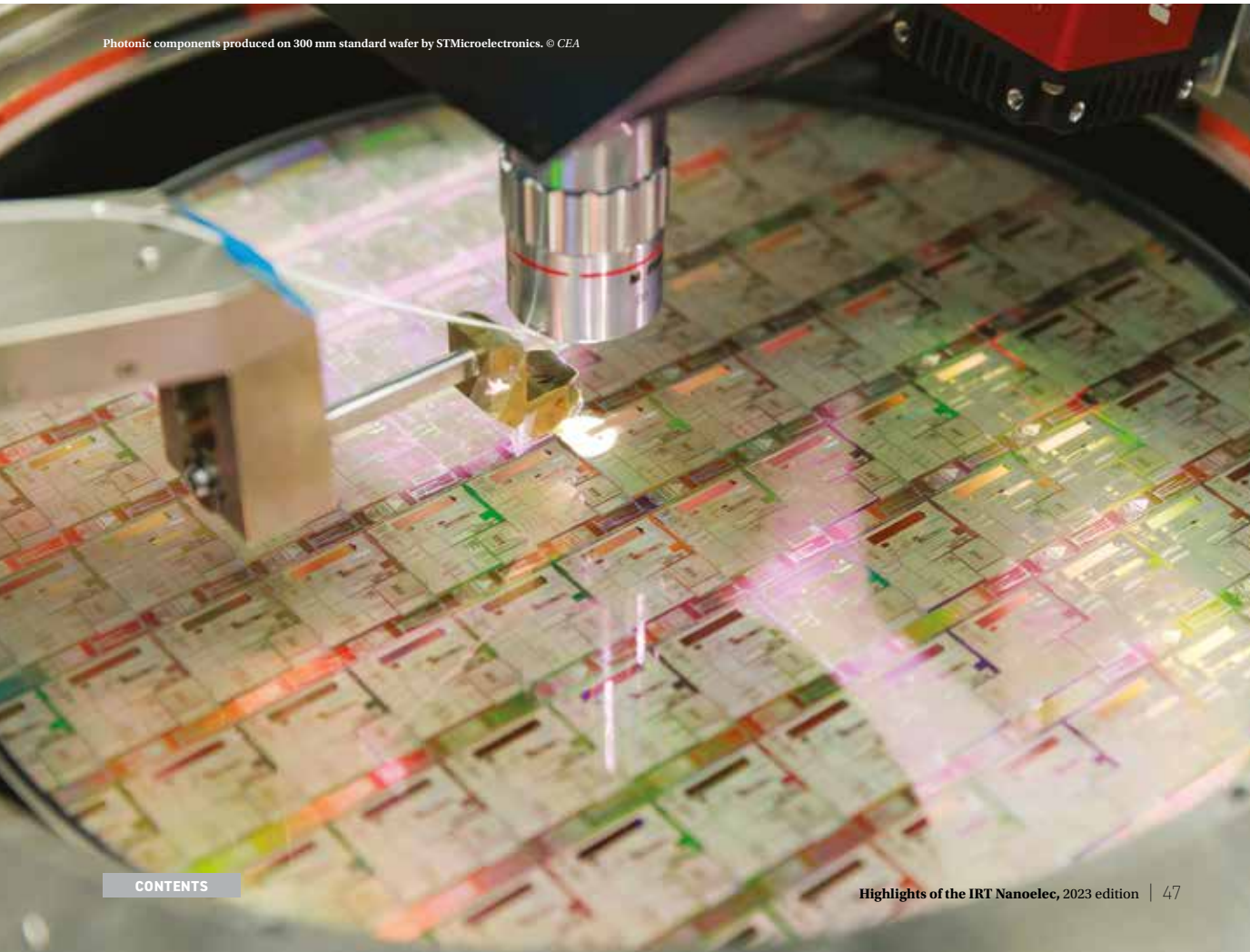
What resources did you use?

Within the IRT, we had to develop appropriate optical benches for detailed characterization of the performance of these new components; this is relatively complex because our OPA chip has to be driven by a dedicated PCB which electrically controls 256 channels via specific connectors. The beam output is imaged by a camera mounted on an arm which must be capable of following the scan by the output beam.

"THIS OPA CAN BE INTEGRATED FOR LIDAR APPLICATIONS, MANUFACTURED ON THE 300MM PLATFORM."

What are the prospects for the solution you are developing?

This OPA can be integrated for Lidar applications, manufactured on the 300mm platform. With energy consumption of less than one milliwatt, it is a particularly efficient system. In addition to the self-driving car market, it could also be used for other applications, such as free-space optical communications (LiFi Type), and it is compatible with future integration of a laser source on a chip. •



Photonic components produced on 300 mm standard wafer by STMicroelectronics. © *CEA*

Photonic applications

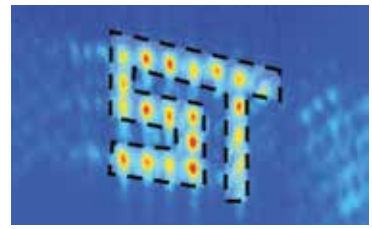
An Optical Phased Array demonstrates high angular resolution at 1550nm

Thanks to efficient phase shifters, the total electrical power consumption is as low as 1mW for a whole OPA circuit.

An optical phased array (OPA) is a device that controls the direction of a laser beam without the need for any moving parts. It uses a series of small optical antennas, each with its own phase shifter, to manipulate the phase of the light. By adjusting the phase of each antenna, the OPA can change the direction of the laser beam without physically moving the device.

"In 2022, we were able to fabricate and fully characterize an Optical Phased Array (OPA) with 256 antennas", explains Sylvain Guerber, photonics engineer at CEA-Leti. *"Our demonstrators operate at 1,550nm wavelenght[2], moreover thanks to efficient phase shifters, the total electrical power consumption is as low as 1mW for the whole circuit."*

OPAs have many potential applications, including free-space optical communications, Lidar systems[3], and optical sensing. OPA based Lidars offer advantages over traditional mechanical beam steering methods, such as faster response times, higher precision, and lower power consumption.



During characterization of a first Lidar produced using 300 mm photonic technology by CEA and STMicroelectronics within Nanoelec: by slightly modulating the input wavelength of the laser beam, it was possible to vary the angle of the beam in both dimensions. In this demonstration, a small ST logo was written on the characterization infrared camera (angular dimensions ~3°*2°).

© DR

OPAs also face challenges in terms of scalability and cost-effectiveness, as the number of antennas required to achieve high angular resolution can be very large.

"We have achieved angular resolution of 0.18° by increasing the number of channels from 16 to 256", Sylvain Guerber adds. •

2. One of the most commonly used infrared wavelengths in optical fibers.

3. Light Detection and Ranging (LiDAR) is a remote sensing technology that uses laser light to measure distances between a LiDAR sensor and the surrounding objects. Time of flight LiDAR systems emit laser pulses that bounce off surfaces and return to the sensor, which measures the time it takes for the pulse to return. By measuring the time of flight and the direction of the pulse, the LiDAR system can then create a three-dimensional map of the object or environment being scanned.

Sylvain Guerber (CEA-Leti) prepares a series of tests on the new "Lidar bench" set-up installed in 2020. The white fiber is used to inject light into the circuit. In red: a camera observes and measures the steering of the beam exiting the Lidar.

© P.Jayet/CEA

Circuit design and testing development tools

Process Design Kit for C-Band components

Design rules has been updated to meet the need for new components industrial processes.

↑
Eleonore Hardy is Business developer in silicon Photonics at CEA-Leti and Deputy Director of the Photonic Sensors program at Nanoelec.

© UtopikPhoto/CEA

A process design kit (PDK) is a set of data files, and documentation that supports design tools used in the development of integrated circuits (ICs). It provides a standardized methodology for designing and manufacturing ICs, which is crucial for ensuring that they function properly[4].

The PDK typically includes information about the IC fabrication process, such as the layer stack, the process steps, and the materials used. It also includes design rules, which specify the constraints on the layout of the IC. *"In 2022, we updated the PDK of the ST-Microelectronics platform, namely PIC 50G[5], specifically its design rule check (DRC) module. Design rules were updated or created to meet the new needs of the STMicroelectronics industrial R&D sector"*, says Eleonore Hardy, Deputy Director of the Photonic Sensors program at Nanoelec.

"We specifically implemented a new two-level metal option for BEOL[6], as well as creating more than 20 new components for C-band[7] (1,550nm)", adds Eleonore Hardy.

PDKs are typically provided by semiconductor foundries, which are companies that specialize in the fabrication of ICs. Each foundry typically has its own PDK, tailored to its specific process technology. This allows designers to choose the foundry that best suits their needs, based on factors such as cost, performance, and power consumption.

"The component library of the Silphide 300mm PDK[8] has been updated to meet the need for new components, particularly in the C Band", explains Tom Daspit, Product Manager Custom IC at Siemens EDA, involved in the Nanoelec/Photonic Sensor Program. These actions are part of the rise in maturity of the photonics

→ 50

4. Using a PDK, designers can create IC layouts that comply with the design rules and can be manufactured using the specified process. The PDK also allows designers to simulate the electrical behavior of the IC before it is fabricated, which can help to identify and correct any potential issues.

5. Dedicated to the STMicroelectronics 300mm industrial R&D platform

6. In photonics, BEOL stands for "Back End of Line". It refers to the processing steps that occur after the active devices have been fabricated on a semiconductor substrate, such as adding metal interconnects, passivation layers, and bonding pads. BEOL processing is essential for connecting the active devices to the outside world, allowing their integration into larger systems and circuits.

7. C band optical refers to a specific wavelength range in the electromagnetic spectrum that falls within the C band of the optical fiber communication window. The C band optical range runs from approximately 1,530nm to 1,565nm.

8. Dedicated to CEA's 200mm and 300mm R&D technologies

industry with the integration of the latest developments in manufacturing processes, design rules and the addition of new components that are cheaper, more efficient and aimed at new datacom and sensing applications such as 3D sensing.

"Silphide PDK has been enriched through a brand-new methodology to simulate photonic integrated circuits (PIC) using commercial IC simulators", explains Emeric de Foucauld, expert in high-precision modelling and simulation for Si technologies at CEA-Leti.

Photonic devices - including transmission and reflection of light - are modeled using Verilog-A language so they are easily usable for any type of simulator. *"For each model, both polarizations, transverse electric (TE) and transverse magnetic (TM) polarized waves, are considered. The methodology allows resonant and interference effects to be simulated, as well as waveguide and ring resonator"*, adds Emeric de Foucauld, first author of the publication reporting on this work in Solid State Electronics[9]. •

9. De Foucauld E., Rozeau O., Myko, A. Fowler, D. Virot, L. & Gays, F. (2023). Compact modeling of photonic devices in Verilog-A for integrated circuit design. *Solid-State Electronics, 200, 108538. https://doi.org/10.1016/j.sse.2022.108538*

Circuit design and testing development tools

Characterizing an OPA

A CEA-Leti team has unveiled a new methodology for fast calibration of OPA circuits.

"We demonstrated the wafer-level characterization of a 256-channel optical phased array operating at 1,550nm, allowing the sequential testing of different OPA circuits without any packaging steps", explains Sylvain Guerber, research engineer in photonics at CEA-Leti, as the first author of an important paper in Optics Express[10].

"Due to random fabrication variations, nominally identical circuits must be individually calibrated. Thus, we investigated methods that significantly reduce the time needed to calibrate each OPA circuit. For a 256-channel OPA, we find that a genetic optimization algorithm is already more than three times faster than a simple hill climbing algorithm. Furthermore, the phase modulators within the OPA may be individually characterized 'in-situ' and this information can be used to configure the OPA to emit at any arbitrary angle following a single, initial calibration step." •

10. "Wafer-level calibration of large-scale integrated optical phased arrays" S.Guerber et al. Optics Express *35246 Vol. 30, No. 20 / 26 Sep 2022, https://doi.org/10.1364/OE.464540.*


"WE INVESTIGATED METHODS THAT SIGNIFICANTLY REDUCE THE TIME NEEDED TO CALIBRATE EACH OPA CIRCUIT."
S. GUERBER (CEA-LETI)
© CEA-Leti

Photonic device integration

Industrial standard red LEDs were produced

Unprecedented results in the epitaxy of III-V materials on silicon in 300mm.

Within Nanoelec, the Microelectronic Technologies Laboratory (CNRC-UGA) and CEA-Leti have together developed red LEDs based on III-V materials (gallium arsenides and phosphides) using direct epitaxy on silicon.

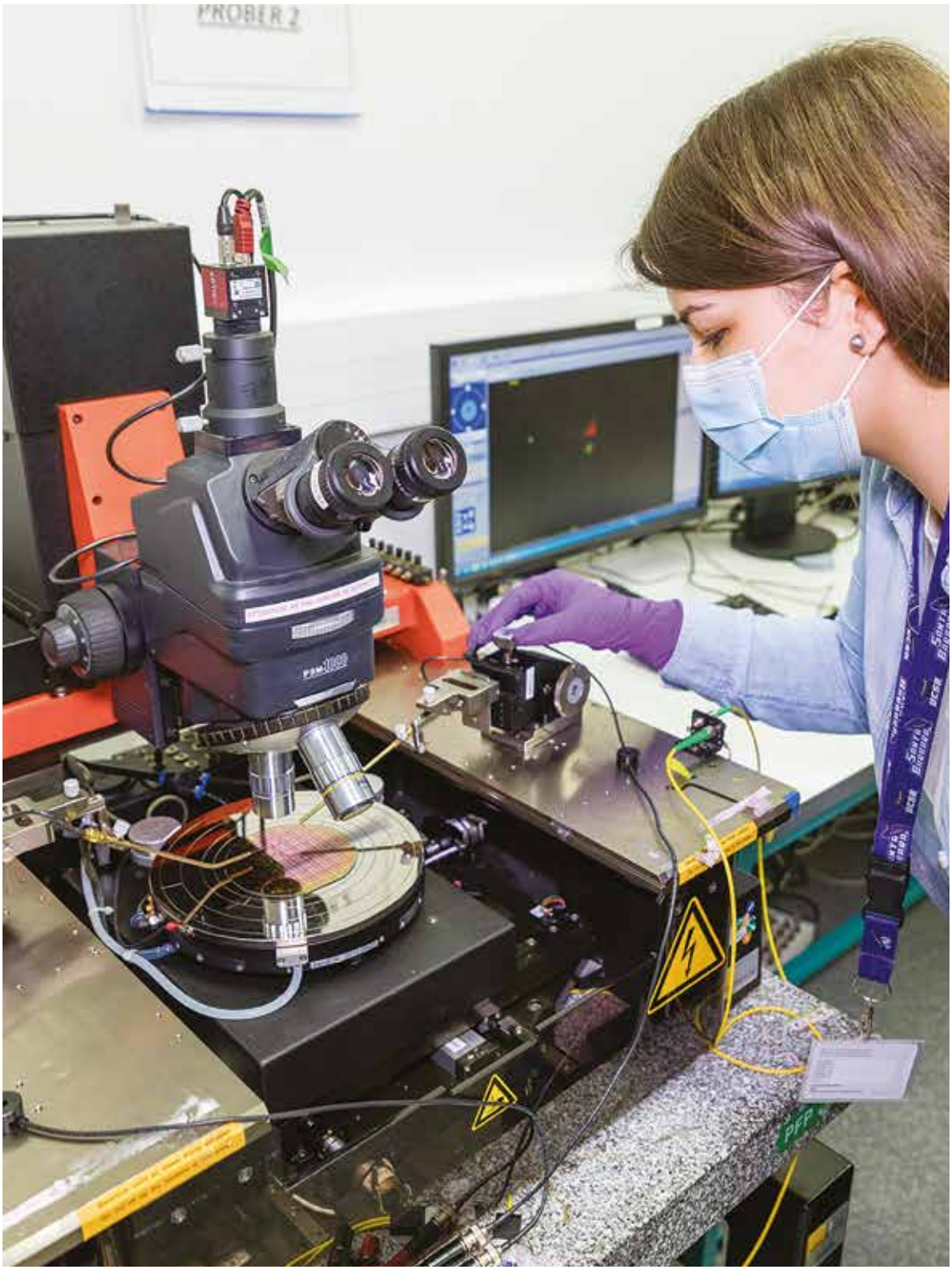
"LEDs are routinely fabricated via epitaxy on a low-diameter III-V substrate (100 and 150mm typically)", says Christophe Jany, Head of the Photon Technologies Integration Laboratory at CEA-Leti. *"Through Nanoelec, we have acquired expertise in direct epitaxy on silicon in 300mm: it is a less costly substrate that is compatible with the most productive industrial standards."*

In 2022, the teams involved obtained unprecedented results in direct epitaxy of stacks of III-V materials on silicon[11] : the growth process for the complete stack of the red LED hetero-structure based on In0.51GaP/(Al0.5Ga0.5)0.5InP was developed. → 54

11. The III-V materials are semiconductor compounds consisting of atoms of column III and column V of the periodic table of elements, such as gallium arsenide (AsGa), indium phosphide (InP), gallium nitride (GaN) and aluminum-gallium arsenide (AlGaAs). These materials have electronic characteristics that are well-suited to photonics.

↑
Mickael Martin, microelectronics engineer at the CNRS. MOCVD III-V (Metal-Organic Chemical Vapor Deposition) epitaxy deposition platform control console – Operated by the Microelectronic Technologies Laboratory (CNRS-UGA) and CEA-Leti, this machine was used to develop industrial standard red LEDs.

© P. Jayet



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Pauline Gaillard (LTM) tests the red LEDs developed by the Microelectronic Technologies Laboratory (CNRS-UGA) and CEA-Leti.
© P. Jayet

SiN WG patterning (combining hard mask strategy patterning and the plasma etching steps involved in WG fabrication) is one of the solutions for accurately controlling the roughness of the SiN waveguide sidewalls and thus controlling SiN-based photonic platform performance (in terms of optical losses). The Microelectronic Technologies Laboratory (CNRS-UGA) has the know-how, not only to pattern SiN WG with low roughness, but also to quantify the sidewalls roughness present after patterning thanks to its powerful 300mm etching platform and its expertise in sidewalls roughness metrology.

© P. Jayet/CEA

"The growing interest in red-green-blue LED developments can be explained by the explosion of new applications using micro-screens for virtual and augmented reality", says Pauline Gaillard, PhD student at the LTM and CEA-Leti[12] and then hired at STMicroelectronics in 2023. *"These components must be extremely bright so that they are visible in an environment that can be strongly lit, with high image definition produced by increasingly small pixels: only micro-LEDs can meet these criteria."*

The Nanoelec project mainly concerns inorganic LEDs, red emitters in particular, which are the most complex to develop of the three colors required. "*We have demonstrated that it is possible to produce red LEDs through direct epitaxy on silicon, to the 300mm industrial standard. Even if our efficiency still needs to be improved, this work opens the door to possible mass production at low cost"*, concludes Pauline Gaillard. •

12. Pauline Gaillard, "Développement de LEDs rouges en matériaux III-V (type AsGa) directement épitaxié sur silicium 300mm", *PhD thesis presented to the UGA on 21 February 2023*

Photonic device integration

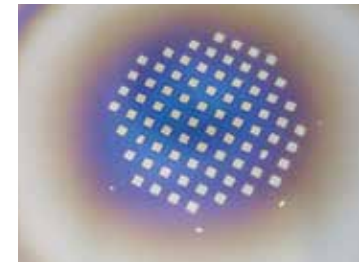
Capacitive modulators for Lidars

Hybrid III-V capacitive modulator on photonic wafers were fabricated by CEA and STMicroelectronics.

To control the beam scan in a Lidar, capacitive modulators are used to create the phase-shifters of OPA circuits[13]. *"In 2021 and 2022, we developed an approach based on a III-V/Si hybrid capacitor, in which the n-doped silicon was replaced by an InGaAsP quaternary alloy",* explains Valentin Ramez, Photonics Engineer at CEA-Leti. *"Our design studies led to testing structures and demonstration circuits based on OPA using the Alcor mask from STMicroelectronics."*

2022 was devoted to developing the fabrication process for this hybrid capacitor on photonic wafers fabricated by STMicroelectronics. *"We were able to demonstrate that it was possible to planarize the wafers and produce Si/InGaAsP capacitors for which the gate oxide was about 5-15nm. At the same time, wafers were fabricated using the Alcor mask for demonstrations of functional components (modulators and OPAs) and are currently being planarized at CEA-Leti"*, says Valentin Ramez. *"The fabrication of these components should enable us to conduct a first demonstration of a modulator integrated into a circuit in 2023."*

13. The capacitive effect maximizes the charge concentration while limiting consumption and is obtained by integrating an oxide coat into the waveguide.



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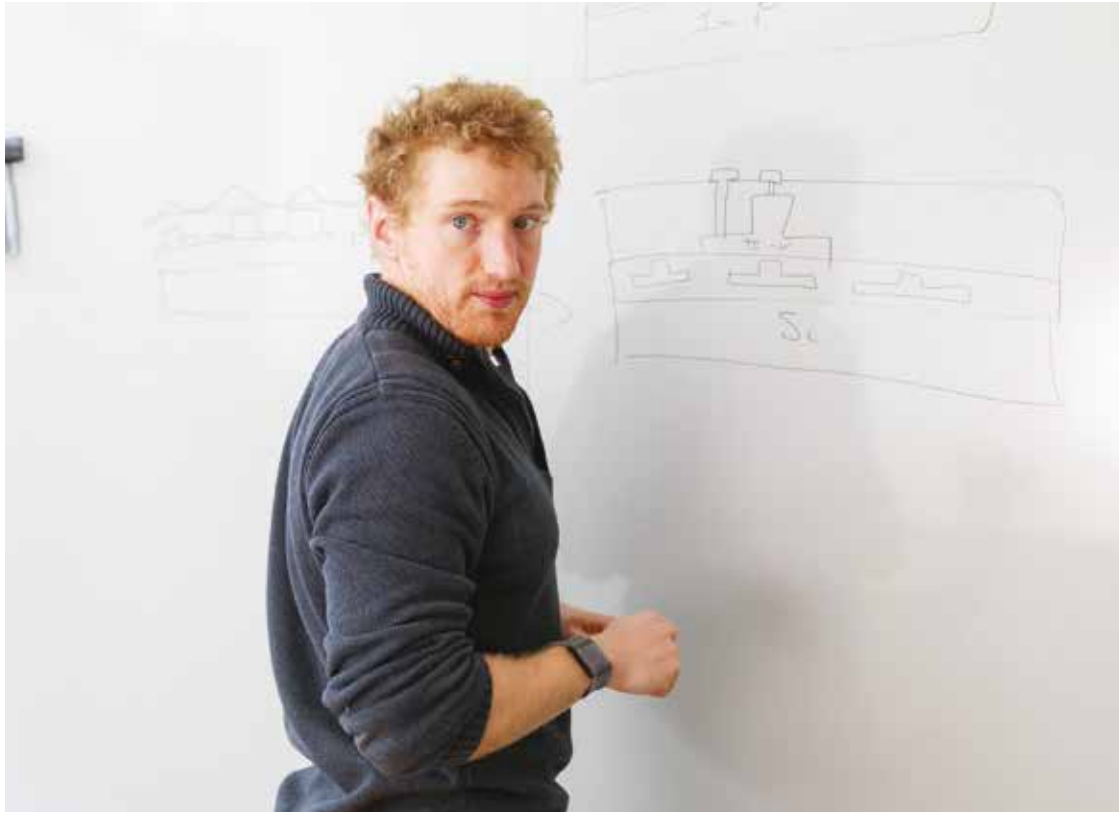
Fabrication process for hybrid modulator on photonic wafers is on going.
© P.Jayet/CEA



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Valentin Ramez, photonics engineer at CEA-Leti, schematizing the process of hybrid bonding for III-V/Si modulator. *© P.Jayet/CEA*

Team of Scintil Photonics. The startup spun off from Nanoelec and CEA-Leti, and associated with the Nanoelec/Photonic Sensors program, has raised €15m in 2022.

© Jayet/CEA

View of the Photonic Plateform of the CEA where are mainly conducted actions of the Nanoelec/Photonic Sensor program.

© CEA

Photonic device integration

Driving the computing architectures of the future

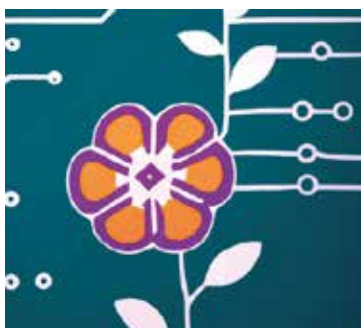
↑
Christophe Kopp, Deputy Director of the Optics & Photonics department at CEA-Leti.
© P.Jayet

The Nanoelec Photonic Sensors program will contribute to the emergence of radically new computing architectures.

In January 2022, a CEA team working on the Nanoelec Photonic Sensors program published a review in French of the promising prospects for photonics on silicon[15]. This technology combines the optical advantages of silicon with the fabrication methods of microelectronics, thus opening the door to new forms of acquisition, transmission and processing of information.

"Photonics on silicon is compatible with production chains supplying demanding mass markets such as automotive or personal computing and IOT and is already penetrating the optical sensors markets. In the medium term, it will be crucial for the emergence of new computing architectures (including the quantum computer and artificial intelligence)", says Christophe Kopp, Deputy Director of the Optics & Photonics department at CEA-Leti, who coordinated this article. •

13. Kopp, C., Szelag, B., Hassan, K., Guerber S., & Charbonnier, B. (*2022, February)* "Le silicium à la conquête de la photonique". *Industrie et Technologies, 1050.*



How Henri Matisse would have painted an electronic circuit? Flowers and fruit being Matisse's great inspirations, he would undoubtedly have included them in his own PDK. Open AI Dall.e provides an answer.

© created with Open AI Dall.e, 2023

PULSE

Inter-connected and smarter systems are now vital

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Vincent Cachard (CEA), Nanoelec/PULSE Program Director, and Manager of the Hardware Security Research department at CEA-Leti

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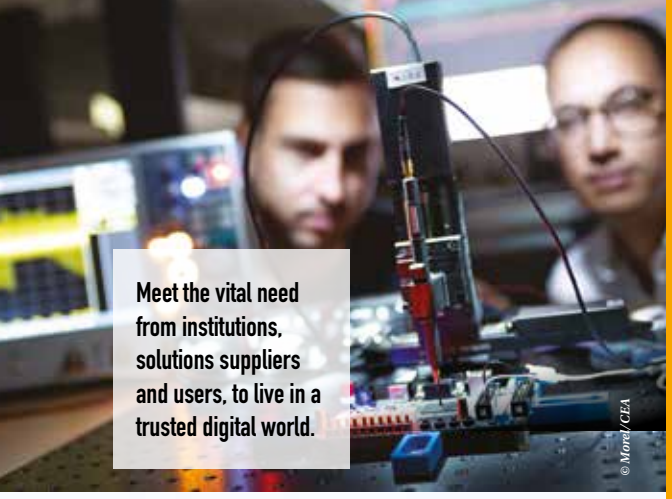

PULSE PROGRAM AT A GLANCE

→ Vision

Due to the rise in cybercrime, Internet of Things (IoT) cybersecurity is a major challenge for digital trust. Strengthening and hardening critical embedded, increasingly interconnected and smarter systems are now vital

→ Ambition

New smart and intrinsically secure nanocomponents to reinforce the resistance of systems against future cyberattacks + improved security of smart embedded systems throughout their lifecycle (including AI algorithms) + safer deployment environments through digital ID, data sovereignty and secure interactions between smart systems

→ Mission

To develop and test new security features for components and systems in three fields of application: Industry 4.0, homecare and robotics

→ Partners

CEA, Diabeloop, Grenoble INP-UGA, Inria, Schneider Electric, STMicroelectronics, UGA

With the advent of the Internet of Things (IoT), new services based on heterogeneous connected devices and data management are multiplying. At the same time, the dramatic increase in the number of cyber-attacks is raising awareness among the public and institutions about the risks associated with a too rapid and poorly controlled digital transition.

New hardware and software vulnerabilities are being identified and revealed to the general public at a time when medical devices, automobiles, industrial and urban equipment are becoming increasingly connected and autonomous. These vulnerabilities and the attacks that exploit them are undermining user trust in connected services and goods. Consequently, they have an impact on the image of businesses, but also on society's economy and citizen privacy. They can even compromise the legal and social liability of public or private players who have inadequately protected their products.

In addition, when designing digital products, cybersecurity is often seen as a constraint which should not weigh too heavily on primary functions (health, mobility, manufacturing, etc.), whether in terms of cost, performance, or ergonomics.

The challenge of the Nanoelec/PULSE program is thus to identify how electronic technologies can provide an adequate response to this new paradigm. It aims at developing new technologies that will allow the emergence of connected products and services that are capable of increasing security, protecting confidentiality, authenticity and integrity of digital data, guaranteeing protection of privacy, and simplifying the deployment of cybersecurity strategies. Our work focuses on three application fields: cybersecurity of industrial systems cybersecurity of healthcare products, and security of autonomous systems and self-driving cars.

In its own way, the Pulse program aims to meet the vital needs of institutions, solutions suppliers and users to live in a trusted digital world.

The work conducted in 2022 focused on the following:
- Integrated circuit micro-architectures that are intrinsically secure against attacks.
- Strong embedded systems ready for the quantum world challenges and enabling secure artificial intelligence.
- Secure, efficient, trusted and sustainable deployment schemes for objects.

These concepts have been applied to three application cases: industrial and manufacturing systems, home health and medical devices, and robotics.

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Home & health cybersecurity

Reliable connected medical devices

Most connected objects and connected medical devices currently on the market take little or no account of cybersecurity requirements.

"While software security and personal safety are taken into account — e.g., CE marking for medical devices — hardware security has still not been integrated into certification and industrialization schemes in France and Europe", explains Christophe Villemazet, Deputy Director of the Nanoelec/Pulse program.

More and more attacks happen through connected devices, which, in turn, become the gateway to critical infrastructure such as hospitals. *"Still highly vulnerable to cyberattacks, French hospitals are increasingly being targeted by cybercriminals looking to steal healthcare data which they can sell at very high prices"*, according to three cybersecurity experts from online media La Tribune. They cited two examples of cyberattacks in France in 2022: "*After hacking the Corbeil Essonnes hospital and demanding a 10-million-dollar ransom, the cybercriminals leaked administrative and personal records. A few weeks later, it was the turn of the Versailles hospital to fall victim to a cyberattack.*"

Cybersecurity of medical devices (MDs) has become a major concern for manufacturers and healthcare organizations. Their main challenge is protecting patients, and ensuring healthcare data confidentiality and integrity.

"THE HIGH-LEVEL TECHNICAL SOLUTIONS THAT NANOELEC OFFERS ARE PERFECTLY SUITED TO ADDRESS SUCH ISSUES, AND TO SUPPORT OUR MISSION: TO IMPROVE THE HEALTH OF THOUSANDS OF DIABETIC PATIENTS."

"Operational (resistance to physical and malware attacks), authenticity (proof of integrity) and confidentiality (resistance to reverse engineering) issues are major challenges for the AI embedded systems of our automated insulin delivery devices", explains Erik Huneker, Co founder and CEO of Diabeloop, core partner of Nanoelec. *"The high-level technical solutions that Nanoelec offers as part of its PULSE program are perfectly suited to address such issues, and to support our mission: to improve the health of thousands of diabetic patients."*

The overall development of this technology in healthcare is a means to enhance patient service and to enable healthcare workers to better treat patients. However, it also increases the risk of cyberattacks and leakage of confidential medical records. *"MD manufacturers can rely on European regulations to comply with patient or software security requirements. Nowadays, however, there is no standard defining hardware protection requirements for MDs, nor the means to ensure their relevance and effectiveness"*, notes Christophe Villemazet.

↗ **The DBLG1 from French manufacturer Diabeloop.**
© Diabeloop

In this given context, Nanoelec/PULSE partners are jointly examining hardware and software security of connected medical devices, as well as that of gateways that translate data output (risk analysis, vulnerability assessment, search of security flaws, penetration testing); recommending suitable cybersecurity countermeasures; providing industries with guidance concerning cybersecurity-oriented design (technical specifications, design, evaluation); and analyzing the security of overall system architectures.

In 2022, the SecWay demonstrator for the protection of sensitive data — particularly medical data — was designed through Nanoelec.

"SecWay, a gateway for secure data, has been developed for medical applications. It is poised to become a standard solution for our product ranges", explains Thierry Fensch, Innovation and Collaboration Director at STMicroelectronics Grenoble. As part of the Nanoelec/PULSE program, a first SecWay prototype was completed in 2021. In 2022, an improved version includes security features. *"Based on mass-market microprocessor STM32MP1, SecWay is currently undergoing approval for use in several European projects (GateKeeper, DigiFed…), and with industrial partners"*, specifies Thierry Fensch. Implemented using a security-by-design approach, the prototype's system architecture is based on secure electronic components (TrustZone, TPM). Its software blocks ensure end-to-end security.

"This demonstrator will enhance the R&D development capabilities of our partners and customers. They will have access to our technologies within a complex system with embedded security", adds Thierry Fensch. *"The new gateway also represents a societal advancement to secure connected medical systems: it facilitates remote patient monitoring and increases the possibility of empowering the frail and elderly."*

"We offer secure hardware and software technologies that enable the implementation of artificial intelligence in the embedded systems for healthcare applications and medical devices", concludes Christophe Villemazet. •

↗
Package of SecWay prototype designed by CEA/Y.Spot. © *P.Jayet/CEA*

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SecWay is a secure data gateway developed for medical applications. © *P.Jayet/CEA*

Home & health cybersecurity

Tools and technologies for trusted components

ScrambleCache is a hardware countermeasure that improves two of the most widely exploited security mechanisms: cache randomization and partitioning. Its effectiveness has been established by a proof of concept with write-through cache memory, using a FPGA demonstrator with a RISC-V CVA6 processor. Two patents are pending.

↑
ScrambleCache presented at ECW 2022.
© CEA

Attacks on embedded systems are on the rise, and the skills needed to secure embedded code are too complex for an average developer to acquire. There are yet numerous flaws which represent a risk to a system's reliability. Cache memory reduces the time it takes to access data between the main memory and the processor, but it is vulnerable to cache-timing attacks, which can be used to obtain sensitive data or encryption keys.

"At Nanoelec, we address this issue by designing intrinsically secure processors that can prevent the exploitation of remaining design flaws", explains Mustapha El Majihi, research engineer at CEA-Leti. *"Designing such processors requires exhaustive knowledge of their vulnerabilities. We rethink the processor overall processor security and implement a consistent sequence of countermeasures to ensure end-to-end confidentiality, integrity and authenticity of data and instructions; in other words, Flash memory up to the execution level in the pipeline",* adds Olivier Savry, Expert in electronic components security at CEA.

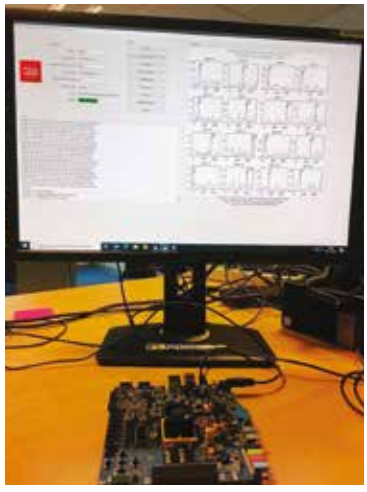
Differences in data processing can remain depending on its availability in the memory cache. A memory request may be longer (miss) if it is not already present in the cache (hit). This difference can be exploited by an attack process to recover addresses manipulated by a victim process, and thus gain access to processed data. Such attacks can be used to find an AES encryption key, for example.

"For the past several years, we developed the ScrambleCache[1] *solution to overcome cache vulnerabilities. It entails dynamic partitioning and randomizing cache addresses thanks to a random bit mixed with the cache index. A history table helps to find data to avoid routinely clearing and reloading the cache"*, continues Mustapha El Majihi.

Based on an RISC-V CVA6 application-class processor with L1 write through cache the demonstrator has shown that Evict+Time and Prime+Probe attacks, which use the fastest state-of-the-art search algorithms of eviction sets, are no longer possible, once countermeasures are activated. Two patents are pending. The demonstrator was presented at the 2022 European Cyber Week, and will be presented at RISC-V Summit Europe in June 2023[2].

1. Cache memory reduces the time it takes to access data between the main memory and the processor. It is vulnerable to cache-timing attacks, which can obtain sensitive data or encryption keys.

2. RISC-V Summit Europe is the premier event that connects European movers and shakers, from industry, government, research, academia and ecosystem support, who are building the future of innovation on RISC-V. *June 2-5, 2023, Barcelona, Spain*



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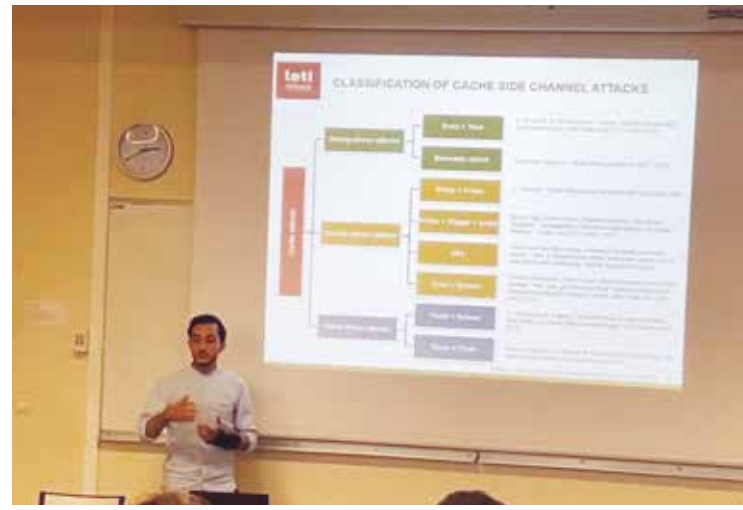
ScrambleCache demonstrator developed by CEA-Leti as part of the Nanoelec/PULSE program.
© CEA

Home & health cybersecurity

Protecting process isolation in multi-task components

Defended in 2022, the following Nanoelec thesis provides a comprehensive study of the most common cache side-channel attacks.



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Amine Jaamoum, who was recently hired at Thalès Digital Identity & Security after having defended his thesis as part of Nanoelec.
© *DR*

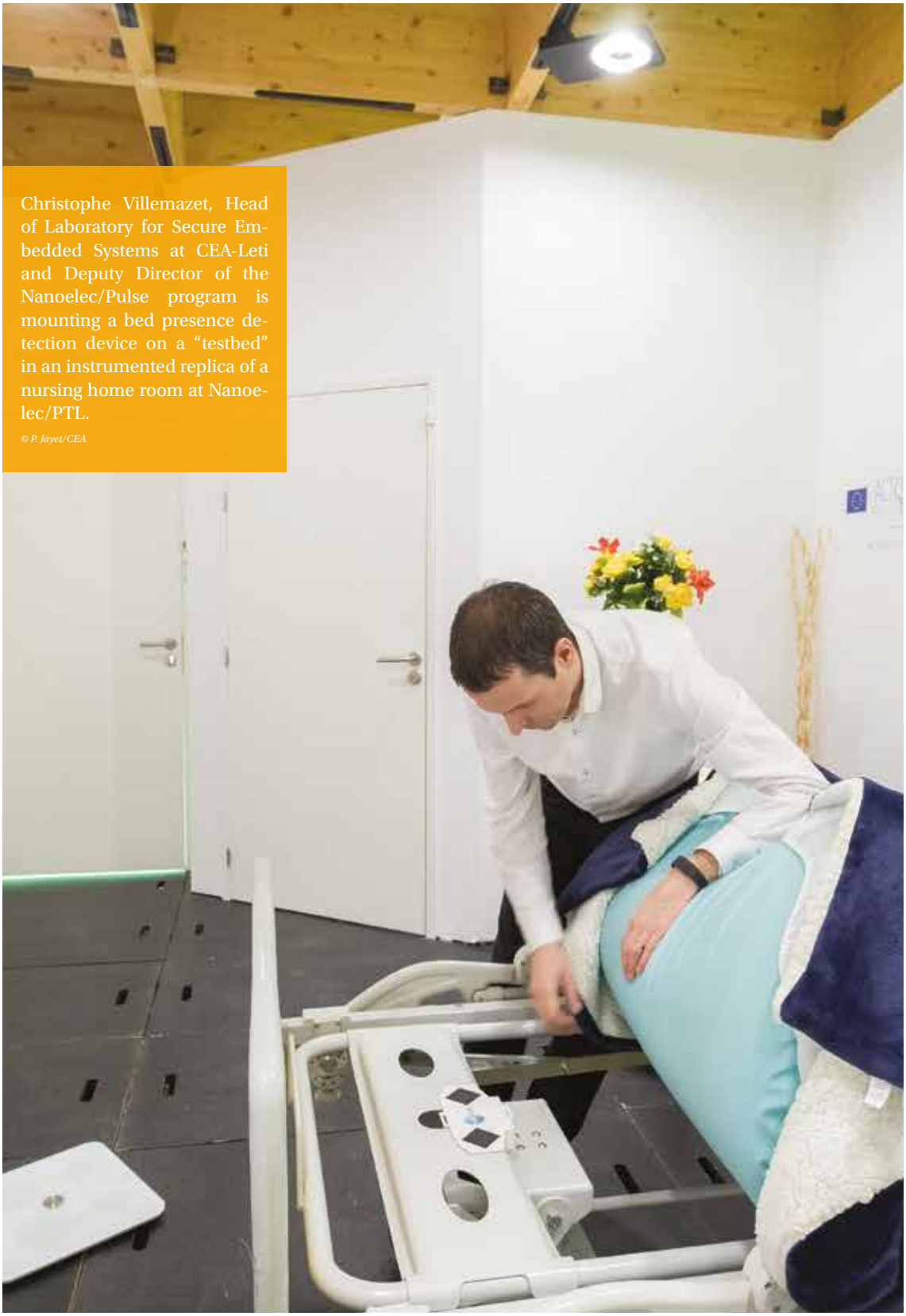
Process isolation is the most important security constraint enforced by operating systems in multitasking systems. *"Isolating memory, in particular, prevents running processes from accessing each other"*, explains Amine Jaamoum, who was recently hired at Thales Digital Identity & Security after having defended his thesis as part of Nanoelec[1]. *"This isolation, however, is not implemented at the hardware level. For example, all processes running on the same CPU eventually share the same caches."* Malware can then manipulate the cache state to derive information about other processes that share the same cache, thus breaking down the isolation that operating systems provide. *"Hence, processor architects must redesign components, and address and effectively mitigate these vulnerabilities for the new generation of processors"*, suggests Amine Jaamoum.

His thesis provides a comprehensive study of the most common cache side-channel attacks. It also provides an overview of ScrambleCache, a novel cache architecture that leverages randomized set placement to thwart the analysis of cache side effects. "A key feature of ScrambleCache is its low impact on performance and its reduced computational overhead," explains Amine Jaamoum. *"This countermeasure protects the system against known cache side-channel attacks while ensuring low costs. The solution is thus well-suited to both embedded and application systems."*

"THESE SOLUTIONS COLLECTIVELY AIM TO ENSURE COMPREHENSIVE PROTECTION ACROSS ALL CACHE LEVELS…"

While ScrambleCache primarily focuses on securing the first-level caches, the thesis also mentions that additional solutions have been proposed for protecting caches in the higher levels of the memory hierarchy. These solutions collectively aim to ensure comprehensive protection across all cache levels, thus fortifying the process isolation in multitasking systems and mitigating the risk of cache-based attacks. •

3. Jaamoum, A. (2022). "Strategies for securing cache memories against software side-channel attacks", Grenoble Alpes University thesis defended on 12/12/2022, and prepared at CEA-Leti as part of Nanoelec.



Christophe Villemazet, Head of Laboratory for Secure Embedded Systems at CEA-Leti and Deputy Director of the Nanoelec/Pulse program is mounting a bed presence detection device on a "testbed" in an instrumented replica of a nursing home room at Nanoelec/PTL.

© P. Jayet/CEA

Home & health cybersecurity

Protecting memory hierarchy against auxiliary-channel attacks

Side-channel attacks have traditionally exploited the vulnerabilities of cryptographic primitives once they were implemented in embedded systems.

The goal has long been to find cryptographic keys — they are difficult to locate when focusing only on the mathematical construction of these algorithms. Several countermeasures have been developed to protect the implementation of cryptographic algorithms from these attacks. Embedded systems, however, store several types of data, which circulate in the memory hierarchy. Just as sensitive as encryption keys, this can include users' personal and confidential data (authentication codes, medical records, etc.).

Ezinam Talaki prepared his thesis at CEA-Leti as part of Nanoelec[4], and defended it in 2022. He focused on side-channel attacks — in particular, first order attacks based on power consumption analysis — and their threats to the memory hierarchy. The characterization of side-channel leakage was able to demonstrate that leaks were exploitable through template attacks. *"This led us to examine and develop a countermeasure to protect the bus and registers as well as the memory hierarchy"*, explains Ezinam Talaki, who was hired at SGS Brightsight after completing his doctorate. Encryption of memory hierarchy is a well-known and applied method, but it entails an overhead in terms of spatial footprint and timing latencies. *"In order to lighten this approach, a solution for fast and lightweight masking of data in cache memory was proposed"*, continues Ezinam Talaki.

"This solution can generate 64-bit masks at each clock cycle and at a frequency of 150 MHz while only having to store an 8-bit random source instead of full masks. Data masking in caches supplements encryption on the bus by avoiding the need to send encrypted data to the caches and by allowing masked execution at the CPU pipeline level."

In the Cryptography journal[5], Eziman Talaki and al. propose a secure and lightweight scheme to ensure data confidentiality throughout the memory hierarchy. *"The advantage of the solution lies in its reduced computational overhead (only two rounds of Subterranean resulting in 400 LUTs after design implementation on FPGA) and the fact that no mask will be stored for further unmasking except the 8-bit IV"*, comments Eziman Talaki.

4. Talaki, E. B. (2022). "A Memory Hierarchy Protected against Auxiliary-Channel Attacks", *Grenoble Alpes University thesis defended on 27/09/2022. [UGA]. https://www.theses.fr/s222744.*

5. Talaki, E. B., Savry, O., Bouvier Des Noes, M., & Hely, D. (2022). A Memory Hierarchy Protected against Side-Channel Attacks. *Cryptography, 6(2), 2. https://doi.org/10.3390/cryptography6020019*

Home & health cybersecurity

2023 RISC-V Summit Europe

Contrary to the world's most common instruction set architectures (ISA)[6], RISC-V is an open-source model[7]. This means that developers can fully access and modify the architecture, and use it for their own applications. CEA teams involved in Nanoelec participate annually at the European RISC-V[8] Summit.

MIKAEL CARMONA, Head of Laboratory for Security of Hardware Components (CEA-Leti), talked to us about the challenges of this technology, poised to become a new standard.

What are the advantages of open-source materials and applications for innovative architecture?

By using an open-source instruction set architecture, or ISA, developers can build end-to-end processors since they have full control over material and application components. There are at least two advantages for innovation: first, it offers myriad possibilities to design new, technologically disruptive processors with high performance and security features. Second, part of the development can be shared with a community well beyond the project's initiator. Sharing ensures faster and consolidated development of technology blocks without having to transfer intellectual property rights. → 66

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Mikael Carmona, Head of Laboratory for Security of Hardware Components (CEA-Leti).

What role does RISC-V play in Nanoelec's digital trust applications?

The goal of the Nanoelec/Pulse program is to make RISC-V ISA processors secure; open source ISAs are a means to ensure that their architecture is intrinsically secure. For processors based on a proprietary ISA, any detected vulnerability is fixed by adding a "patch". This leads to a significant cost increase in surface (silica) and performance (time) due to the need for a solution that will directly modify the core and make it resilient.

How can RISC-V be an alternative to ARM processors, which are ubiquitous in mobile phones and tablets, and even in certain computers?

The RISC-V Foundation foresees over 80 million RISC-V cores in the automobile, IoT, and industrial markets by 2025. In 2022, ROMA, the first RISC-V laptop, arrived on the market, and Android was able to support RISC-V architecture. As a result, RISC-V has become a direct competitor of ARM in an ecosystem which is powerful (Google, IBM, Samsung) and dense (number of markets and company types).

Why is RISC-V not an issue in the trade war between the United States and China?

An ISA is not the only hardware component of a processor. Although there is no current fight for sovereignty over ISAs, the trade war has nevertheless affected electronic components. One of the goals of the Nanoelec/Pulse program is to design and characterize intrinsically secure RISC-V processors, and therefore gain a competitive edge over current security solutions.

What are the highlights of the 2023 RISC-V Summit Europe?

"IN BARCELONA, WE INTRODUCED TWO SECURITY INNOVATIONS FOR RISC-V PROCESSORS"

ScrambleCache is a highly effective technique to secure the cache of application processors. Safeguarding against cache-based attacks means, for example, protecting the data encryption key on a medical device processor to prevent theft of medical data.

The memory encryption engine (MEE) encrypts (confidentiality) and authenticates (integrity) data stored in DRAM (or Flash) memory, which then travels to lower-level caches to be executed by the processor. With an additional cost of only 10% on Linux execution latency and 3% on core area used, this innovation offers consistent protection against DRAMA and Rowhammer attacks, which can alter data stored in non-volatile memory, and render systems unusable.

6. An ISA defines the set of basic operations (representation and address mode of data types, registers, instructions) to execute computer programs (codes) via a processor.

7. RISC-V stands for Reduced Instruction Set Computing Five, meaning it is a simplified (reduced) version of the set of instructions compared with older, more complex architectures. The term "Five" indicates the fifth version of the architecture.

8. The RISC-V Summit Europe https://riscv-europe.org/

Home & health cybersecurity

RISC-V week in 2022

Held on-line by Nanoelec, Inria and CEA, the "RISC-V week" underlined the benefits of hardware and software co-design and open source collaboration.

The fourth edition was held in Paris from May 3 to 5, 2022. Over 200 face-to-face and 40 remote participants took part in the plenary sessions, as well as an exhibition featuring seven stands (SiFive, Codasip, Siemens, Andes Technologies, OpenHW Group, RISC-V Foundation and CEA) and some twenty posters. Nanoelec/PULSE teams presented their work on intrinsically secure application processors.

Nanoelec's Products & Technologies Living-lab at CEA-Leti. This R&D platform helps pioneer new technologies with applications in connected mobility, in-home healthcare and other home services. The goal is to support companies in their development of innovative and secure products and services.

© P. Jayet/CEA

Cybersecurity of industrial systems

Ultra-secure device for critical IoT

SecIoT integrates an enhanced arsenal of hardware and software security features. It simultaneously ensures object authentication and protection of sensitive data in terms of confidentiality and integrity. Implemented security functions leverage both local capacities and off-the-shelf hardware security components to maximize security and performance. Along with management of encryption keys, automatic recovery and quantum threat protection, SecIoT automatically detects when the case is opened in order to prevent reverse engineering. The demonstrator was presented at the 2022 European Cyber Week and at 2023 Leti Innovation Days.

© *CEA*

Detect and prevent malware attacks that target hardware vulnerabilities in IoT/IIoT devices

A CEA and Grenoble INP-UGA study within Nanoelec[9] lists this type of attacks and the side effects that they produce in a system.

"Security mechanisms can be set up to combat certain attacks", declares Nikolaos Polychronou, the study's main author. Most of these mechanisms target a small set of attack vectors or a single specific attack vector. Since there are many attack vectors, it is vital to find solutions for a large number of threats. *"Our study aims to inform designers about the side effects of attacks, and about the detection mechanisms in scientific literature."*

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Classic setup for electromagnetic emanation recording (target being tested is a Cortex M4 32-bit microcontroller).
© *CEA*

9. Polychronou, N., Thevenon, P.-H., Puys, M., & Beroulle, V. (2022). A Comprehensive Survey of Attacks without Physical Access Targeting Hardware Vulnerabilities in IoT/IIoT Devices, and Their Detection.

Cybersecurity of industrial systems

Improving cybersecurity of a critical infrastructure

A hardware-software co-simulation environment is continuously designed and improved to alert the public and professionals about the cybersecurity threat to industrial control systems, and to experiment with innovative security solutions.

© P. Jayet/CEA

The WonderICS platform — hosted at CEA site within Nanoelec — integrates simulators that emulate physical processes for different use cases, such as hazardous gas management or hydroelectric power plants. *"Nowadays, a set of tools can be used to attack industrial control systems in different ways (phishing emails, corrupted USB keys, hardware Trojans, etc.). This platform demonstrates organizational and technical solutions that help prevent these types of attacks"*, comments Maxime Puys, cybersecurity research engineer at CEA, in charge of WonderICS.

Hospital infrastructure

In 2022, the information system of WonderICS was duplicated and adapted to raise awareness of IoT cybersecurity among an industrial audience in a hospital use case. *"Attacks could impact the operation of a healthcare facility, for example, by causing a circuit breaker to be triggered remotely. The idea is to draw a parallel between an installation without security measures and an installation with different security functions"*, explains Maxime Puys.

Education & training

Maxime Puys and colleagues from academic partners of the Nanoelec/PULSE program presented "SCADA Cybersecurity Awareness and Teaching with Hardware-In-The-Loop Platforms", including WonderICS, in the Journal of Wireless Mobile Networks, Ubiquitous Computing, and Dependable Applications[10]. *"We introduced two twin demonstrators based on the same technology: an Advanced Persistent Threat (APT) demonstrator used for awareness training, and a flexible lab used for student training and penetration testing. Both are based on a common Hardware-In-the-Loop technology that combines virtualized devices with real industrial devices"*, reports Maxime Puys. •

"DRAWING A PARALLEL BETWEEN AN INSTALLATION WITHOUT SECURITY MEASURES AND AN INSTALLATION WITH DIFFERENT SECURITY FUNCTIONS "

10. The article is an extended version of a conference paper presented at a workshop on Education, Training and Awareness in Cybersecurity (ETACS'21) held in conjunction with the 16th International Conference on Availability, Reliability and Security (ARES'21).

↑
Post-Quantum Cryptography (PQC) is a field of technological research aiming to guarantee the security of information that could potentially be threatened by quantum computing attacks.
© CEA

Cybersecurity of industrial systems

Towards a global standard for internet confidentiality and embedded systems

Within Nanoelec, researchers from CEA, UGA and STMicroelectronics have published in open source a first level of optimization for the implementation of a community-acclaimed standardized post-quantum algorithm (NIST competition).

The advent of quantum computing could very well make asymmetric cryptography vulnerable. Today, this type of cryptography ensures, among other things, confidential communication on the internet, and integrity of embedded software on critical devices. "*Post-quantum cryptography (PQC)*[11] *will become the standard in the coming years; it will replace current cryptography. The NIST in the United States, the ANSSI in France and the BSI in Germany have initiated the technological and industrial transition of cryptography*", explains Guillaume Goy (UGA and CEA), who is conducting PhD research on the subject as part of Nanoelec.

11. Cryptography aims to ensure data security against quantum-computing attacks.

"Since 2016, the NIST has conducted a selection process for cryptosystems that can resist attacks from quantum and traditional computers[12]*. The goal of the competition-like process is to identify the most secure and effective cryptographic schemes, and to set forth standards by 2024"*, explains Antoine Loiseau, PQC specialist at CEA who oversees the research that CEA and UGA conduct with STMicroelectronics. *"The selections that the NIST has made among research teams all around the world, since 2016 until today, are proof of the difficulty of the task."*

Nanoelec/Pulse program partners have decided to examine one of the standardization approaches selected by the NIST: Hamming Quasi-cyclic (HQC). *"By choosing to work on a specific system, our goal was to improve overall upskilling on PQC, and to obtain concrete results pertaining to a given cryptosystem"*, adds Antoine Loiseau.
Researchers from CEA and UGA (working as part of Nanoelec), and from Limoges University published two articles in 2022[13,14]. The second article was selected for a presentation at the fourth NIST conference.

"In comparison with the state-of-the-art scientific literature review, we have a 40 to 60% better performance rate in terms of computing time, and a 70% smaller memory footprint", declares Guillaume Goy.

The same team carried out an optimized HQC implementation for their embedded system on a STMicroelectronics STM32U5 microcontroller (available on the market), adapted to an embedded device (portable medical device, household appliance, industrial sensor), and including hardware security primitives.

"As a result of these tests, we were able to truly observe the impact of our modifications in comparison with the standard implementation", continues Antoine Loiseau. Conclusion: The Nanoelec implementation offers a much higher optimization level than the scheme's standard implementation.

"Nanoelec helped us to anticipate the future rollout of post-quantum cryptography in our products. We were able to have discussions and to actively collaborate with academic partners from UGA and CEA", adds Bernard Kasser, Company Fellow & SRA Security Roadmap Director at STMicroelectronics.
The research was published in open source so that the entire community could benefit from the performance implementation for an embedded system.

"WE HAVE A 40 TO 60% BETTER PERFORMANCE RATE IN TERMS OF COMPUTING TIME, AND A 70% SMALLER MEMORY FOOTPRINT."

As part of Nanoelec, a CEA team examined the particular pertinence of PQC for the needs of the European Poliiice project launched at the end of 2022. *"We updated technological intelligence pertaining to physical attacks and associated countermeasures for PQC and key quantum exchange"*, explains Mikael Carmona, Head of Laboratory for Security of Hardware Components (CEA-Leti). •

12. *US National Institute of Standard & Technology https://csrc.nist.gov/projects/post-quantum-cryptography*

13. G. Goy and al., Estimating the Strength of Horizontal Correlation Attacks in the Hamming Weight Leakage Model: A Side-Channel Analysis on HQC KEM, WCC 2022.

14. G. Goy and al., A new key recovery side-channel attack on HQC with chosen ciphertext, *PQCrypto 2022.*

Industrial robotics

Digital identity

Individuals can manage their own personal or confidential data on device-centric or user-centric system architectures. How to create trust so that stakeholders of a given ecosystem can work together, while protecting their own interests and business activities?

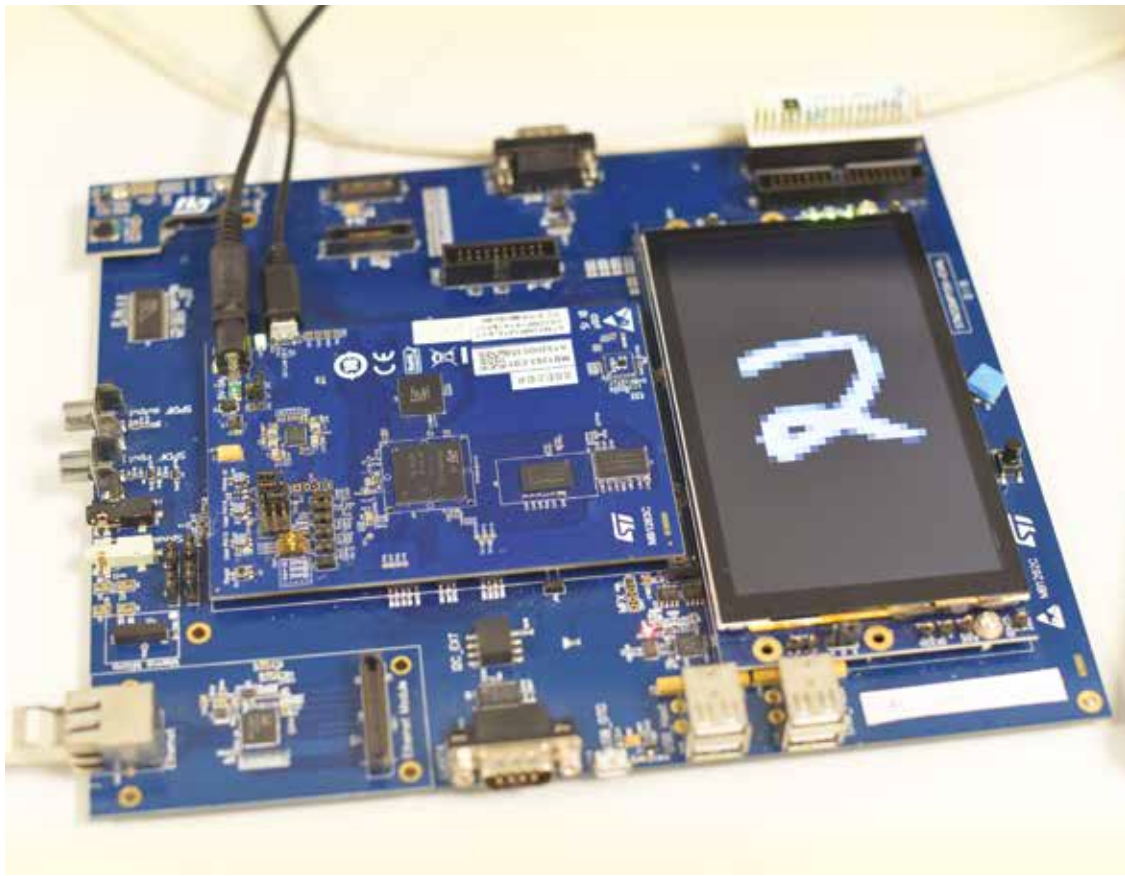
In 2021, as part of Nanoelec, CEA-Leti developed the HistoTrust blockchain[15] demonstrator. It provides a solution to the problem: a system architecture in which each stakeholder handles their own confidential data, and shares cryptographic proof of the data's origin, timestamp, order and integrity in an Ethereum blockchain ledger. The robust solution is meant to be resilient against malware attacks, and to provide a high level of protection against physical fault injection and side-channel attacks. Furthermore, the integration of security measures does not affect operational performance, thus respecting the real-time constraints of an embedded industrial application.

"In 2022, the demonstrator was refined: integration of a neural network in the ARM Cortex M4 microcontroller on the System-on-Module (SoM) of the STMicroelectronics STM32MP157C-EV1 evaluation board", explains Christine Hennebert (CEA-Leti), who supervises blockchain-oriented topics for digital trust as part of the Nanoelec/Pulse program.

Increasingly integrated into automated industrial systems, artificial intelligence uses image analysis to automate certain decisions; this has an impact on control-command systems. Artificial intelligence, however, is merely computer code: reproducibility of decisions is not always guaranteed, and this raises issues concerning the responsibility of formulated decisions. HistoTrust aims to track and attest the decisions made by the embedded neural network, as well as the actions carried out by individuals, in a decentralized ledger. The origin of a problem can thus be understood in the event that production comes to a halt.

In 2022, in addition to HistoTrust, a new demonstrator, named TrustMe, was designed to enhance the value of a decentralized Digital Identity Wallet, which aims to prevent identity theft of personnel working on the industrial system. It also ensures the anonymity of physical individuals in the digital system and data confidentiality.

15. Blockchain technology is used to store and exchange information in a decentralized and secure manner. It consists of a network of interconnected computers that store and validate transactions with transparency and immutability. The distinctive feature of blockchain is its public and shared ledger in which all network transactions are recorded. This ensures traceable and transparent exchanges, and prevents fraudulent alterations of recorded data.



↑
The HistoTrust solution aims to be resilient and robust against malware attacks, and to provide a high level of protection against side-channel and fault injection attacks. © *CEA*

Few solutions operate on public blockchains, in which everyone has access to the registry. This presents many challenges. At present, there is no decentralized public or private identity provider. The need for regulations in this field is evident. *"Nanoelec develops technological solutions to address these challenges. Its Digital Identity Wallet, based on secure and embedded hardware components in mobile and/or IoT devices, operates on public blockchains based on an Ethereum protocol"*, explains Christine Hennebert.

Ethereum is an open-source technology that is gradually becoming a global standard. *"The designer of the Ethereum public blockchain, Vitalik Buterin, sees the possibility of using it to execute smart contract code. Ethereum also enables the construction of permissioned blockchains by cloning the open-source depository, and it provides an emulator"*, continues Christine Hennebert. "*These tools enable the construction of proofs of concept by gradually increasing the maturity level of our demonstrators (TRL), and without the need for cryptocurrency."* •

"THE INTEGRATION OF SECURITY MEASURES DOES NOT AFFECT OPERATIONAL PERFORMANCE, THUS RESPECTING THE REAL-TIME CONSTRAINTS OF AN EMBEDDED INDUSTRIAL APPLICATION."

Industrial robotics

Validating automotive software with augmented reality

A collision-avoidance driver assistant on augmented reality on Lidar data was developed and tested.

Testing and validating advanced automotive software are of paramount importance to guarantee safety and quality.

"Real-world testing is highly demanding, and simulation testing is not reliable", notes Thomas Genevois (Inria). *"That is why we propose*[16] *a new augmented reality framework that takes advantage of both environments."*
This new testing methodology is intended to be a bridge between Vehicle-in-the-Loop and real-world testing. It makes it possible to easily and safely place the whole vehicle and all its software, from perception to control, in realistic test conditions.

16. Best Paper award for the article pertaining to the 2022 IEEE Intelligent Vehicles Symposium (June 5-9, 2022. Aachen), Germany, Genevois, T., Horel, J.-B., Renzaglia, A., & Laugier, C. (2022). CONF + ART | AWARD: Augmented Reality on LiDAR data: Going beyond Vehicle-in-the-Loop for Automotive Software Validation. *2022 IEEE Intelligent Vehicles Symposium (IV), 971 976.*

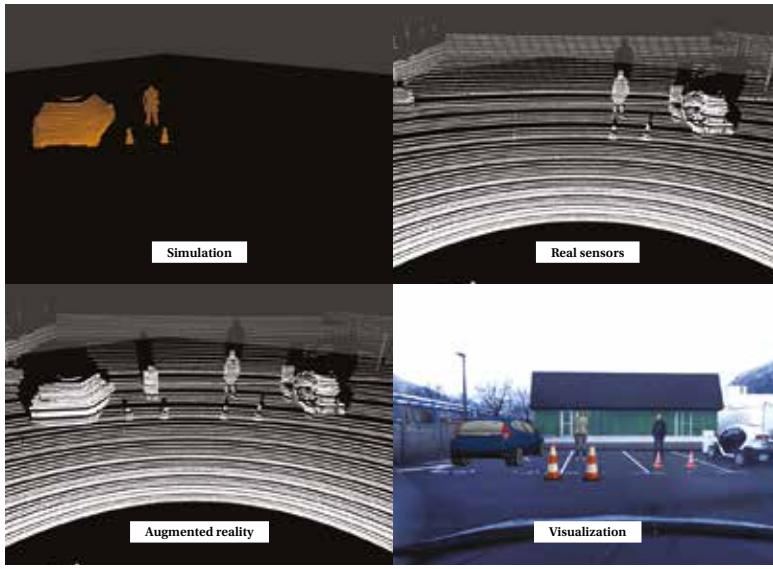
↑
Best Paper Award at the IV22 conference.

"This framework provides a flexible way to introduce any virtual element in sensor outputs of the vehicle being tested", underlines Thomas Genevois. *"For each sensor modality, the framework requires a real-time augmentation function that preserves real sensor data and enhances them with virtual data."*
The team from Inria, UGA and Insa-Lyon studied the Lidar data augmentation function and its implementation details. Relying on both qualitative and quantitative analysis of experimental results, the representability of test scenes generated by the augmented reality framework was finally proven.

"*We developed and tested in augmented reality (AR) a collision-avoidance driver assistant on our prototype, the Renault Zoé Inria/Nanoelec, in the environment of the Product & Technologies Living Lab R&D platform (Nanoelec/PTL)"*, Thomas Genevois adds.

Future developments include the ability to augment other sensors, the design of test actors reacting to the vehicle and the contextual automated generation of critical test scenarios. •

↑
Thomas Genevois (Inria) giving his talk at the IV22 conference. © *DR*



Example of LiDAR point cloud augmentation: The introduced virtual point cloud and initial sensor point cloud are shown at the top. Deployed on a vehicle, the technique generated the fused point cloud and the visualization of the augmented scene (bottom). The augmented environment may be used to safely evaluate the performance of complex automotive software such as AI-based solutions. It also helps to compare simulation and reality in order to assess accuracy of simulation tools.

Industrial robotics

Developing the senses of self-driving cars

Research carried out in 2022, as part of Nanoelec, under the leadership of Inria, and resulted in the final software and hardware development of a demonstrator: an industrial automated material handling system equipped with sensors and an embedded automated perception and navigation system. The demonstrator was validated in hardware-in-the-loop simulation.

Developments also continued on the Zoe/Inria-Nanoelec self-driving car, in connection with projects that involved Toyota and Sumitomo Electric. A prototype of semantic occupancy grid filtering system was assessed and stabilized, and an augmented-reality navigation platform to test self-driving cars in a densely-populated urban area was designed and experimented with. The development of V2X communication tools, which fuse perception between the car and a realistic, perceptive and communicative infrastructure has been also studied.

The new self-driving car demonstrator of Embedded Bayesian perception and navigation, developed by Inria as part of Nanoelec, was presented at the World Electronics Forum in Grenoble, in October 2022.

↑
Zoe demonstrator of embedded Bayesian Perception and Navigation, at the World Electronics Forum in Grenoble, in October 2022. © *DR*

Industrial robotics

Nanoelec, System X and mobility partners

The Prissma project is the response proposed by the autonomous mobility sector to Pillar 2 issued by the Grand Défi in partnership with the French Ministry of Ecological Transition and Solidarity, on the securing, the reliability, and eventually the certification of AI-based systems.

This project aims at proposing a platform that will allow to lift the technological barriers preventing the deployment of secure AI-based systems, and to integrate all the elements necessary for the realization of the certification activities of the autonomous vehicle and its validation in its environment for a given use case. Two main use cases are focused on, namely shuttles and automated robots (Droids).

"TWO MAIN USE CASES ARE FOCUSED ON, NAMELY SHUTTLES AND AUTOMATED ROBOTS (DROIDS)."

The project includes 21 stakeholders, including SystemX IRT and most important smart-mobility French agents. Nanoelec participates in conjunction with CEA and Inria involvement. In this context, Nanoelec Zoe demonstrator of embedded Bayesian perception and navigation, and augmented-reality experimentation tools, have been interconnected to the developed Prissma validation tools, and experimented with at the Transpolis test center for innovation and security (Auvergne-Rhône-Alpes region, France), allowing for large-scale, densely-crowded scenarios.

↑
Zoe demonstrator of embedded Bayesian Perception and Navigation, using Augmented-Reality to experiment with large-scale, densely-crowded environments, at Transpolis. © *Inria*

Industrial robotics

Digitalizing products and services for SMEs

From January 2020 to March 2023, Isabelle Chartier (CEA-Leti) coordinated Digifed, a project developed in conjunction with IRT Nanoelec, and funded by the European Commission. This is her take on a collective experience that included twelve partners and cascade funding schemes.

Is Digifed somewhat similar to Nanoelec/Easytech, but at a European level and with the goal to foster cross-border collaborations?

Yes, it is similar in the sense that we champion small projects: we have provided support for SMEs with a maximum budget of €70,000 to develop a demonstrator within a year or more. Projects must be developed with a partner from another country (cross-border collaboration): another SME, or a Digifed partner contributing a technological block.
Projects covered a wide range of fields: automation of pollen analyses for honey producers (Spain/Greece), optimization of dental implants (Spain/Romania), and electric vehicle chargers (Slovakia/Czech Republic).

What operational contributions did IRT Nanoelec bring to Digifed?

Digifed is made up of twelve partners, three of which are Nanoelec consortium members: Minalogic provided innovation/management assistance; as digitalization often entails changes in a company's business model. CEA-Leti and STMicroelectronics contributed their technical expertise, particularly a kit of ready-to-use and secure blocks for SMEs: a secure gateway[17] based on secure STMicroelectronics components (STM32MP1).

Why is digital trust the project's main focus area?

We have supported projects for companies that specialize in data security and communication (CYSEC in Switzerland), others in agrifood industry logistics (NGS in Italy) — security is important for the legal aspects of cold chain control — and others in healthcare (Panoramic Digital Health in France), all of which require digital trust for data confidentiality and integrity.

Thanks to Digifed we have also initiated a novel collaboration mode called Generic Experiment. Its goal is to rally a SME community around a research center in order to enhance mutual knowledge and initiate future collaborations. CEA and STMicroelectronics led a community discussion on cybersecurity with a focus on secure gateway design standards. Y.Spot initially led the group to define common objectives. Technical developments — co-funded by the Easy-poc program and the Auvergne-Rhône-Alpes region — helped to set up algorithms that detect intrusions and cyberattacks. Five SME community members were able to test the prototype.

↑
At Nanoelec's General Assembly in December 2022, Isabelle Chartier (CEA-Leti) gave an overview of Digifed, a European project that she coordinated from 2020 to 2023.

© C.Tresca/CEA

17. https://digifed.org/news-events/success-stories/segway-cysec/

↑
The international experts gathered to animate the EU DigiFed projet dedicated to SMEs digitalization. © *Digifed*

Why did Digifed make cross-border collaboration a priority?

There are many funding opportunities for French SMEs that want to work with a French research center. It is much more difficult for an Irish SME, for example.
We therefore focused on small consortiums with two SMEs from different countries. Our idea was greatly appreciated; companies made joint progress. It also fostered collaborations between mid caps and big groups, which otherwise would not have obtained funding. In addition, we funded a consortium between an SME and a large group via a new tool called Digital Challenge.

Has the European Commission recognized your approach?

Yes. DigiFed followed three cascade funding projects (EuroCPS, GateOne and FED4SAE) which ensured upskilling and the optimization of funding processes for SMEs. In 2023, as part of Nanoelec, CEA-Leti was selected to coordinate a new project called Earashi[18]: a new cascade funding mechanism that aims to improve the security of individuals in the workplace by using robotics and artificial intelligence. •

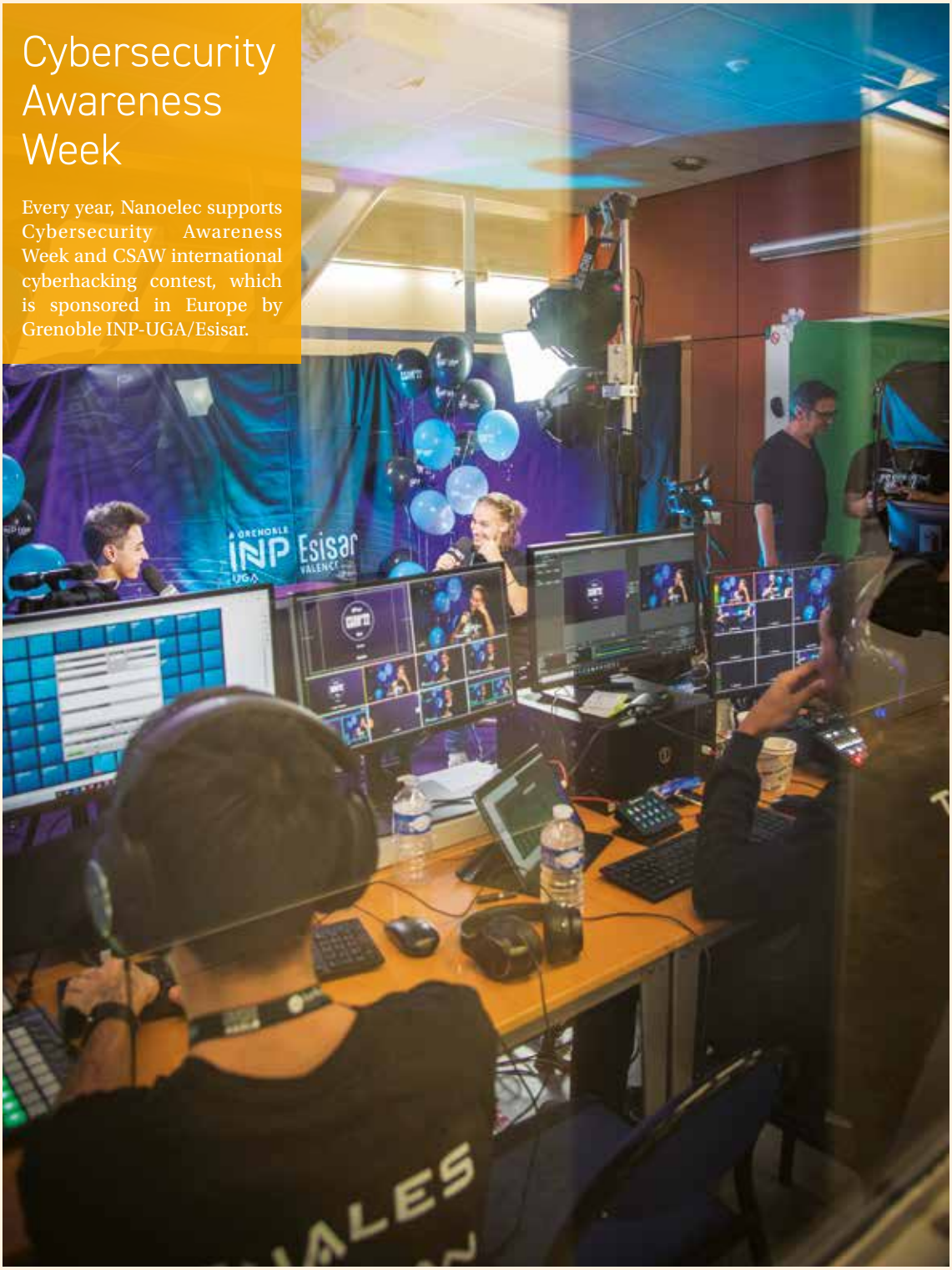
"EARASHI IS A NEW CASCADE FUNDING MECHANISM THAT AIMS TO IMPROVE THE SECURITY OF INDIVIDUALS IN THE WORKPLACE BY USING ROBOTICS AND ARTIFICIAL INTELLIGENCE. "

18. https://earashi.eu/open-calls/

Events

Cybersecurity Awareness Week

Every year, Nanoelec supports Cybersecurity Awareness Week and CSAW international cyberhacking contest, which is sponsored in Europe by Grenoble INP-UGA/Esisar.



European Cyber Week

European Cyber Week (ECW) is a European-scale must-attend event that focuses on strategic fields such as cyber defense, cybersecurity and artificial intelligence. It also offers relaxed, high-quality and efficient networking opportunities for participants, opinion leaders and companies. ECW 2022, the event's seventh edition, was held in Rennes in November 15 17, 2022.
The Nanoelec/PULSE program presented its research on intrinsically secure application processors and on the security of IoT devices.

© DR

Events

International Cybersecurity Forum

The International Cybersecurity Forum (FIC) is a major event in Europe for security and digital trust. The event's 14th edition was held in Lille in June 7-9, 2022, with more than 19,000 participants from 60 countries, and 520 speakers. Two of the event's masterclasses — Detection of Intrusions in Industrial Systems and The Resilience of Post-Quantum Cryptography to Physical Attacks — were presented by Nanoelec/Pulse members.

A robot car painted in Picasso-like style, climbing the Chartreuse Mountains.

© created with Open AI/Dall.e

Would your cat be authorized to drive an autonomous vehicle?

© created with Open AI/Dall.e

CHARACTERIZATION

↗
Ennio Capria, Deputy Head of Business Development at ESRF and Director of the Nanoelec Characterization program

© P.Jayet/CEA

Easy access to large scale instruments for characterization

CHARACTERIZATION PROGRAM AT A GLANCE

→ Vision

The unmatched performance of large-scale instruments must be identified by industrial users as a cutting-edge tool to perform advanced characterizations of electronic components and devices.

→ Ambition

Develop a competence center for testing radiation hardness of electronic components.

→ Mission

Continue to make unique scientific instruments & methodologies available to meet the new challenges of the electronics industry for the serenity and sovereignty of the digital transition.

→ Partners

CEA, CNRS/LPSC, ESRF, ILL, Schneider Electric, Soitec, STMicroelectronics, Iroc Technologies

Mapping both crystalline and electronic defects in materials has been demonstrated at the ESRF BM05 beamline.

© P.Jayet

Nanoelec's Characterization program is part of the institute's digital trust offering for the serenity and sovereignty of the digital transition. Ennio Capria, Program Director, sheds light on the issues of 2022.

Through the Nanoelec Characterization program, industrial firms and researchers have access to top-notch tools to assess the quality of their products and processes and study the effects of ionizing radiation on components and systems. Thanks to the high penetrating power of neutrons and X-rays, these evaluations can be performed non-destructively, without the need for opening or damaging the objects, and in many cases maintaining its functionality.

The year 2022 brought a renewed and revitalized commitment from the program partners. They are undertaking extensive and diverse research and development efforts focused on radiation hardness testing for electronic components, failure analysis and advanced physical-chemical characterization. Notably, this year marked the first dedicated utilization of correlative microscopy, employed to explore different substrate families. Since 2022, the teams involved in the Characterization program have been heavily engaged in three European projects related to nanotechnologies and the irradiation of electronic components.

In 2022, the activity of the CEA team participating in the Nanoelec Characterization program was concentrated on preparing and executing a multi-scale correlative analysis project for detailed inspections of semiconductor materials. In collaboration with an industrial partner of the program, they developed a workflow to analyze some unique characteristics of crystalline defects in SiC, ranging from the scale of the wafer to sub-micrometric lateral resolution. In parallel, at the ESRF, two different teams, in collaboration with two innovating SMEs and the partners of the program, pursued some further development of correlative microscopy methods. An XRD/Raman correlative microscopy station has been installed on the ESRF/ID01 beamline, and on BM05, an instrument capable of mapping both crystalline and electronic defects in materials has been successfully implemented.

—

Characterization becomes correlative

A new instrument capable of performing correlative analyses between XBIC (X-ray Beam Induced Current) and topography was deployed in 2022 on the ESRF BM05 beamline. Fabien Lafont, research engineer at ESRF, is thus overseeing the development of a test bench to characterize semiconductors[1].

You are developing a test bench to characterize semiconductors, more particularly on diamond substrates. Why?

Diamond is a semiconductor on which we are working extensively because one of our project partners has a particular interest in medical applications on this semiconductor, but this potentially applies to any other type of semiconductor.
One of our primary interests is to be able to show that we are capable of obtaining very high quality crystals, for example to monitor ion beams or proton beams, which will be dedicated to treating cancerous tumors in the medical sector.

What technique are you using?

We are adapting the technique called XBIC (X-Ray Beam Induced Current) to synchrotron radiation. This technique has been around for many years and aims to characterize electronic properties, notably of semiconductor crystals2.
However, it is not readily available because of the large streams of X-rays needed, such as those provided by synchrotrons. We therefore intend to provide the Nanoelec Characterization program with a permanent test bench which will subsequently facilitate a large number of studies.

What is your experimental approach?

We study diamond wafers of about five by five millimeters. To be able to use this technique, we metallize the faces of the semiconductor and mount the sample on a printed circuit which will enable us to make the electrical connections of the surfaces we metallized.
On our test bench, we use a very fine X-ray beam of about ten microns, produced by synchrotron radiation. With this, we scan the entire surface of the semiconductor, which enables us to produce 2-dimensional maps of the electronic response to excitation by the X-rays.

On the ESRF BM05 beamline, you correlate XBIC with another technique. Which one?

BM05, which is one of the IRT Nanoelec tools at the ESRF, already had a Bragg diffraction[3] imaging tool. By coupling this tool with our XBIC bench, we can look for correlations between defects in the crystalline properties of the material and those of its localized electronic properties.

↑
Fabien Lafont, research engineer at the ESRF, for the Nanoelec Characterization program. © *Cédrine Tresca/CEA*

1. Within Nanoelec, with four partners: CNRS/LPSC, the Institut Néel, the Institut Laue-Langevin and the ESRF.

2. XBIC: when an X-ray beam passes through matter, it creates charges inside the irradiated material. By applying a potential difference to electrodes mounted on the semiconductor, it is possible to derive these charges and induce currents. By means of high-precision electrometers, accurate measurement of these currents provides information on defects in the crystalline lattice of the material studied.

3. Rocking Curve Imaging (RCI) is a characterization technique used in materials science and semiconductor physics to study the crystallographic properties of thin films and crystal surfaces. Often used in the semiconductor industry, it is a powerful technique for non-destructive imaging of crystal defects, strain, and lattice distortions in semiconductors and other crystalline materials.

Manon Letiche preparing a sample for irradiation experiments on the new Nanoelec neutron beamline called TENIS, at the ILL. As a physicist, she runs most of the Nanoelec experiments on the ILL facility. She is also heavily involved in training courses for PhD students at Grenoble-Alpes University.

© P.Jayet/CEA

The test bench was installed in April 2022. Is it operational?

With this approach we have already demonstrated the overall operation on various crystals. Last October, we produced our first maps on different types of diamonds: a diamond which was grown on an iridium substrate, a CVD diamond irradiated by a proton beam and a diamond obtained by a high-pressure, high-temperature process. Some things still need to be improved, notably more precise interpretation of the maps, using correlation to access the physics of the defects we are looking for.

The test bench will be open to industry in 2023. What will the applications be?

The aim is to understand what is the cause of the localized electronic defects, because what interests us is to obtain semiconductors that are as uniform as possible or free of defects. The applications can vary widely (biomedical, automotive, aerospace, energy, for detectors, power components, and so on). The diamond is a crystal particularly well-suited to the fabrication of detectors, notably for proton therapy. •

4. Chemical vapor deposition (CVD) is a deposition process using chemical evaporation. It produces layers with low stress owing to a thermally induced chemical reaction.

Thermal and Epi-thermal Neutron Irradiation Station

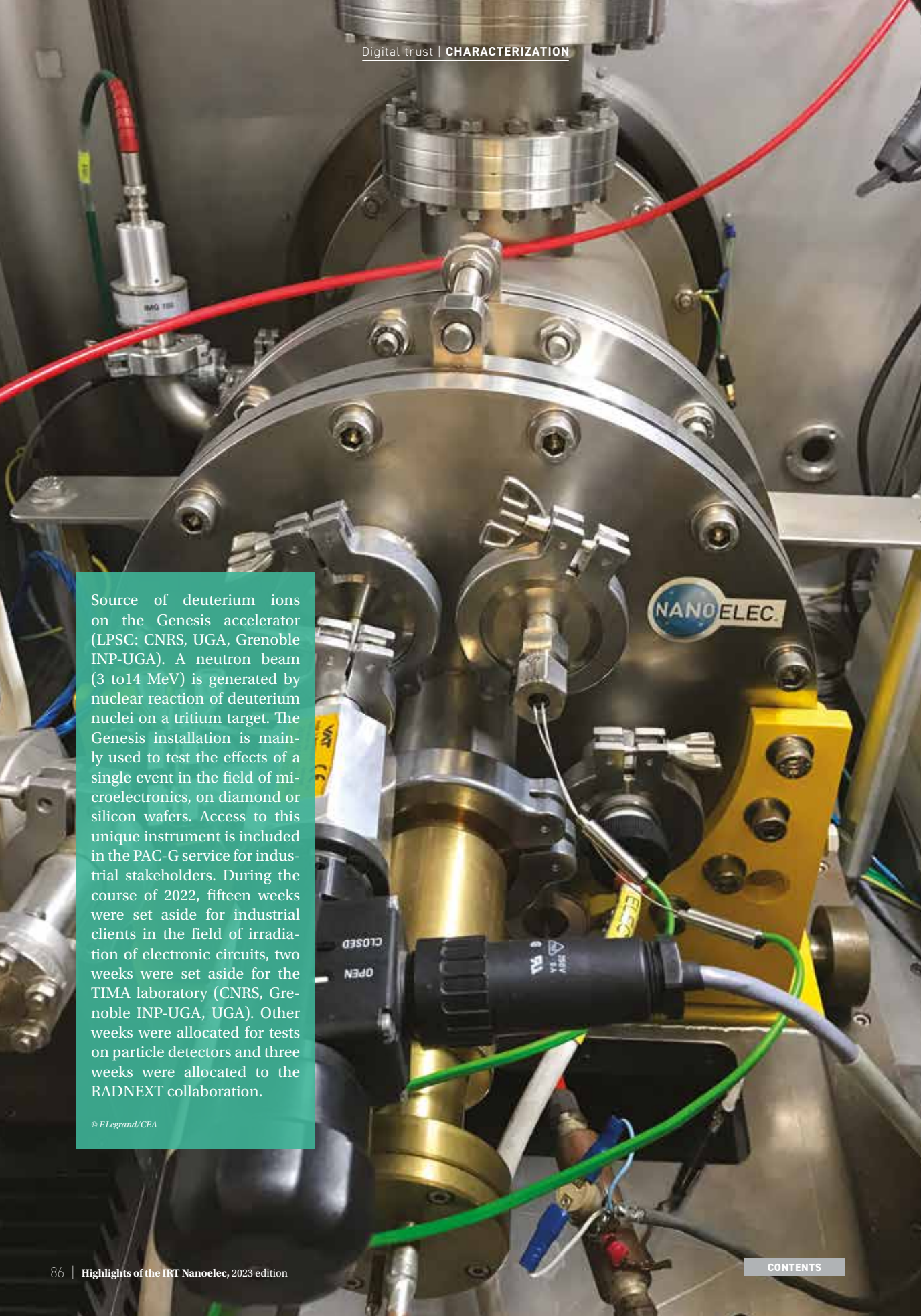
The opening of the TENIS characterization line in 2021 has already generated a large number of publications and event participations.

Among the studies recently conducted at TENIS, the reliability of Google's Coral tensor processing units (TPUs) was investigated with both high energy atmospheric neutrons (at ChipIR) and thermal neutrons from a pulsed source (ISIS spallation neutron source of the Rutherford Appleton Laboratory (RAL), U.K.) and from a continuous reactor flux (at ILL/TENIS). *"The vast majority of errors are not critical for the neural network execution, which is strictly related to the fault model observed for convolutions. Finally, the TPU seems more prone to corruption by high energy neutrons than by thermal neutrons"*, points out Rubens Luiz Rech Junior, as first author of the study published in IEEE Transactions on Nuclear Science[7]. •

5. Thermal and Epi-thermal Neutron Irradiation Station (TENIS) at the Institut Laue-Langevin (ILL) operated under the Nanoelec Characterization program and available through PAC-G services and transnational access via the RADNEXT project.

6. Google Tensor Processing Units (TPUs) are specialized hardware accelerators designed by Google specifically for machine learning workloads.

7. Rech Junior, R. L., Malde, S., Cazzaniga, C., Kastriotou, M., Letiche, M., Frost, C., & Rech, P. (2022). REVUE | High Energy and Thermal Neutron Sensitivity of Google Tensor Processing Units. *IEEE Transactions on Nuclear Science, 69(3), 567-575. https://doi.org/10.1109/TNS.2022.3142092*



Source of deuterium ions on the Genesis accelerator (LPSC: CNRS, UGA, Grenoble INP-UGA). A neutron beam (3 to14 MeV) is generated by nuclear reaction of deuterium nuclei on a tritium target. The Genesis installation is mainly used to test the effects of a single event in the field of microelectronics, on diamond or silicon wafers. Access to this unique instrument is included in the PAC-G service for industrial stakeholders. During the course of 2022, fifteen weeks were set aside for industrial clients in the field of irradiation of electronic circuits, two weeks were set aside for the TIMA laboratory (CNRS, Grenoble INP-UGA, UGA). Other weeks were allocated for tests on particle detectors and three weeks were allocated to the RADNEXT collaboration.

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Platform for advanced Characterization | PAC-G

A gateway to large-scale instruments dedicated to electronics industry needs

PAC-G is a dedicated gateway giving the electronics industry quick and easy access to some of the world's most advanced characterization facilities.

PAC-G also provides an extremely broad portfolio of individual, but complementary characterization techniques. *"We are unique, offering a single point of access to large-scale facilities such as synchrotron and neutron-based sources through a cost-effective and rapid service tailored to innovation in electronics",* says Caroline Boudou (ILL), senior scientist in charge of Nanoelec projects at the ILL. •

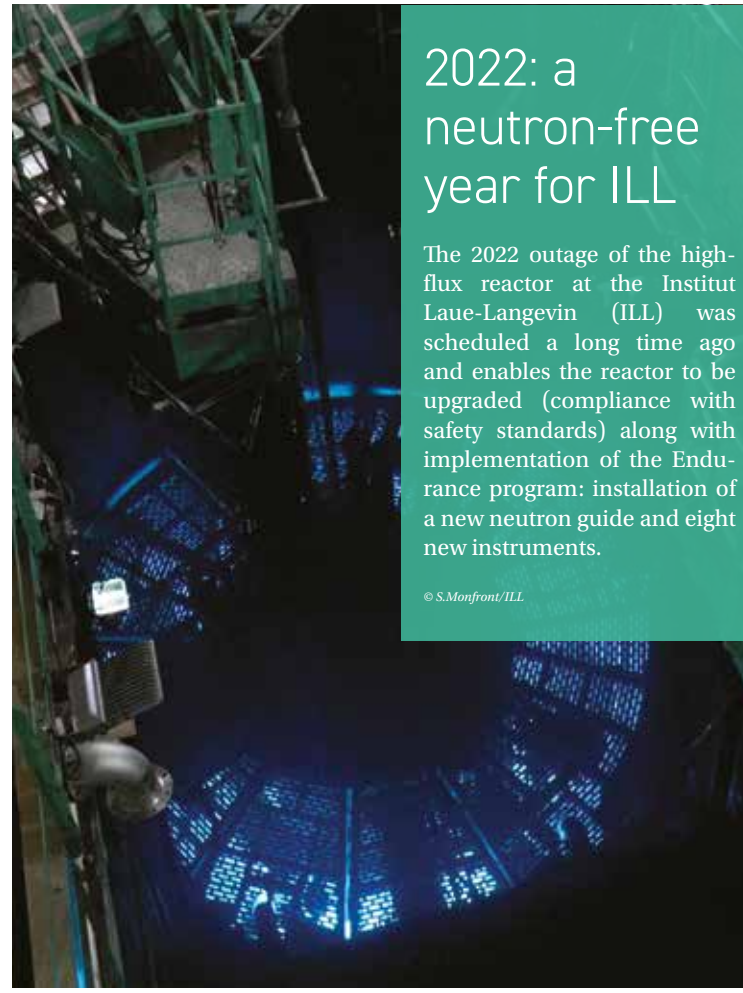
↑
PAC-G provides a single point of access to large-scale facilities such as synchrotron and neutron-based sources through a cost-effective and rapid service tailored to innovation in electronics.
© P.Jayet/CEA

Platform for Advanced Characterization | PAC-G

Carac 2022

Prepared by Nanoelec Characterization , in collaboration with the Institut Néel-CNRS, the Consortium of Common Technological Resources CMTC-INPG and the Grenoble Institute of Interdisciplinary Research (IRIG), the CARAC 2022 seminar was held last November in a hybrid format (face-to-face and remote).

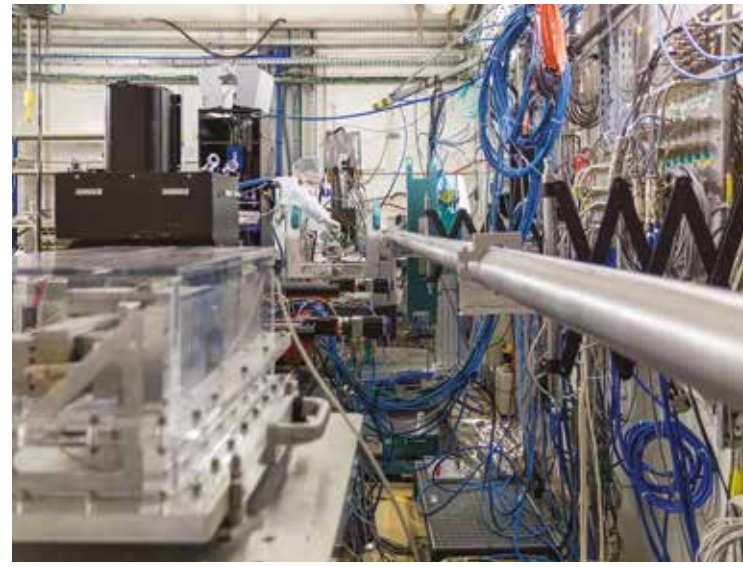
Four papers highlighting the progress made on the large research infrastructures for management of the large volume of data generated, from acquisition to processing of data, were proposed, followed by a visit to the characterization resources of several laboratories in Grenoble. •



2022: a neutron-free year for ILL

The 2022 outage of the high-flux reactor at the Institut Laue-Langevin (ILL) was scheduled a long time ago and enables the reactor to be upgraded (compliance with safety standards) along with implementation of the Endurance program: installation of a new neutron guide and eight new instruments.

© S.Monfront/ILL



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As ESRF/BM05 beamline manager, Phil Cook is checking an X-ray mirror focusing the synchrotron beam on the sample to be analyzed. This beamline is a key component of the Nanoelec/ Carac program. In 2022, it received an additional permanent setup for correlation mapping of topography and XBIC.

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Irradiation

Radiation Facilities and Testing of Semiconductor Devices and Systems for Industry

On May 4, 2022 the G-RAD(NEXT) workshop was dedicated to radiation facilities and the testing of semiconductor devices and systems for industry.

Supported by Nanoelec and other partners, this one-day event was held via a digital platform by the ESRF and CERN. It attracted between 60 and 80 industrial and academic experts. *"Our goal was to increase the level of engagement of industry with the members of the RADNEXT consortium*[8]*, with growth of the industrial quota for transnational access and proprietary/confidential access (when needed). Our aim is to better serve the industrial community, and in this way to create value for European Industry and increase the socio-economic impact of RADNEXT"*, explains Rubén García Alía, Scientific Coordinator of RADNEXT.

Three G-RAD(NEXT) technical sessions were organized around the main applications in the field of irradiation effects on electronics: Space, Aeronautics and Ground Level applications. In each session, a representative of the industrial stakeholder group reviewed the main challenges and prospects. Then, the most appropriate RADNEXT facilities to meet the needs of the user community were described.

8. RADNEXT is an H2020 INFRAIA-02-2020 infrastructure project with the objective of creating a network of facilities and related irradiation methodology for responding to the emerging needs of electronic components and system irradiation; as well as combining different irradiation and simulation techniques for optimizing radiation hardness assurance for systems, focusing on the related risk assessment.

Radiation and its effects on components and systems

Thermal neutrons are an important contributor to any radiation environment where spallation reactions are involved.

This is the case of the atmosphere (ground level to flight altitudes) as well as of high-energy physics accelerators, nuclear fusion and medical facilities. A paper presented at the Radecs international conference on "radiation and its effects on components and systems"[9], explores the possibility that thermal neutron upsets[10] in deep sub-micron SRAMs may not only be caused by boron contaminants or dopants, but also by the nitrogen employed in the manufacturing of the BEOL[11]. *"Thermal neutron Single Event Upset (SEU) measurements combined with construction*

→ 90

9. Radecs, the annual international conference on "radiation and its effects on components and systems" took place in Italy (Oct. 3-7, 2022). Several studies presented involved teams engaged in the Nanoelec Characterization program.

10. Single event upset (SEU) in a component induces software errors.

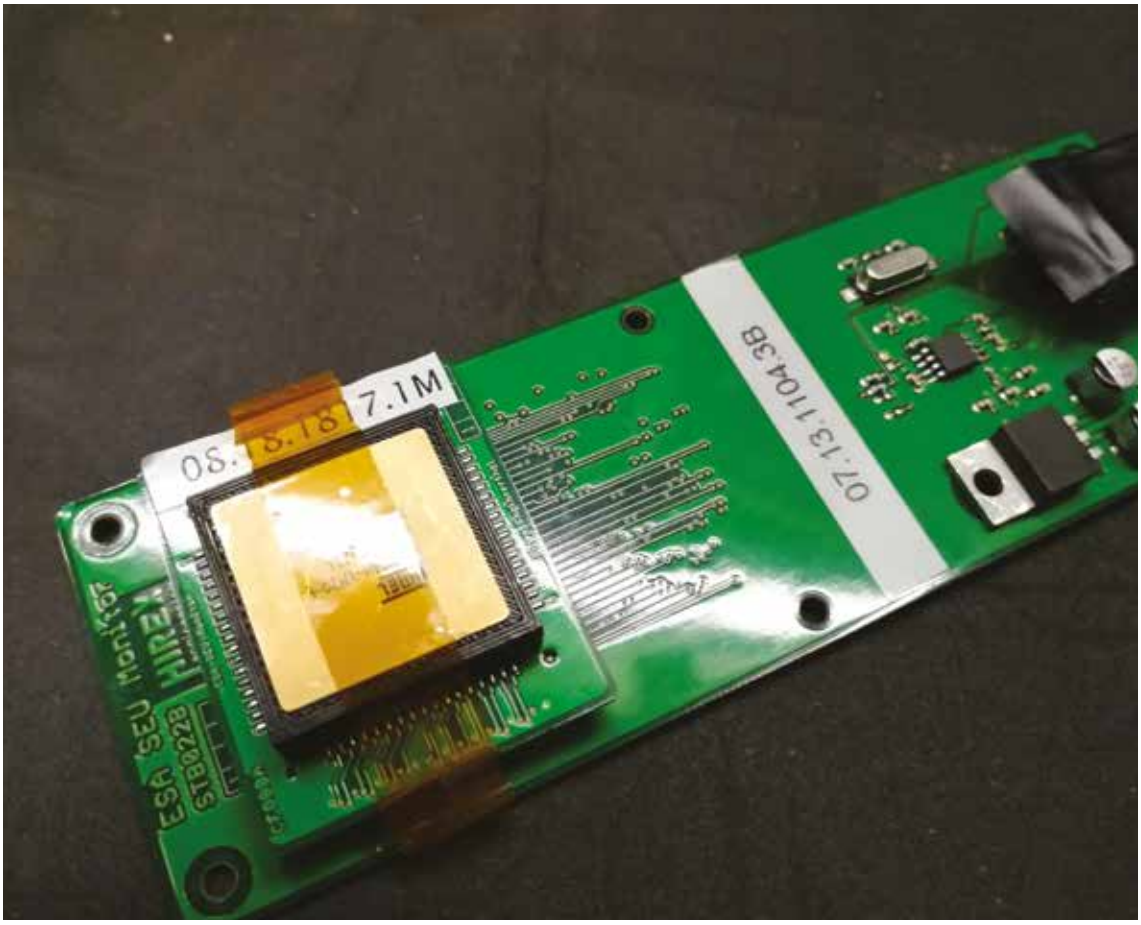
11. In this particular case, the BEOL (Back end of line) is the metallization layer that gives access to the contacts (drain, source) of a transistor as well as control of the transistor contact (gate).

analysis and Monte-Carlo simulation suggest that SEUs from thermal neutron interaction with nitrogen in the memory over-layers may cause SEUs in devices sensitive to low energy protons", explains Andrea Coronetti (Cern) as the first author[12]. "Thermal neutron testing for this study was conducted at the ILL D50 facility operated under Nanoelec, where high fluxes of thermal neutrons (10^9 n/cm2/s) are obtained by cooling down the fast neutrons emitted by the nuclear reactor."

Earlier, another paper from Coronetti et al.[13] reports on the testing of several commercial SRAMs under thermal-to-high-energy neutrons. The tests were initiated for the needs of the electronic equipment of the Large Hadron Collider (Cern). *"Parts of the study were conducted at ILL D50 and the early testing set-up of the future Tenis instruments under the Nanoelec Characterization program"*, says Manon Letiche, one of the authors and an engineer on the Tenis ILL instrument. "*We studied failures in time (FIT) on the studied devices for atmospheric and ground applications as well as predictions for the Cern accelerator soft error rates."* •

12. Coronetti, A., Alia, R., Lucsanyi, D., Letiche, M., & Saigne, F. (s. d.). CONF + ART | An analysis of the criticality of the 14N(n,p)14C reaction for single-event upsets induced by thermal neutrons in *SRAM. RADECS. https://www.radecs2022.org/*

13. Coronetti, A., Alía, R. G., Letiche, M., Cazzaniga, C., Kastriotou, M., Cecchetto, M., Bilko, K., Martìn-Holgado, P., & Letiche, M. (2021). CONF + ART | Thermal-to-high-energy neutron SEU characterization of commercial SRAMs. 2021 IEEE Radiation Effects Data Workshop (REDW), *1-5. https://doi.org/10.1109/NSREC45046.2021.9679344.*



↑
SRAM commercial memory set-up on a connecting PCB ready for irradiation on the ILL D50 beamline. ©*CERN*

Luca Capasso is positioning a reference sample on the Nanoelec giant goniometer on the ESRF/BM05 beamline.

© P.Jayet/CEA

↗
Setup at the ESRF ID09 beamline. *© ESRF*

Irradiation

Inducing single events in the components

The particularity of the ESRF/ID09 beamline is its ability to select isolated X-ray pulses, which were used to irradiate different types of electronic circuits (based on silicon, SiC and GaN technologies, whether test circuits or commercial components).

The irradiation tests were carried out with different photon energy levels (from 14 to 18 keV) and different pulse durations (from 100 pico-seconds to 80 micro-seconds). The goal of these measurements was to determine which events can be induced in these electronic circuits using single X-ray pulses, in different conditions, and to compare the results obtained with similar measurements produced using a heavy ions beam.

In the context of the activities of the program, the ESRF launched a research program to develop and validate a novel testing methodology for the RadHard domain of the electronic industry. In this attempt the ESRF is supported by a core group of partners representative of the main stakeholder.

Florent Miller, engineer at Nuclétude/ArianeGroup, could access to the ESRF in this framework: *"Focused pulsed X-ray sources offer considerable potential as a complement to heavy ion accelerators in evaluating sensitivity to the effects of radiation (such as the single event type) on electronic components for space applications, owing to the ability of X-ray photons to pass through the component packages, while most of the heavy ion tests require prior preparation (laser and/or chemical ablation of the package to allow direct access to the component chip)",* underlines Florent Miller. *"The problem is particularly acute for power components, owing to the potentially destructive nature of the test and the number of samples then needed to obtain sufficient statistics to characterize their sensitivity to the effects of radiation"*.

↑
ID09 beamline at the ESRF, operated under Nanoelec. © *S.Cande/ESRF*

Irradiation

Effects of Thermal Neutron Radiation on a Hardware-Implemented Machine Learning Algorithm

Hardware-implemented machine learning algorithms are finding their way into various fields, including safety-critical applications.

These algorithms have to perform correctly even in harsh environmental conditions, such as in avionics at altitude. Support Vector Machine (SVM) is an important Machine Learning algorithm that has been the target of hardware implementation in recent years. A scientific team from UGA, CNRS, Grenoble INP, Universidade Federal do Rio Grande do Sul, (Brazil) and Institut Laue-Langevin (ILL) published the very first work to assess both Binary and Multiclass SVMs under thermal neutron radiation, a type of particle noticeably present at high altitudes. At the ILL, they performed a fault injection campaign along with a radiation test with the D50 thermal neutron source operated under Nanoelec. They demonstrated high intrinsic fault tolerance for both varieties of the SVM algorithm, especially for the Multiclass SVM.

Matheus Garay-Trindade & al.
Effects of thermal neutron radiation on a hardware-implemented machine learning algorithm.
Microelectronics Reliability, 2022

↑
The CEA Characterization platform is part of the Nanoelec Characterization program. © *Cottet/CEA*

Training design

VR + AI visit for education

A number of initial training actions continued in 2022, via collaboration between the CHIF program and the Nanoelec Carac program.

↑
Screenshots of the virtual reality visit to the Tenis equipment. The application has an avatar with artificial intelligence which can dialog with the visitor, inform them and guide them.

© ILL

A half-day module dedicated to the large instruments was presented to the Master Nanotech students and a one-week course was given to the students of the Grenoble PhD school.

Finally, the preparation of a teaching capsule specifically for the large instruments was launched[14]. This capsule, will be based - among other things - on the performance of a virtual reality experiment based on a 3D reconstruction of the TENIS instrument at the ILL, developed in collaboration with the Ubilink company in Grenoble.

Two visits to Tenis accompanied by an avatar are available: a discovery visit and a technical visit. The application can also be used in free mode. The avatar has artificial intelligence that must be trained so that it can answer the various questions from the visitors.

"For us, this virtualization enables the new user to be guided through the preparation of their experiment", explains Manon Letiche (ILL) who designed the visit. *"The fact of being able to move freely around the model will make it possible to anticipate certain often extremely time-consuming problems that arise when setting up the system. The virtual visit is available on a mobile phone and/or a VR headset and will attract a new audience to the fairs and conferences at which the PAC-G is present. The aim is two-fold, because the virtual visit is a means of gaining the attention of a potential new customer to whom we can then show the PAC-G offering and the other techniques available."*

14. This virtual environment will eventually be used to produce practical work course modules and train students for testing electronic components under irradiation.

Open AI Dall.e provides its own view of the "inside the heart of the Institut Laue-Langevin nuclear reactor, painted by Vincent Van Ghog".

© created with Open AI Dall.e, 2023

TECHNOLOGY DISSEMINATION

CONTENTS

Promoting the adoption of emerging technologies in new application fields

TECHNOLOGY DISSEMINATION PROGRAM AT A GLANCE

→ Vision

Sovereignty in the electronics industry requires efficient dissemination of innovative components and their adoption by national and European integrators and end-users

→ Ambition

To identify weak signals from the market and to accelerate the time to market of technologies developed by Nanoelec partners with fast prototyping and tests as well as access to merging markets

→ Mission

- to help component and software manufacturers better understand the needs/possibilities of new applications
- to provide companies, notably SMEs, with information to plan ahead for the arrival of new technologies
- to contribute to the ambition of re-industrializing France and Europe
- strengthen investor confidence with IRT industrial partners

→ Partners

CEA, Minalogic, Grenoble INP-UGA, Captronic/Jessica France, STMicroelectronics, Lynred, Prophesee, GEM

Responsible integration of numerical devices in SME processes is the motivation behind the Nanoelec/Technology Dissemination program.

© Olivier Devise/Grenoble-INP

As far as the digital transition is concerned, technologies and components are focused on few mass markets and companies sometimes lack the information and the in-house skills needed to integrate new technologies. However, these technologies are also opportunities to expand their offering and strengthen their commercial position.

With the Technology Dissemination program, the partners in Nanoelec are promoting and accelerating the dissemination of emerging devices and new technologies in a variety of application fields; they are drawing more particularly on R&D skills in imaging, artificial intelligence, embedded software and electronic systems design.

The program comprises two initiatives:
- The aim of the System Lab initiative is to exploit innovative imager components developed by major industrial partners involved in R&D programs at Nanoelec. New applications and uses cases are explored.
- In the Easytech initiative, we make advanced electronic blocks embedded software accessible to SMEs and mid-cap businesses, including those whose core business is anything but digital. The aim is to enable them to take the digital transition on board, to increase the added value of their products or improve their manufacturing processes.

In 2022, the core of Easytech's business remains concentrated in the Auvergne-Rhône-Alpes region, but the national distribution is significant with 25% of the 16 contracts signed. As for System Lab, the platform is now made up several sensors providing multimodal and multispectral imaging; all sensor and peripheral control board has been developed; embedded artificial intelligence software for object recognition and open access imager plateform has been implemented. Several use cases have been tested on sites, up to April 2023, when a seminar dedicated to “New Imaging for sport and health” was organized.

—

The Technology Dissemination program was managed by Elvir Mujic (down right, Minalogic), until may 2023, then by Florent Bouvier (down left, Minalogic) in charge of the Easytech initiative. Also, Sandra Tochon (up right, CEA) in charge of the System Lab initiative is now replaced by Christophe Vautey (up left, CEA).

© P.Jayet/CEA | DR

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System Lab

It is time for new usages of imaging

System Lab was launched in 2020 and established as part of the Nanoelec Dissemination program in 2021. Y.Spot, the open innovation center at CEA, operates this initiative.

SANDRA TOCHON (CEA-Y.Spot), co-director of the Technology Dissemination program, in charge of SystemLab up to April 2023, explains.

↑
Sébastien Balle, engineer, and Germain Magat, designer (CEA), are setting up the System Lab technical platform at the Y.Spot studio box dedicated to Nanoelec. The commercial offer easy access for testing the platform on new use cases will be soon named Addvisia.

© P.Jayet/CEA

Where did the idea of creating System Lab come from?

Together with our main industrial partners, we felt that it would be interesting to enhance Nanoelec's technology dissemination offering, by organizing a stronger and more direct link with the R&D programs. In the System Lab initiative, we work with the component manufacturers looking to explore new application fields.

What is the concept?

We are exploring the use of new sensors based on the synergies between building technical blocks provided by various partners and on approaches closely linked to the potential users. In the medium or long term, we will use the results of this process to expand or enrich the characteristics of our partners' components and generate opportunities for new technological routes, new markets.

So what is the approach?

The System Lab partners share an open technical image platforms, methodologies to support open innovation processes combining creativity skills, exploitation of large usage scenarios, value analysis and eco-design. We created an open platform for use case exploration and evaluation based on merging optical sensor data flows. The components are supplied by our partners and we work on their integration at the system level integrating data fusions, spatial and temporal coherencies.

What fields are concerned?

First of all, we work on the functions and services that can be introduced by multispectral image sensors. We aim to seek out what has not been explored yet. This means that we have to take account of many additional technical aspects, such as AI, data security, and data fusion.

What is the driving force behind your coordination of the initiative?

System Lab is a new way of exploiting the technology that we engineers hold so dear. It creates a link between the largest possible number of players, from widely differing backgrounds and sectors. which means meeting committed and fascinating men and women, virtually every day.

We benefit from pathways already opened up by our colleagues in the open innovation team at CEA-Y. Spot. Their methods for leading workgroups and generating new designs are absolutely amazing. It's now up to me to organize and coordinate that for our partners!

What fields are concerned?

The developments in System Lab can deal with component architectures, but also new functions (security, signal processing, data fusion) or manufacturing processes needed for implementation of these innovations on the products. We work first of all on the functions and services that can be introduced by multispectral image sensors. •

System Lab

Innovating in imaging usage

System Lab is a dynamic collaboration between STMicroelectronics, Lynred, Prophesee, and four institutional stakeholders[1]. It aims to explore new imaging applications, by combining the data from existing optical systems. The purpose of the approach is to help bring the potential users together with the optical imaging R&D players, by exploring, anticipating and paving the way for the technologies and usages of tomorrow.

An operational platform

Thanks to the provision of sensors from STMicroelectronics, Lynred and Prophesee as well as the development of interfacing software to ensure the spatial coherence and temporal synchronization of the sensors, the System Lab platform was commissioned at the end of 2021.
It aims to prototype usage ideas for merging data from these multispectral sensors. The platform was presented to industrial firms and has already been the subject of discussion between experts on applications as diverse as gas leak detection, the creation of digital twins for buildings or waste sorting.

↑
Sandra Tochon & Thimothée Silvestre, engineers at CEA/Y.Spot, during a creativity session on the System Lab.
© P.Jayet/CEA

JEAN-LUC JAFFARD
VP hardware at Prophesee[2], analyses what is at stake.

What challenges do you anticipate for innovation in imaging?

There is first of all the wavelength. Between an ultraviolet sensor and an infrared sensor, there is a lot of different details to see. So, if I want to create a new application, maybe the first question to be answered is what wavelength will I be using.

The second is, what do I want to do with it? Do I want to take photos? Video? Smart vision to move a robot ? This is where I start to look at the quality of the image.
Moreover, the development of automated image processing has appeared more recently. From this viewpoint, it is no longer the quality of the image that is important, but the quality of the information that one wishes to detect.

How do you explore all these issues at the same time?

Adressing the field is a huge difficulty for a single actor who would have necessarily to cover areas far

→ 100

from his key skills. The very large applications stakeholders are capable of setting up this type of platforms, but this is style complex for medium-size actors. So much is to be gained from close collaboration between several players in the field, in order to look for and identify optimal solutions.

Is System Lab an advantage in meeting these challenges?

In Grenoble-Alps area, we are extremely lucky to have a large pool of companies involved in imaging. This configuration is almost unique in the world, where within a circle thirty kilometers in diameter, all the imaging technologies are potentially available.

To build System Lab, this was our starting point and we all tried to work together in order to exploit all these technologies for the common good.

The idea is to try to create a platform which uses a certain number of technologies from stakeholders in the valley, to put these technologies together and obtain something that is easy to use and on which someone wishing to test a new solution will rapidly be capable of obtaining information about the various types of sensors, fine-tune their application and determine what type of technology they will be able to use for this application.

What does Prophesee bring to System Lab?

We use a latest generation camera with a resolution of 1280 X 720 pixels. It is highly sensitive and detects changes in contrast while consuming very little (3nW/event).

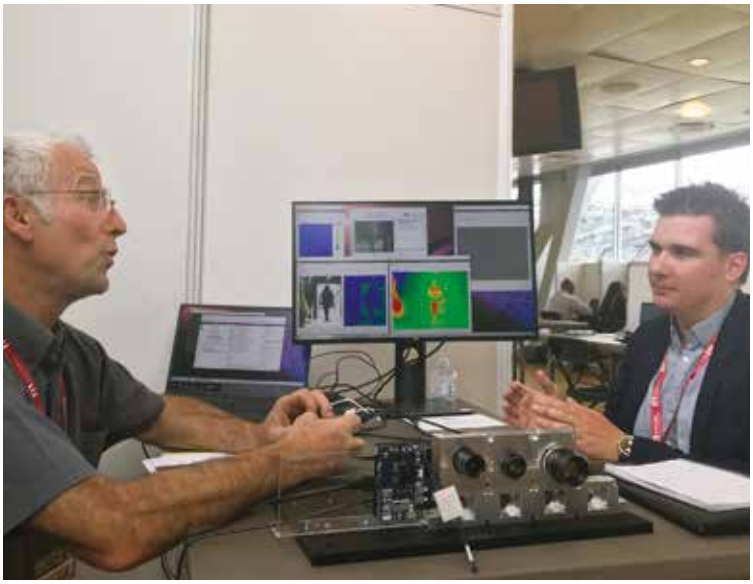
Are you already seeing tangible results from this approach?

What we're beginning to see after eighteen months of activity is actually unique and after a first generation, each of the partners is beginning to come up with the new generations of sensors enhancing the solutions and demonstration capacity. For the application examples, there are an enormous number of new areas in imaging which require data merging, hence the interest of pooling these technologies in a unified environment, which is portable, and easily adaptable to different use cases. •

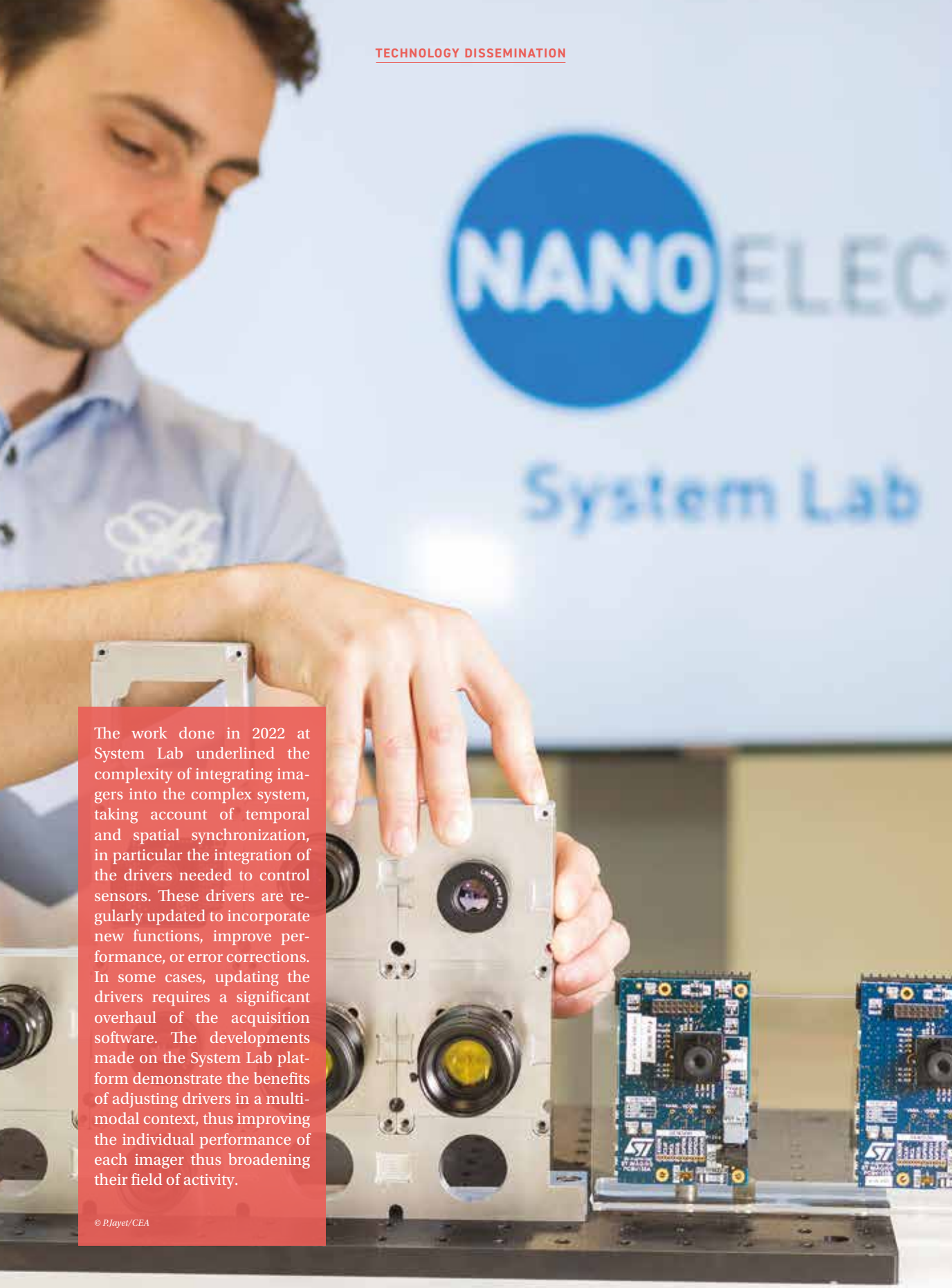
1. The four partners, in addition to the industrial firms, are Captronic, Minalogic, Grenoble Ecole de management and CEA. Y.Spot, CEA's open innovation center, is managing the initiative.

2. Based in Paris and Grenoble, Prophesee is developing a technology which reproduces the behavior of the human eye and the way the brain processes the information it receives from the eye.

"SO MUCH IS TO BE GAINED FROM CLOSE COLLABORATION BETWEEN SEVERAL PLAYERS IN THE FIELD, IN ORDER TO LOOK FOR AND IDENTIFY OPTIMAL SOLUTIONS."



↑
In 2022, the System Lab demonstrator was presented in different contexts, in France, here at the Minalogic Business Meeting in Grenoble.
© F. Legrand/CEA



The work done in 2022 at System Lab underlined the complexity of integrating imagers into the complex system, taking account of temporal and spatial synchronization, in particular the integration of the drivers needed to control sensors. These drivers are regularly updated to incorporate new functions, improve performance, or error corrections. In some cases, updating the drivers requires a significant overhaul of the acquisition software. The developments made on the System Lab platform demonstrate the benefits of adjusting drivers in a multimodal context, thus improving the individual performance of each imager thus broadening their field of activity.

© P.Jayet/CEA

Easytech

Growing success with SMEs, mid-caps and start-ups

Established in 2012, the Nanoelec/Easytech initiative provides global support for SMEs and mid-caps in their innovation process (creativity, expertise, R&D project). It is operated by Minalogic, a global innovation cluster for digital technologies, supported by the Auvergne-Rhône-Alpes Region and local authorities.

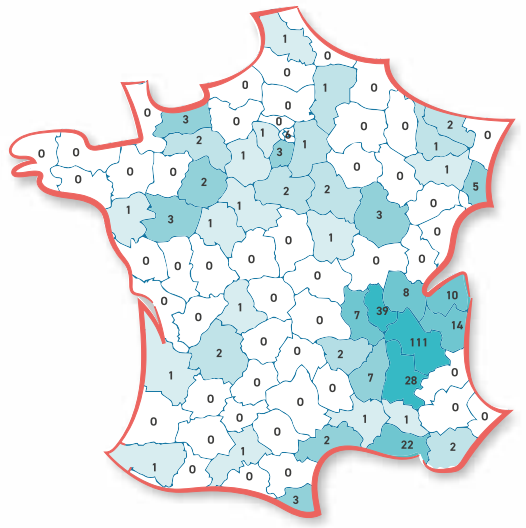
Easytech is attracting a diversity of companies. It offers a simple and easy fast-track for innovation projects. According to our survey, it is really appreciated by managers of small companies & startups, given that such companies do not necessarily have large R&D departments. 295 Easytech projects have been sponsored with more than 200 companies since 2012.

"We deal primarily with SMEs, a few mid-caps and an even fewer number of large companies. Most of these companies are in the Auvergne-Rhône-Alpes region", explains Elvir Mujic (Minalogic) co-director of the Technology Dissemination program, in charge of the Easytech initiative up to April 2023. *"Their core business is usually electronics but sometimes also maintenance and mechanics, instrumentation, materials, or other fields."*

Their application markets are highly diversified, ranging from space to health, to new modes of mobility, construction, sport and the agriculture+food industry.

Like all IRTs, Nanoelec's main focus is not solely thematic, but also regional. This is why the local authorities top up funding for the Easytech projects. This helps bring down the financial risk for the local companies that innovate with us. First of all, the Auvergne-Rhône-Alpes region contributes 20% to the approved projects. Moreover, local authorities (mainly cities and urban areas) can add 10% for projects for SMEs based in their district. This is the case with Grenoble Alpes Métropole, Valence Romans Agglomération, Saint-Etienne Métropole, Thonon Agglomération, La communauté du Pays Voironnais, Annemasse Agglomération, Clermont Auvergne Métropole. More than one quarter of our projects are also carried out with companies in other regions of France.

The Easytech initiative also takes better account of the societal and environmental impact of the innovations developed with the SMEs. *"In 2021, we carried out a pilot experiment called Defi-Ino,*



This map shows the geographical origin of the Easytech partner companies since the initiative was launched in 2012. The core business is concentrated in the Auvergne-Rhône-Alpes region, but nationwide dissemination is significant. Contracts have been signed for 88 projects outside the Region since the program started, out of a total of 310, or 28%. In 2022, contracts were signed for 4 projects outside the Auvergne-Rhône-Alpes Region out of a total of 16 (25%).

"IN 2022, 10 NANOELEC/EASYTECH PROJECTS WERE CARRIED OUT BY STUDENT-ENGINEER TEAMS, WITH THE SUPPORT OF THE TEACHERS AND RESEARCHERS AT ESISAR, THE SCHOOL OF THE GRENOBLE INP - UGA GROUP LOCATED IN VALENCE."

in collaboration with Nanoelec and the Ines.2S ITE: we are looking to develop an environmental diagnostic offering for SMEs, mid-caps and start-ups wishing to work with us. Our priority is to help companies cope with the environmental issues of public innovation policies and to provide them with competitive advantages", adds Elvir Mujic.

Under the Easytech Technology Dissemination initiative, with the support of the Auvergne Rhône-Alpes region and local authorities, Nanoelec has accompanied more than 306 companies since 2012. *"In 2021, Nanoelec carried out a socio-economic impact study on 101 of these projects: the analysis reveals that more than 3 out of 4 projects result in expanded activity after the Easytech phase and that it takes on average 2 years for a project to enter the commercialization phase"*, adds Florent Bouvier (Minalogic), who replaces Elvir Mujic in leading the Easytech initiative. •

Easytech

Pocket lab to detect pathogenic bacteria

In January 2022, Direct Analysis presented a prototype of a portable device to detect pathogenic bacteria in the agriculture and agri-food sectors.

This demonstrator was developed under an Easytech project run with CEA in 2021 and 2022. In the mean time, Direct Analysis was awarded in 2021 Grand Prix of the BPI I-Lab Challenge.

"We are developing microfluidic chips for DNA extraction. Our test will be four times faster than those currently on the market", says Thomas Bordy, one of the co-founders of Direct analysis. The company is a CEA spin-off, created in February 2021. As soon as it was created, the company was able to market a consumable for sample preparation with no need for a laboratory. "It is now already in continuous use in agri-food plant quality laboratories, where it drastically reduces the time taken to obtain results", says Thomas Bordy. The second step consists in developing a "field" version for direct read-out of the analysis results.

"Three similar machines have been designed and produced under Easytech", explains Charles Elie Goujon, Project Manager at Y.Spot (CEA). *"To facilitate the use of the device, we decided to make analysis start-up automatic: simply by closing the device, the user starts the process. To do this, we have a mechanical system inside the reader which places the heating element in contact with the component (65°C in just a few seconds), and places the target DNA amplification read-out imager at the right height in front of the sample."* The main work done in 2022 concerned the design of the electronic parts and software implementation, at a time of extreme pressure on supply lines. •

↑
The prototype of the pathogenic bacteria detection analyzer for the agriculture and agri-food sectors, developed by CEA and Direct Analysis under Easytech.

© C-E. Goujon/CEA

Easytech

Detecting abnormal heating

Orioma, a start-up co-founded and accompanied by Linksium, won one of the 10 grand prizes at the i-Lab 2022 competition.

The company is developing a compact camera needing no outside power. *"Our camera can operate for 15 years with no battery, cable, or maintenance"*, explains Serdar Manakli, one of the company's co-founders. This technological feat is achieved using an innovative infrared sensor coupled with artificial intelligence functions.

"Under an Easytech project, CEA-Leti helped Orioma develop an abnormal heating detection algorithm, for example to monitor the correct working of an industrial process and sound the alert if necessary", adds Serdar Manakli. The ultimate goal is to be able to run compact thermographic analysis efficiently within the camera, while retaining the advantages and energy frugality of the system.

Oriama's technologies come from CEA-Leti and the TIMA laboratory (CNRS/UGA/Grenoble INP). Serdar Manakli is proud of the i-Lab award and admits that his goal *"is to be the global reference for energy-independent connected objects within the next 5 years."*

"OUR CAMERA CAN OPERATE FOR 15 YEARS WITH NO BATTERY, CABLE, OR MAINTENANCE."

Tiny and Self-powered device for massive energy-saving in building sector. © *Orioma*

Easytech

Towards a sovereign European processor

"The SiPearl start-up is raising 90 million euros to speed up the marketing of a European microprocessor." Such was the headline of the Usine nouvelle on April 5, 2023, echoing the start-up's official announcement.

SiPearl is building the world's first low-consumption microprocessor specifically for high-performance computing and designed to operate with any third-party accelerator (GPU, AI, quantum). It aims to be the core of Europe's supercomputers.

"Our ambition is to be the leading designer of high-end microprocessors in France and in Europe", explains Vincent Casillas, SVP R&D Software at SiPearl. "*With our Rhea microprocessor, we aim to contribute to Europe's technological sovereignty in the critical fields of artificial intelligence, medical research, combating climate change and energy management.*"

Under an Easytech contract in 2022, SiPearl and Grenoble INP-UGA developed advanced functionalities on RISC-V[3] coprocessors present in the Rhea chip designed for supercomputers and data centers.

3. RISC-V is an Instruction Set Architecture (ISA) in the processor's native language. There are various ISAs, but what makes RISC V specific is the that it is free for any user to use and develop.

↑
The SiPearl team (around Vincent Casillas) at work on the Easytech project. *© Sipearl*

"These coprocessors will provide security and power supply management functions for the ARM Neoverse V1 computer cores", says Vincent Casillas. *"The main technological hurdle for this project was the fact that the chip itself was only at the design stage! But we could not afford to waste time because the advanced functionalities to be developed on these dedicated micro-controllers will have a significant impact on differentiation with respect to the offerings from the competition."*

At the end of the Easytech project, SiPearl had a solution for testing the Rhea bootload sequence[4] as well as the tools allowing automatic start-up and execution of unit and functional tests on the coprocessors. *"This solution allows shorter iterations in the development phases, while ensuring the stability of the functionalities already developed and tested. Consequently, we speed up our technological development thanks to Easytech"*, Vincent Casillas concludes. •

4. Bootloader: minimum program enabling code to begin on a chip at start-up

Dall.E may provide ideas for driving the design of a device for pathogenic bacteria detection.

© created with Open AI Dall.e, 2023

HUMAN CAPITAL & TRAINING DESIGN

↗
Panagiota Morfouli, Professor at Grenoble INP-UGA, co-Director of the Nanoelec/Human Capital & Training Design program

© P.Jayet/CEA

↗
Sylvie Blanco, Senior Professor and Leader of the Technology and Innovation Management Institute at Grenoble Ecole de Management (i.e. Grenoble Graduate School of Business), co-Director of the Nanoelec/Human Capital & Training Design program

© P.Jayet/CEA

Sustainable development as a driver of innovation

A learning community of students working on attractiveness of microelectronics business.

CHIF PROGRAM AT A GLANCE

→ Vision

The competitiveness of the electronics sector is linked to the development of interdisciplinary, agile collaboration capacities.

→ Ambition

Design and experiment with an integrative and customized learning and training design system that strengthens the human capital, and the dynamic innovation capabilities of the institute and its academic and industry partners.

→ Mission

Design and develop new training module content and formats within three areas: fundamental skills, experience-based learning, and learning communities to tackle emerging challenges.

→ Partners

Grenoble INP-UGA, Grenoble Ecole de Management (GEM), STMicroelectronics, Schneider Electric

The overall goal of the Human Capital & Training Design program is to design, develop, test and prepare the rollout of Elise (Experiential Learning of Innovation for Sustainable Ecosystems) throughout IRT Nanoelec.

An unprecedented program in Europe, Elise is based on experiential learning and co-engineering, it brings together scholars, industrials, engineers and managers, and offers standard university curriculums and continuing education programs. It has been designed to address the upskilling needs of the IRT Nanoelec ecosystem: high technological intensity, wide-ranging fields of application, and a commitment to sustainable development.

The project includes three complementary focus areas: common capsules of IRT Nanoelec-specific fundamental skills; experimental sessions in immersive environments such as labs and demonstrators for hybrid collaborative teams involved in institute research; and learning communities committed to sustainable electronics applications.

—

Capsules for fundamental skills

Mission in a cleanroom

An educational capsule to raise awareness of cleanrooms and their process flows.

An educative team lead by Céline Ternon, professor at Grenoble INP-UGA, has developed two virtual reality tools under the Nanoelec/CHIF program, with the aim of enabling as many students as possible to discover the microelectronics cleanroom environment, the notion of process flow and the various characterization techniques required to monitor a technological process in microelectronics hardware fabrication. The first steps were unveiled at the Euromat conference in 2021[1].

"We chose to rely on an electronic device that students would be drawn to: the photovoltaic cell", Céline Ternon says. First of all, a virtual reality tour of the CIME-Nanotech cleanroom — developed with the Maison pour la science as part of the Idex UGA project and Nanolec/Chif program — is an immersive experience that provides information about process flows, machines and the work environment. Next, a video game allows students to characterize the materials throughout the integration process as if they were actually in the cleanroom.

"Finally, we chose an original scenario that would spark participant curiosity and motivation. Players become spies for an activist association; they aim to make inventions and technologies that are beneficial to the planet and humanity, and available to all humankind. The association's next mission is to obtain the architecture of the latest first-generation solar cell manufactured in the CIME Nanotech cleanroom. To do this, spies first join a tour of the cleanroom open to the public (virtual tour), in order to prepare their mission and to collect the target data (video game)", reports Céline Ternon. •

1. Céline Ternon & al. Cleanroom or virtual reality mission to learn about microelectronics. *2021 Euromat conference.* *© Grenoble INP-UGA*

A spy mission in a microelectronics cleanroom has been designed in a serious game environment by Grenoble INP-UGA as part of the Nanoelec program.

© CEA

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Capsules for fundamental skills

From early adopters of the technology to major markets

Learning capsules help students to describe and understand the adoption and diffusion of technological innovations such as smart systems, in close collaboration with a disruptive startup with high growth potential.

↑
Since 2015, ISKN has sold over 100,000 Slate graphic tablets. © *Franck ARDITO/CEA*

"A learning capsule entails 40 minutes of interaction, thought and self-assessment", explains Emmanuelle Heidsieck, educational engineer at Grenoble Ecole de Management. In 2022, she coordinated the design of learning capsule "ISKN/AMI: accelerating entry into a major market", which analyzed drivers for progress for startup ISKN/AMI from 2014 to 2021. ISKN/AMI is a spinoff startup of CEA-Leti, supported by Nanoelec R&D, and acquired by BIC in 2022.

"The growth of startups based on hardware and software technologies is a major challenge for innovation ecosystems such as Nanoelec. To drive progress, we believe in learning from seasoned entrepreneurs who have experienced the process within the ecosystem, and who are willing to question themselves in order to learn", explains Pars Mukish, Director of Knowledge Management at Yole Intelligence, who oversaw content creation.

"We confronted the diffusion of ISKN solutions with a diffusion-of-innovation curve based on research by Everett M. Rogers and Geoffrey Moore. We then used a specific curve based on the theory of "Big Bang" disruption", states Pars Mukish. *"The curve analyses demonstrated that crowdfunding is not a pre-sales tool; on the contrary, it makes startups face operational and financial targets too soon given their level of maturity."*

"The objective of the capsule is to test the capacity to describe and understand the adoption and diffusion of technological innovations such as smart systems, in close collaboration with a disruptive startup with high growth potential", he continues. The driving effect of sustainable values is put into question. Once the capsule has been completed, learners are able to use an analytical approach with specific entrepreneurial and technological tools, and to delineate diffusion determinants for a given technology and innovation, in a real-life company setting, with the support of Nanoelec.

> "THE OBJECTIVE OF THE CAPSULE IS TO TEST THE CAPACITY TO DESCRIBE AND UNDERSTAND THE ADOPTION AND DIFFUSION OF TECHNOLOGICAL INNOVATIONS SUCH AS SMART SYSTEMS…"

"We relied on the insight of Jean-Luc Vallejo, one of ISKN/AMI founders, who had previously attempted to understand the overall process in order to share his learnings with Nanoelec partners", adds Emmanuelle Heidsieck. She specified that the capsule is geared to future managers or engineers in microelectronics and its fields of application, who have basic knowledge of corporate management and strategy. It is also well-suited to techno-entrepreneurs of startup projects, to leading innovative businesses which use Nanoelec technologies, as well as to research managers who focus on marketing of technological innovation. •

The experiential learning program

Agent of Better Cyberlife

ABC Stories are a tool and a workshop to understand and promote the adoption of connected solutions.

Nanoelec develops comprehensive technological applications aimed to integrate complex systems (not products or isolated processes). Growth and sustainable impact are of vital importance in these innovations, which reconfigure systems and overall practices, and which are tailored to environmental and societal needs. *"This novel and complex concept is difficult to grasp"*, states Sylvie Blanco, Professor and leader of the Institute for Sustainable Technology Innovation Management at Grenoble Ecole de Management, co-Director of the Nanoelec/Human Capital & Training Design program (Chif).

"As a result, we have developed a tool to examine the sustainable development and connectivity value that customers perceive in a new solution."

Developed in 2022 at Grenoble Ecole de Management as part of the Nanoelec/Chif program, ABC Stories *"enhances skills in innovation marketing, the goal being to demonstrate the use of new solutions and to spark reactions and discussion with target audiences and potential customers. It is similar to Alberto Savoia's[2] pretotyping techniques"*, continues Blanco.

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2. Pretotyping is a set of tools, techniques, and tactics designed to help validate a new product quickly, objectively, and accurately. Pretotyping was originally developed at Google in 2010 and since then has been tested, refined, taught, and put into practice with great success in hundreds of projects and organizations. The concept was developed by Alberto Savoia, former engineering director and innovation agitator at Google, in his book The Right It.

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Students from la Cité scolaire internationale de Grenoble. Award ceremony for the IRT Nanoelec 2022 "Youth" challenge prize: Mission "Agent for Better Cyberlife". © *GEM*

ABC Stories focuses on innovative solutions based on image sensors built with artificial intelligence. It has been tested with different groups and in different educational scenarios: with university and high-school students, and with research professors.

"The learning capsule for the ABC Stories tool teaches participants about adoption determinants of smart solutions by early adopter customers, and focuses on a basic experiential co-design approach to analyze the mediating effect of perceived value on customer behavior", specified Blanco.

ABC Stories was also used for a video contest as part of the 2022 Nanoelec challenge called Mission ABC: Agent for a Better Cyberlife. *"Using a technological solution with a camera, image sensors and artificial intelligence, 32 high-school candidates from Cité Scolaire Internationale de Grenoble were up to the challenge. They created a video or a storyboard to encourage users to imitate their behavior and thus avoid misuse of the solution"*, explains Isabelle Sauret, communication and events manager at GEM, and contest organizer. Seventeen videos were shared on YouTube to spark reactions and discussion with an open community.

"USING A TECHNOLOGICAL SOLUTION WITH A CAMERA, IMAGE SENSORS AND ARTIFICIAL INTELLIGENCE, 32 HIGH-SCHOOL CANDIDATES FROM CITÉ SCOLAIRE INTERNATIONALE DE GRENOBLE WERE UP TO THE CHALLENGE."

Overview of the experiential learning program

Engineers for sustainable solutions

The Piste program provides engineers with hands-on experience regarding the challenges of sober and sustainable technological innovation projects.

Piste is a 378-hour learning program divided into four training modules. It began in 2021 at Grenoble INP-UGA, with the support from Nanoelec. In 2022, it became a full-fledged program. It has been presented at the European Society for Engineering Education conference[3].

Piste aims to provide an all-encompassing experience that will give students a sense of the real-life challenges they will face as engineers. The program's main project is based on theoretical learning. The challenge for students is to bring together local companies in order to offer global solutions that will ensure a sober and sustainable approach throughout every project stage. The students' work provides valuable feedback for stakeholders. They are creators of sustainable innovation.

The program focuses on new skills suitable to address the socio-ecological transition. Engineering students become experimenters of sustainable solutions. The program's educational material and hands-on experience are varied, as for example, serious game My IoT, a collaborative initiative between Nanoelec and Idex UGA.

3. Feron, A., Poinsotte, F., & Jossic, L. (2022, 22.09). Co-designing a curriculum for sober techno- and eco-responsible engineering: Transition to a new professional identity for a sustainable world. SEFI22 *(The European Society for Engineering Education), Barcelona, Spain.*

Learning community to tackle challenges of responsible microelectronics

Experimenters of Sustainable Technology and Innovation Management

Learners in the Estim learning path have access to robust and useful innovation tools, and experiment with them in real-life situations.

In 2022, the co-design process of the experiential learning program at Nanoelec/Chif was adjusted to ensure a proper balance between theoretical learning and empirical scenarios. The main challenge is to provide high quality learning that is up to par with our partner's norms and accreditations. We also want to help students to be thorough in hands-on activities, and for their experience to be shareable, useful and reusable within the community.

The Estim learning path (Experimenters of Sustainable Technology and Innovation Management tools) is essentially geared to students completing a final-year dissertation based on solving an industrial innovation problem. Learners must test sustainable and robust tools in real-life situations.

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↑
Pierre Harrisart (Schneider Electric) during a workshop to identify and test sustainable innovation tools, which were designated as energy-efficient applications in the Estim Learning path.
© M. Colletti/GEM

"When working on innovation tools, the entire process does not thoroughly and validly address sustainable development issues. Nowadays, few approved tools are recognized as sustainable despite numerous initiatives and communication campaigns", explains Sylvie Blanco (GEM), who coordinated the Estim program's development. *"To move forward, we rely on published research to create or adjust tools and practices to be sustainable, and to test them on real use cases",* adds *Michele Coletti, Associate Professor at GEM, who designed the Estim program. She adds that such an approach "will become vital for sustainable innovation practices in the coming decades."*

"TO MOVE FORWARD, WE RELY ON PUBLISHED RESEARCH TO CREATE OR ADJUST TOOLS AND PRACTICES TO BE SUSTAINABLE, AND TO TEST THEM ON REAL USE CASES"

The learning approach is based on a DSRM methodology.[4] It includes support workshops for students working on a real-life project with a deliverable (i.e., case study) or an article publication.

The learning path was designed in conjunction with students enrolled in a GEM Master's degree in energy management and marketing, and in international affairs for technology innovation management.

For example, at Schneider Electric, Pierre Harrissart conducted a study on eco-friendly habits geared to people in individual housing units. The goal was to generate consumer engagement on energy savings. The study was carried out as part of the Master's program in energy management and marketing (GEM and Grenoble INP-UGA/ Ense3). *"Estim readily provided a methodology and tools that helped to clarify and address the issue"*, he explains. Harrissart had to work within an existing ecosyste m (a Schneider Electric solution), and to develop an approach based on artificial intelligence in order to raise end-user awareness and get them to reduce their energy bills and, therefore, their environmental impact. *"The tailored messages — some short, others very short — are intended to raise end-user awareness about their daily energy consumption and to foster customer loyalty. These messages are still not used sufficiently",* adds Pierre Harrissart. *"Qualitative results and management based recommendations are provided in storyboard form during workshops and user-oriented surveys. In the future, the development and implementation of eco-friendly habits will promote user involvement, and, as a result, win over the housing market."*

4. Design Science Research Methodology is a research process to design, develop, and evaluate information systems, technologies, and artifacts. It is focused on creating innovative solutions to complex problems by using a cyclical process of design, evaluation, and improvement. Peffers, K., Tuunanen, T., Rothenberger, M. A., & Chatterjee, S. (2007). A design science research methodology for information systems research. Journal of Management Information Systems, 24(3), 45-77.

Learning community to tackle challenges of responsible microelectronics

Anticipating the rollout of digital product passports

In February 2023, 52 students from Grenoble INP-UGA and Grenoble-Ecole de Management, and experts, participated in a workshop for digital product passports as part of the EU's sustainable products initiative.

ESTELLE BELIN-DI STEPHANO, educational engineer at Grenoble INP-UGA/Phelma for the Human Capital & Training Design program at Nanoelec, provided an overview.

What is a Digital Product Passport?

In March 2022, the European Commission introduced a proposal aiming to make almost all physical goods more sustainable and energy efficient throughout their life cycle. One of the goals of the eco design for sustainable economy initiative is to create a digital passport for every product [5].

How will it work?

The passport will provide information on the product's environmental impact according to sustainable development criteria. It aims to make the repair, recycling, reuse and resale of a product easier, and to increase transparency about the product's impact on the environment and society throughout its life cycle.

What products does it cover?

It is a priority for the following industries: electronics and electric vehicle batteries. The goal is to have access to increasingly sustainable and recyclable products in order to reduce their carbon footprint, and to raise consumer awareness about their choices.

How did you get students and industry experts to work together?

The two-half-day workshop took place on February 10 and 24, 2023. The sessions were organized in cooperation with experts from ST-Microelectronics, CEA-List, Akileo, and students from Grenoble INP UGA, GEM. As part of a Nanoelec program, students worked on the digital passport for a Nucléo circuit board. The small electronic board contains a processor, as well as memory to, for instance, program and control actuators through event-detecting sensors.

What method did they follow?

Students broke up into small groups, and were assisted by business professionals. They had to design the digital passport of a Nucléo circuit board, a secondary board and its sensors (i.e., for humidity, temperature, optics, etc.), and the communication modules (i.e., Bluetooth, 4G, Wi-Fi, etc.). The product was tailored to one of the following five fields of application: voice recognition, mini weather station, bicycle radar, programmable lighting, and water quality control.

↑
Estelle Belin-Di Stephano, educational engineer at Grenoble INP-UGA/Phelma, is part of the Human Capital & Training Design program at Nanoelec.
© DR

5. Funded by the European Commission as part of the Digital Europe Program, CIRPASS is a collaborative initiative that prepares the ground for the gradual oversight and deployment of a standards based Digital Product Passport (DPP) in accordance with the requirements of the Proposal for Eco-design for Sustainable Product Regulations (ESPR), and with an initial focus on electronics, batteries, and textile sectors.

"THE MICROELECTRONICS INDUSTRY HAS A LONGSTANDING COMMITMENT TO REDUCING ITS ENVIRONMENTAL IMPACT ACROSS THE ENTIRE LIFECYCLE OF PRODUCTS.
OUR PARTNERS ARE CONVINCED THAT MICROELECTRONICS ENGINEERS AND MANAGERS MUST TAKE ACTION AT THEIR OWN LEVEL, BOTH AS EXPERTS WITH HIGHLY SPECIALIZED SKILLS AND AS RESPONSIBLE CITIZENS, TO CONTROL THE IMPACT OF TECHNOLOGIES, CREATE NEW "ECO-FRIENDLY INSTINCTS" AND HELP REDUCE HUMANITY'S OVERALL ENVIRONMENTAL FOOTPRINT."

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A Nanoelec workshop on attractiveness of the microelectronics business with a student focus group at Grenoble INP-UGA. © *P.Jayet/CEA*

Learning community to tackle challenges of responsible microelectronics

Sustainable electronics for smart buildings

In 2022, Nanoelec's Human Capital and Training Design program once again designed and implemented a new training module on sustainable electronics with Grenoble INP-UGA and Grenoble Ecole de Management (GEM). For two half-days, about 60 students from the Grenoble ecosystem as well as Erasmus European exchange students, worked hand-in-hand with professionals from STMicroelectronics, Akileo Formation, CEA and members of association Think What Matters.

Interview with **Panagiota Morfouli,** professor at Grenoble INP-UGA and co-director of Nanoelec/ Chif.

What design challenges do training programs in sustainable electronics involve?

Our students tell us that, more than ever, they search for meaning in their jobs; they are looking for jobs that make a real contribution to society. We must therefore adapt our training offers to this new demand. This is what we have been doing for the past three years within the Nanoelec Human Capital and Training Design program: developing different modules that include a sustainable approach.

What are the expectations of your industrial partners?

The microelectronics industry has a longstanding commitment to reducing its environmental impact across the entire lifecycle of products. Our partners are convinced that microelectronics engineers and managers must take action at their own level, both as experts with highly specialized skills and as responsible citizens, to control the impact of technologies, create new "eco-friendly instincts" and help reduce humanity's overall environmental footprint.

The module essentially consists of a two-step workshop. What is the outline of the educational program?

A first session sheds light on various technical aspects concerning the environmental impact of microelectronics. We are working on eco-design concepts through a method that consists of integrating environmental parameters into the design and implementation of a manufacturing process.
The workshop also aims to develop cross-cutting skills, for example by leading future engineers or managers to understand the complexity of the world and its scientific, ethical and political dimensions. This will help them to become drivers of real change in attitudes and behaviors by proposing new approaches and ways of working on the issues facing their company.

How are you initiating a real educational change?

With this type of module, our students begin their semester by thinking about the future; they are encouraged to get involved, to become a driving force for global change. It is also an opportunity to work directly with industry experts who share their experience and guide them in their thinking.

This was the third session of the sustainable microelectronics workshop. What are the main focus areas?

After addressing the topic of a green smartphone and its lifecycle in 2020 and 20216, the 2022 event was dedicated to IoT for smart buildings[7]. → 118

6. Morfouli, Y., Christou, M., Prejbeanu, L., & Fourmanoir, M. (2022, January 19). Atelier—Défi : Vers une microélectronique durable. Colloque "Questions de pédagogies dans l'enseignement supérieur", *La Rochelle, France Janvier 2022 https://qpes2021.sciencesconf.org/358956*

7. A smart building is a structure that utilizes advanced technologies and automation systems to enhance its efficiency, functionality, and sustainable development. These technologies enable the building to collect, analyze, and utilize data to improve overall building performance and user experience.

Fifty-four students were split up into six groups and, with the help of our experts, each group worked on different technical topics based on an initial scenario: transforming an office floor into a "smart floor" by using IoT technologies to cut energy costs (while reducing the overall carbon footprint), and improving employee safety and comfort.

The 2022 module focused on the design of a smart, adaptable and connected building. Could you give us the main lines of the scenario?

It read as such: "You are employees at Green IoT for Smart Buildings. As part of the construction of a new office building, you must recommend a prototype for the use of new technical services for management and for occupancy rate monitoring (optimize room occupancy and the quality of the environment, anticipate energy consumption, etc.). You must integrate the use of artificial intelligence (AI) (powerful neural network embedded on a microcontroller) as much as possible in order to manage IoT data (thermal, optical, chemical sensors)".

What surprised you in the final outcome? What stood out?

The students felt like real engineers and managers, faced with practical problems similar to those found in the real industrial world. We were struck by the quality of the discussions and the teamwork. They were highly motivated and committed, and they took a very pragmatic approach to the problems in order to design and implement real action plans.

What happened after the workshop?

A month after the workshop, the six-student group who placed first was able to visit and truly appreciate the 1000+ Solutions for Cities exhibition created by the Solar Impulse Foundation and Schneider Electric. The event focused on energy, buildings, waste, production and consumption, mobility and infrastructure.
And as a result of the ideas that emerged during the workshop, a second group, very keen to learn about the challenges of smart buildings and the contributions that microelectronics technology can make, decided to work throughout the entire semester on a project entitled "IoT for smart buildings", with the help of start-up Akileo Formation.

"THE DIRECT FEEDBACK FROM STUDENTS HAS BEEN A REAL MOTIVATION FOR SUSTAINABLE DEVELOPMENT ISSUES. OVER AND ABOVE THE TECHNICAL SKILLS, SINCE WE ARE LOOKING FOR NEW HIRES, WE APPRECIATE THEIR INVOLVEMENT IN DEVELOPMENT, ECOLOGY ISSUES, AND THEIR ABILITY TO INNOVATE IN THIS FIELD, TO SEE ENVIRONMENTAL ISSUES DIFFERENTLY FROM THE PREVIOUS GENERATION."

© Grenoble INP-UGA

Eric Jouseau, co-founder of Akileo Formation and Ace-WithYou, during the all-new "Sustainable electronics/Smartbuilding" session of the Nanoelec/CHIF program, in February 2022.

© DR

During this workshop, we showed them the means and tools they can use. We saw highly creative solutions; it's a very important point in terms of innovation. You have to "think outside the box" and explore all possible ideas in this field."

"DURING THEIR CAREERS, EACH OF THESE STUDENTS WILL BE AN ENVIRONMENTAL PLAYER."

Thierry Fensch, Innovation & Collaborations Director, STMicroelectronics Grenoble, during the all-new "Sustainable electronics / Smart building" session of the Nanoelec/CHIF program, in February 2022.

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A serious game testing session at CHIF program. © *P.Jayet/CEA*

↑
Group of studens working on attractiveness of the microelectronics business. © *P.Jayet/CEA*

Dall.e/open AI tool built a view of a classroom for engineer students learning electronics. Why does the AI understands 'student classroom' as a messy place?

© *Created with Dall.e/Open AI in digital art style.*

SUSTAINABLE DEVELOPMENT

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Sandrine Maubert, Deputy Director of Nanoelec

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For sustainable competitiveness in the electronics industry

New ways of questioning our processes.

Inspired by its industrial partners, Nanoelec is active in four work areas in line with the United Nations' framework for sustainable development goals.

We conducted in 2022 an R&D Life Cycle Assessment (LCA) for a new display manufacturing process under development at Nanoelec. At the same time, in conjunction with Minalogic, we are evaluating and setting up a fast-diagnosis methodology to help SMEs assess the societal and environmental impact of their innovation projects. We are also working on human capital and skills by building a full range of training modules for sustainable electronics. And finally, in spring 2022, we launched our first ever competition for women in technology research. Even if our major areas of focus remain technological, we are fully aware that to be competitive, industries must properly manage their environmental and societal impact.

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Four work areas for sustainable development

In 2021, after a survey seminar in November 2020, Nanoelec launched a number of cross-cutting work areas in sustainable development, in response to the recommendations that accompanied the decision for further funding.
The Nanoelec Sustainable Development action plan comprises four work areas.

Two of them concern **eco-innovation for R&D projects:**

- A quick and inexpensive diagnostic solution for companies looking to run a project within the Easytech framework;

- An eco-innovation tool in the R&D phase for the new-generation display production sector, currently under development with Aledia as part of the Displed program.

Two of these work areas concern **management, skills and governance:**

- Events to promote greater gender equality in the electronics sector;

- Design of training courses for sustainable electronics, through the Human Capital and Training Design program.

Running R&D projects and eco-innovation

As a result of the ongoing trend in Europe and France for a circular economy, companies are adopting sustainable innovation and eco-innovation concepts, which take into account economic, environmental and societal aspects[1].

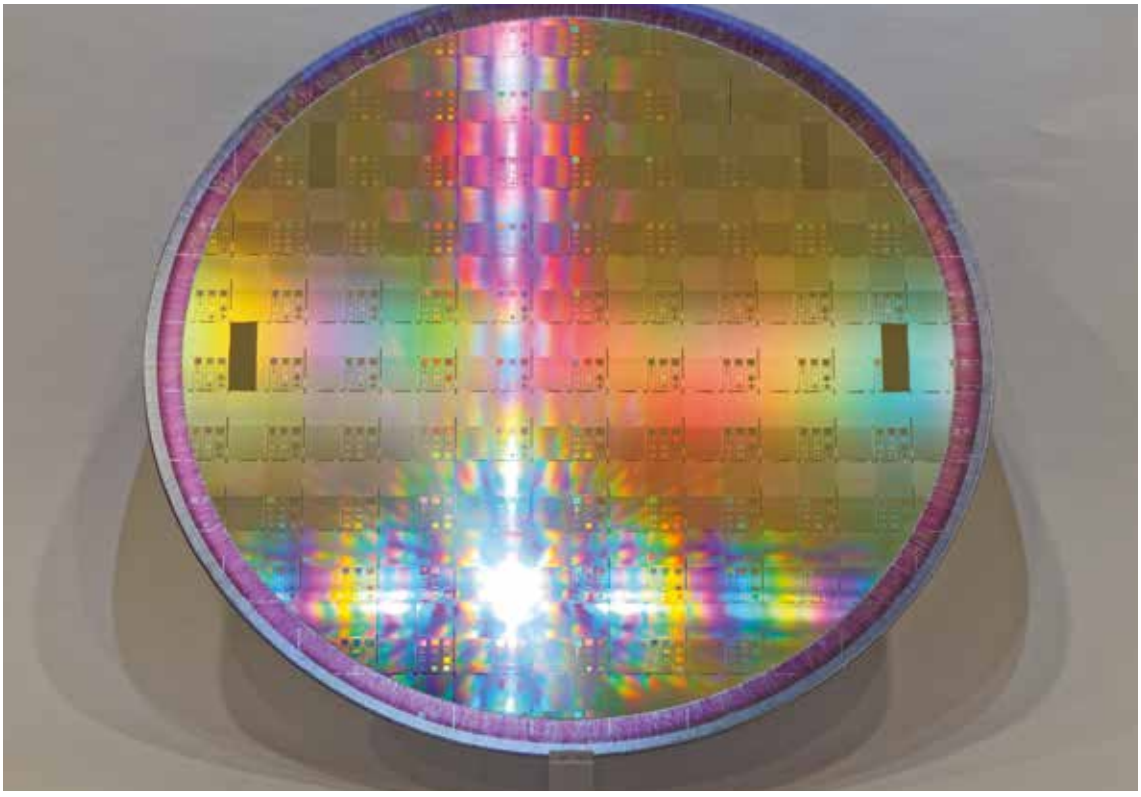
The explicit and legible incorporation of these concepts is also becoming a strong factor in competitiveness for companies. To address these issues and the requirements of the Secrétatiat General Pour l'Investissement (SGPI), Nanoelec has committed to two specific projects: Defi-Ino and Ecodispled.

Quick diagnostic for Easytech: Defi-Ino

In close collaboration with Minalogic and Grenoble-INP/Esisar, IRT Nanoelec launched the Defi-Ino project in 2021[2]. It entails developing an "eco-innovation" type diagnosis for companies such as SMEs, mid-caps, and start-ups, and launching an innovation project with the expertise of one of the two institutes. The proposed diagnostic is quick and inexpensive. It does not replace an actual environmental assessment, nor a life cycle assessment (LCA). Instead, it aims to be a simple evaluation, which could encourage companies to commit to a more detailed study and to change their environmental responsibility culture.

1. For example, see the impact assessment of the Act on combatting waste and on the circular economy adopted in 2020 https://www.legifrance.gouv.fr/contenu/Media/Files/autour-de-la-loi/legislatif-et-reglementaire/etudes-d-impact-des-lois/ei_art_39_2020/ei_trep1902395l_cm_10.07.2019.pdf

2. The project was initiated in conjunction with Ines.2S Energy Transition Institute (ITE).



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Micro-LEDs GaN on Silicium for high illumination screens. The optimization of the targeted industrial process might start right from the R&D stage. *© Y.Lee/CEA*

In 2021, the process was determined during a pilot phase. It was explained in detail in the 2022 Nanoelec Highlights public report.

In 2022, a questionnaire (survey) was included in the Easytech labeling application file. It will allow the experts of the labeling committee to evaluate:

- the awareness of the company, and its consideration for the environmental impact of the activity and the project;
- the eco-innovation maturity of the product and the company.

Eco-design in the R&D phase: Eco-Displɛd

In parallel with the R&D actions of the Displed program, Nanoelec launched an R&D phase for an eco-design project, in close coordination with Aledia. LCA tools are available, although they require a stabilized production framework and access to large volumes of data. The aim of the project is to implement an eco-design tool in an R&D phase, adapted to an immature sector, and devoted to Smart Pixel technology for the production of new-generation displays. The tool can be used to evaluate the environmental gain from innovative solutions regarding choice of materials, components or procurement routes, and compared with a reference process[3]. •

3. Addressing needs in electronics will entail adapting a method and a tool already developed by CEA-Liten for photovoltaics. See details in the Displed section of this report.

Management, skills and governance

Sustainable development is built on two pillars: on the one hand, protecting the environment and, on the other, protecting humankind.

Gender equality is one of the 17 United Nations sustainable development goals to be achieved by 2030.

Employment in the microelectronics sector is under stress. Attracting talent, both men and women, is a real challenge. Students and professionals in the sector are looking for meaning and values. To hire and retain personnel, the players in the sector such as STMicroelectronics, Schneider Electric, Siemens EDA and CEA have implemented initiatives built around sustainable development and human resources.

"NANOELEC IS MEMBER OF THE NATIONAL NETWORK 'FEMMES INGÉNIEURES' AND KEEPS A CLOSE WATCH ON INITIATIVES…"

Nanoelec is member of the national network 'Femmes ingénieures' and keeps a close watch on initiatives carried out by other networks line Women In Engineering Society (UK), Cercle Inter'Elles (FR), Nanoelec edits a bimonthly newsletter providing a lot of information for opportunities to meet actors of these networks. •

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Nanoelec, CEA-Y.Spot and Giant organization gather managers women for a special event as a round table on March 8th, 2023, live in Grenoble.

© P.Jayet/CEA

Every year, Nanoelec organizes or co-organizes round tables and events for international days: Women Rights, in march, Women In Engineering, in june.

© Jayet/CEA

HR, diversity, inclusion, workplace parity and equality

The approach adopted by Nanoelec to address workplace parity and equality was initiated in accordance with proposals by a few representatives of our Steering Committee.

Following this commitement, the managment team of the institut took a number of pragmatic and operational steps. We took into account Nanoelec's particular status: it does not have its own legal identity and therefore cannot represent the employer. The steps are designed to foster discussion between consortium partners, and ensure a gradual creation of a collective culture on the subject.

At its tenth anniversary (2022), Nanoelec organized a contest to promote the role of women in scientific research, to shed light on role models for future generations, and enhance the attractiveness of the industry.

The contest uses a comprehensive approach to highlight candidate profiles, and an action plan to make their careers known across a wide range of communication channels; radio, middle schools and high-schools, and webinars. The initiative has sparked interest in decision makers from several Nanoelec industrial partners, who have decided to sit on the jury panel. •

"TO MARK ITS TENTH ANNIVERSARY, NANOELEC ORGANIZED A CONTEST TO PROMOTE THE ROLE OF WOMEN IN SCIENTIFIC RESEARCH, TO SHED LIGHT ON ROLE MODELS FOR FUTURE GENERATIONS, AND ENHANCE THE ATTRACTIVENESS OF THE INDUSTRY."

Training in Engineering

Several initiatives within the Nanoelec/ Human Capital and Training Design program have helped to strengthen the sustainable development culture, and the skills of the sector's current and future professionals. They are detailed in the CHIF program chapter. A quick overview is given below.

Experiential learning programs

ABC Stories
The ABC Stories program focuses on innovative solutions that use image sensors built with artificial intelligence. Four courses, based on DSRM methodology (Pfeffer et al., 2007) and an experience-based co-design process (Leclercq et al., 2014), have been developed or are in the final development stage. The premise: How to understand and have influence on sustainable adoption intentions for connected solutions?

Piste
The program gives engineering students an idea of the challenges that sober and sustainable technological innovation projects involve. Students have to bring together local companies in order to offer global solutions that will ensure a energy efficient and sustainable approach throughout every project management stage.

Learning community to tackle emerging challenges of responsible microelectronics

Estim
The program's goal is to use AI in order to promote energy efficient solutions through eco friendly habits, business models that ensure access to energy for underserved populations (refugee camps), and funding conditions for SMEs in photovoltaics.

The environmental & societal impact of a company project
Nowadays, engineers have a dual responsibility towards society: they must be knowledgeable in increasingly advanced technologies, and mitigate the global risks generated by their business activities. For these reasons, 35 students from the Nanotech international Master's program focused on the overall environmental and societal impact of a project during their internships in a company or a laboratory. •

Attractiveness of the microelectronics industry

As a consortium of different actors, in 2022, Nanoelec started to implement answers to the new candidate shortage problem, both in training and on the job market.

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May 11, 2023: territorial forum for the attractiveness of the microelectronics industry. © *P.Jayet/CEA*

In 2023, several webinars were organized, and two large workshops involved Nanoelec partners (March 2), and the microelectronics community[4] in the Grenoble area (May 11).

Striving to move beyond the observations regarding tensions and the inventory of initiatives, the work focused on two themes:

- **training:** from awareness-raising among schoolchildren, to training for technicians and scientific and non-scientific executives (management, marketing, innovation through use), including retraining;
- **recruitment** (promotion of offers, company images, lifestyle, recruitment cycle, soft landing, recruitment forum and events).

More than 30 initiatives, from local actors to international network of stakeholder in microelectronics business, were presented on the place during the forum for attractiveness, May 11, 2023, with more than 150 attendies. •

4. Including state, local authorities, public services, national education, higher education and research, industry.

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Pascal Metzger, CEO of SET (right), and Stephane Berthier, Head of HR developement at STMicroelectronics (left), on May 11, 2023 at the territorial forum for the attractiveness of the microelectronics industry.

© P.Jayet/CEA

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Some of the nominees and winners at the award ceremony on December 13, 2022. © *Tresca/CEA*

Thirteen inspiring women in technological research

Thirteen nominees were chosen by their coworkers. All nominees have made significant contributions to Nanoelec in the past ten years.

In conjunction with its tenth anniversary, Nanoelec organized, in 2022, a competition for women in technological research. Nominators had to ensure approval of the nominee's application, and help the nominee prepare their presentation before the jury panel, this coworker support was particularly important. To symbolize the multi-partner approach that characterizes the institute's way of working, we strove to involve a wide range of participants from different partners.

By organizing such a contest, the Nanoelec general management intended to promote the role of women in scientific research, to shed light on role models for future generations, and to enhance the attractiveness of the industry.

"It was not simple to get candidates", noted Sandrine Maubert, Nanoelec Deputy Director. "*When we talked to certain coworkers, who either have a scientific background or otherwise, their first reaction was: "Can I legitimately claim to deserve such an award?" Once we explained the vital need to empower women in technological research, they gradually accepted, even though they took on the role of ambassadors rather than contestants."*

"To symbolize the multi-partner approach that characterizes the institute's way of working, we strove to involve a wide range of participants from different partners", added Sandrine Maubert. A jury panel, tailored to the contest's 13 candidates from seven strategic Nanoelec programs, was made up of nine renowned figures.
On June 23, 2022, at Grenoble-Ecole de management, each candidate gave a three-minute presentation to the jury panel. They described their job at Nanoelec and the contributions they have made.

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"ON DECEMBER 13, 2022, DURING THE GENERAL ASSEMBLY THAT MARKED NANOELEC'S TENTH ANNIVERSARY, ALL THIRTEEN CANDIDATES, INCLUDING THE THREE PRIZEWINNERS, RECEIVED A TROPHY."

They were also asked to convey a message to young generations encouraging them to follow their own path.

↑
The trophies were designed by Woodalpine, a startup association in Grenoble.
© Legrand/CEA

"We are used to talking for 20 minutes or even an hour in front of a group of coworkers; talking about yourself for three minutes straight, is a whole other story", proclaimed one of the nominees.

On December 13, 2022, during the general assembly that marked Nanoelec's tenth anniversary, all thirteen candidates, including the three prizewinners, received a trophy5. The awards were made out of wood, a material that symbolizes the environment; the discs' 300mm diameter is the standard size of silica discs used in component-producing plants. A small silica plaque affixed to each trophy served as a reminder of the materials used in our industry. Nominees received cube-shaped awards; the three winners received discs. •

5. Trophies were designed by Woodalpine, a startup association in Grenoble, which employs people in return-to-work schemes. The drawings on the awards symbolize the regular patterns on silica electronic circuits, and the crystal lattice of mineral materials.

NOMINEE	NOMINATOR	NANOELEC PROGRAM INVOLVEMENT
Lucile Arnaud (CEA)	**Alexis Farcy** (STMicroelectronics)	*3D*
Gaelle Del Rey (CEA)	**Bruno Charrat** (CEA)	*Pulse and institute management control*
Emmanuelle Feltrin (Minalogic)	**Elvir Mujic** (Minalogic)	*Easytech*
Manon Fourmanoir (UGA)	**Ennio Caria** (ESRF)	*Training/Carac*
Magali Grégoire (STMicroelectronics)	**Fabrice Nemouchi** (CEA)	*Photonics*
Nadine Guillemot (UGA)	**Karim Chibane** (Grenoble-INP)	*Training/Easytech*
Christine Hennebert (CEA)	**Amélie Favreau** (UGA)	*Pulse*
Eva Kempf (STMicroelectronics)	**Sylvain Guerber** (CEA)	*Photonics*
Manon Letiche (ILL)	**Youla Morfouli** (Grenoble-INP)	*Carac/Training*
Radolslava Mitova (Schneider Electric)	**Jean-Luc Schanen** (Grenoble-INP)	*PowerGaN*
Andrea Quintero (Soitec)	**Philippe Rodriguez** (CEA)	*Photonics*
Lee Wang (Siemens EDA)	**Jean-Marc Talbot** (Siemens EDA)	*3D*

Nanoelec for women in technological research: panel members

- **Anne-Sophie Hajjar** (Schneider Electric), *panel president*
- **Alain Fontaine** (CNRS and French Society of Physics)
- **Flore Gouaux** (Siemens EDA)
- **Adrian Ionescu** (EPFL)
- **Sandrine Maubert** (Nanoelec)
- **Jean-Eric Michalet** (Minalogic)
- **Florence Robin** (Limatech)
- **Valentina Vetere** (CEA)
- **Hélène Wehbe-Alause** (STMicroelectronics)

INCREASINGLY INVOLVED IN EMBEDDED ARTIFICIAL INTELLIGENCE

Nanoelec tackles the topic of artificial intelligence (AI) from the perspective of embedded electronics. The development and expansion of embedded AI applications is triggered by the generation of large amounts of data that require local processing at component and system levels.

The aim is to provide these components with the ability to make decisions in a more decentralized, autonomous and reliable manner. Therefore, processing must be integrated close to the sensor in order to optimize the flow of data and to ensure that it remains undamaged and confidential. This allows a good trade-off between data flows from the sensor to the user and the related energy footprints of both the sensor and the central computer handling reduced amounts of data.

Digital Trust

Future connected objects will need reliable implementations of embedded AI algorithms and security mechanisms to protect them from potential software and hardware threats. The safe deployment and use of this technology in embedded systems requires securing the implementation of AI algorithms within these objects, as well as their communication protocols with the outside world. Researchers from academic laboratories and industrial teams are working together within the Nanoelec/Pulse program to implement and deploy AI algorithms, in particular machine learning algorithms embedded in IoT components.

With regard to the safety of autonomous vehicles, program teams are focusing on the validation of AI systems for mobility/vehicles. The issue of evaluating and validating the effectiveness of these technologies is one of the last central barriers holding back the adoption of embedded context capture technologies. Technological research in this area is therefore a major challenge for access to the autonomous vehicle market. •

Smart Imagers

Imaging is one of the three main fields that use AI. The aim is not only to achieve better image quality, but also to extract relevant data from the image, taking account of the environment, the object and the scene (potentially across a range of lighting conditions), and knowledge of the context. The main objective of the Nanoelec/Smart Imager program is to evaluate the advantages of using 3D-stack technology to integrate the processing of artificial intelligence into the third layer of an image sensor.

The research teams are focusing on developing generic AI building blocks and the associated processing as well as on exploring the impact of these blocks on low-energy imager architectures. •

Training design

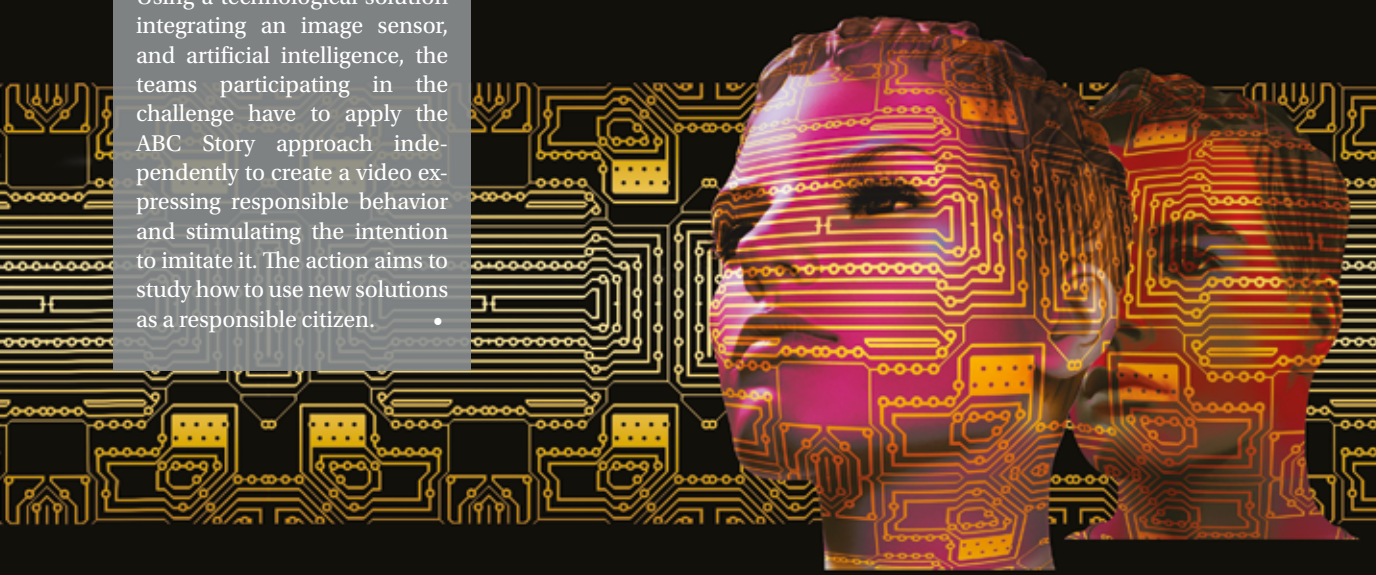
In collaboration with the MIAI institute (Idex Université Grenoble-Alpes), the Nanoelec/Chif program developed and digitalized the module entitled "Introduction to embedded artificial intelligence". Design of the module was done in 2021. It has been tested in Elise plateforme in 2022. The learning capsule contains theory and test sequences in the form of short videos. It is aimed at student in engineering or management curricula as well as professionals fromthe microelectronics industry. It introduces the learners to embedded artificial intelligence (for example, image recognition or identification of spoken keywords) and is able to qualify and quantify the limits of this technology.

2022 was also the time for the Mission ABC capsule dedicated to a public audience. Using a technological solution integrating an image sensor, and artificial intelligence, the teams participating in the challenge have to apply the ABC Story approach independently to create a video expressing responsible behavior and stimulating the intention to imitate it. The action aims to study how to use new solutions as a responsible citizen. •

Application demonstrators for imagers

Teams involved in the Nanoelec/System Lab initiative define, develop and test cases using embedded AI technologies that are integrated into or associated with image sensors.

The project aims to develop functional demonstrators and explore new applications scenarios. Merging the data from optical sensors is based on artificial intelligence solutions in order to exploit the pertinent data. AI is usually developed specifically for the given use case. The System Lab teams are looking to identify the generic added value of AI, independently of the use cases. •



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ENGAGEMENT IN THE EUROPEAN R&D SPACE

Nanoelec has taken part in 28 European projects since 2012. Eleven are ongoing in 2022.

Photonic Sensors

Cytometry

CEA-Leti and Prophesee, both partners in the Nanoelec consortium, are taking part in the Neoteric project. The Neoteric partners are aiming to develop a reconfigurable photonic circuit to detect cancer cells in a solution (cytometry).

https://neoterich2020.eu/

Transceivers (embedded transmitter+receiver)

The EU Masstart project will lead to the production of several Datacom and Telecom demonstrators. It focuses on the development of advanced packaging and test methods for producing very high speed transceivers (800 Gbps and 1.6 Tbps), with reduced form factors (COBO type). CEA-Leti and Almae, partners in the Nanoelec consortium, are contributing to this project. A first generation of circuits was produced using the Silphide Design Kit developed within Nanoelec, and used by the partner Bright Photonics in its Nazca tool.

https://masstart.eu/

Neuromorphic computing

The European Prometheus project aims to manufacture a complete neuromorphic computing chip (set of interferometers using low-consumption BTO-based phase shifters for the synaptic part and pulsed lasers integrated on silicon for the neural part). The work in 2022 focused on the design of the first circuits and the first prototype BTO phase-shifters and pulsed lasers, targeting start of manufacturing in early 2023.

Characterization

Nanomechanical materials characterization in industry

NanoMECommons is an H2020 collaborative project focusing on the development of new characterization methodologies tailored to industrial needs in the nanomechanical field. The ESRF is in charge of developing a deformation microscope to be installed on ID01 to complete a suite of instruments which also includes a Raman spectrometer reconditioned with the support of Nanoelec, which will be included in the Nanoelec/PAC-G offering. This tool will support research activities in band-gap design for various microelectronics applications, in particular the study of new materials and substrates for optoelectronic devices.

https://www.nanomecommons.net/

Addressing key bottlenecks in nanoscience research

NFFA (Europe's Nano Foundries and Fine Analysis Pilot) is an H2020 collaborative project which prefigures the first distributed research infrastructure within the EU, offering access to high-level instrumentation in the field of nanosciences and nanotechnologies. Within the NFFA consortium, IRT Nanoelec provides access to the ESRF/BM05 synchrotron beamline.

https://www.nffa.eu/

Exploring radiation effects for industry and research

Radnext (for RADiation facility Network for the EXploration of effects for indusTry and research) is an H2020 collaborative project aiming to launch a distributed research infrastructure within the EU devoted to the industrial and university irradiation community. The projet coordinator is Cern in Switzerland. The consortium houses a range of equipment/installations offering time on different beam families for electronic components. The available beams are: heavy ions, protons, neutrons, lasers, X-rays, electrons, gamma radiation. The collaborations with industry are coordinated by the ESRF, which also heads a Committee of industrial advisers. The Nanoelec/Characterization program teams (ESR, ILL and Iroc Technologies) are involved and will concentrate on harmonizing the initiative with the operations to launch the Irradiation competence center.

https://radnext.web.cern.ch/

Pulse

Digitizing SMEs

DigiFed is run by Nanoelec through its founding partners, CEA, STMicroelectronics and Minalogic. The aim is to demonstrate the potential of digital technologies in terms of hardware security, human-machine interaction, and autonomy for small and medium enterprises.

DigiFed involves nearly 200 European SMEs in its innovation program. 80 of them can receive financial support and benefit from one of the DigiFed innovation channels. Half of them will be companies initiating their digital transformation. The projet was shut down in 2022.

https://digifed.org/

Artificial intelligence of objects

The European InSecTT (Intelligent, Secure, Trustable Things) project is an ECSEL (Electronic Components and Systems for European Leadership initiative) project, in which the participants include CEA and STMicroelectronics, within Nanoelec. InSecTT aims to combine the Internet of Things (IoT) with Artificial Intelligence (AI) by building trust in AI-based smart systems and solutions, which constitute a significant part of the concept of the artificial intelligence of things (AIoT), which is the natural evolution of AI and the IoT.

The projet comprises 52 partners (12 nationalities) and is coordinated by Austria (Virtual Vehicle). The project began on 15 June 2020 and will last a total of three years.

https://www.insectt.eu/

Secure IoT for agriculture

To meet the needs of agriculture, the H2020 Sarmenti project is developing in-situ, real-time solutions to measure the various nutrients present in the soil and the gas emissions just above the soil, in order to improve management of natural or chemical fertilizer inputs, to maximize crop growth, minimize environmental losses and thus reduce the pollution linked to poor fertilizer management.

The Pulse program at Nanoelec, which more particularly involves CEA and STMicroelectronics, provides solutions to secure sensors in IoT mode against side channel attacks. Open-field experiments are ongoing in France, Romania and Ireland.

https://sarmenti-project.eu/

Post-quantum encryption (PQC) and quantum key exchange (QKD) against crime

In conjunction with the French Ministry of the Interior, the CEA is studying the interest of the Post quantum Cryptography (PQC) for the needs of the European Poliiice project associated with the Nanoelec/Pulse program and launched at the end of 2022.

The aim of Poliiice is to enable European local authorities to make progress in lawful interception, investigation and intelligence to effectively prevent, detect and investigate crime and terrorism, drawing in particular on our skills in post-quantum encryption (PQC) and quantum key exchange (QKD).

https://poliiice-project.eu/

Embodied AI/Robotics Applications for a Safe, Human-oriented Industry

The Horizon Europe EARASHI (Embodied AI/ Robotics Applications for a Safe, Human-oriented Industry) project was launched in September 2022 and will support European start-ups and SMEs in adopting advanced eco-friendly digital technologies (in particular AI, data and robotics) to help workers in their day-to-day activities and improve their working conditions (security, health and well-being) eventually leading to productivity gains.

https://earashi.eu/

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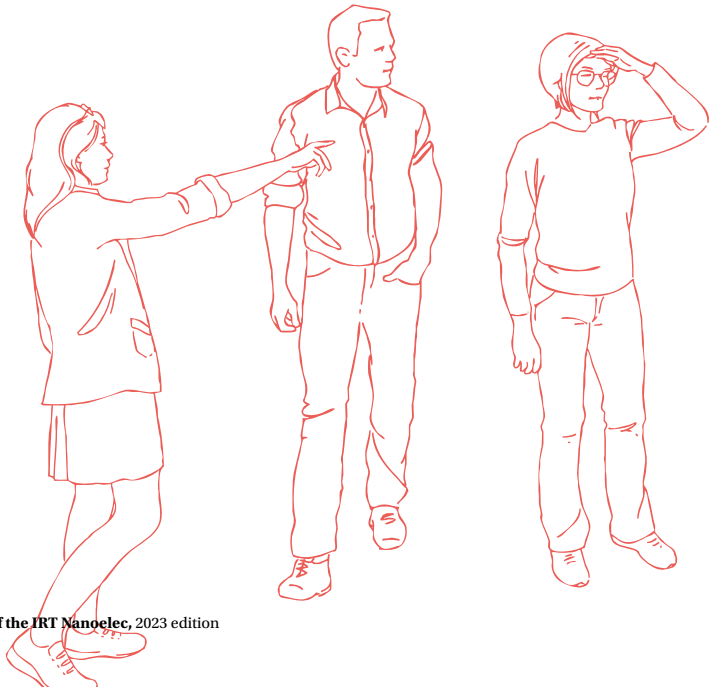

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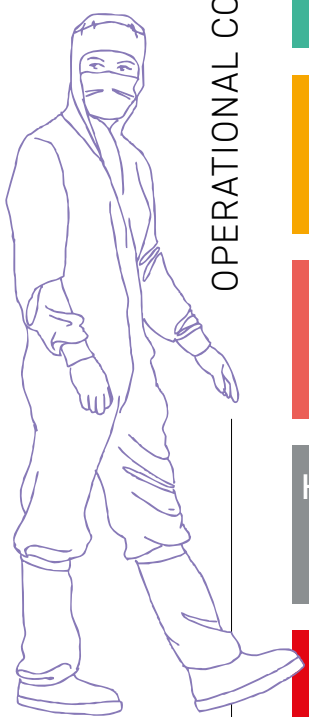

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