

ICs and sustainability: Image sensors case study

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Growing impact of smartphone image sensors

Around 1.4 billions smartphones produced each year





Life Cycle Analysis (LCA)

Fabrication

ESOS



Increased number of sensors → more silicon surface In the meantime, silicon area of SoC remains stable



Model for use phase

Use phase accounts for the electrical energy used during image capture (Use power) and when the device is powered up but not in use (Idle power).

The GWP is determined by the total energy consumption of the device, which is then weighted according to the energy mix specific to the location where the device is used.

$$G_{Use} = T_{loc}(P_{Use}t_{Use} + P_{Idle}t_{Idle})$$

Electric carbon intensity

-	IVIIII.	тур.	Max.	Unit
I _{ANA}		62.8	65.5	mA
I _{DIG}		257.8	356.0	mA
l _{IF}		2.2	2.7	mA
I _{STBANA}			2	μA
	Iana Idig Iif Istbana	I _{ANA} I _{DIG} I _{IF} I _{STBANA}	IANA 62.8 IDIG 257.8 IIF 2.2 ISTBANA	IANA 62.8 65.5 IDIG 257.8 356.0 IIF 2.2 2.7 ISTBANA 2 2

Results

Total GWP for scenarios with the same sensor:

- security camera active 24/7
- smartphone camera active 15min/day
- \rightarrow G_{Use} is negligeable for smartphones sensors.

For devices that remain continuously active: → the local energy mix has a significant impact.



at the use location kgCO²e/kWh)

Excernt from IMX576 datasheet						
Standby current (IF)	I _{STBIF}			1	μA	
Standby current (digital)	I _{STBDIG}			158	μA	

Model for fabrication phase

Scarce data from semiconductor manufacturers Public information in databases and publications:

- impact with more advanced technologies.

- Proportional to **silicon area**





Fabrication impact of sensors with similar characteristics, constructed in different locations \rightarrow influence of the <u>energy mix at the factory</u>.

The incorporation of 3D stacking technology amplifies GWP of the device by more than double.

For context, the estimation from Fairphone 4 LCA is 3.6 times lower for the same sensor.



	IMX 582	VD1940
Vendor	SONY	ST Microelectronics
Fab location	Japan	France
Silicon area per layer	34mm ² (est.)	35mm ²
Node 1 (sensor)	65nm	65nm
Node 2 (logic)	45nm	45nm

Rise of 3D technologies and global warming

3D stacking technologies increase the total silicon area of an integrated circuit.

Same apparent package size, but multiple times the impact compared to 2D devices.

Example: Flash storage Ics:

Source: Hitachi 9X layer 3D NAND flash memory (2020)



Carbon footprint of SSDs relative to their capacity

10 ³			
	*	HP	
	^	1.11	
		N 4 '	28.
	*	MICrosoft	0.12
			IPEU

Excerpt from IMX576 datasheet



Advanced sensors use stacking of 2 dies:

- Sensitive surface (pixels) on the top
- Control and processing below ۲
- → Twice the carbon footprint per surface unit







Bonding connections

> Streamlined Models of CMOS Image Sensors Carbon Impacts Olivier Weppe, Jérôme Chossat, Thibaut Marty, Jean-Christophe Prévotet, Maxime Pelcat DSD Conference 2024

https://hal.science/hal-04632499

