From imaging to visioning

Providing relevant and real-time environment analysis by vision.

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ERIC OLLIER, DIRECTOR OF THE NANOELEC/ SMART IMAGERS PROGRAM

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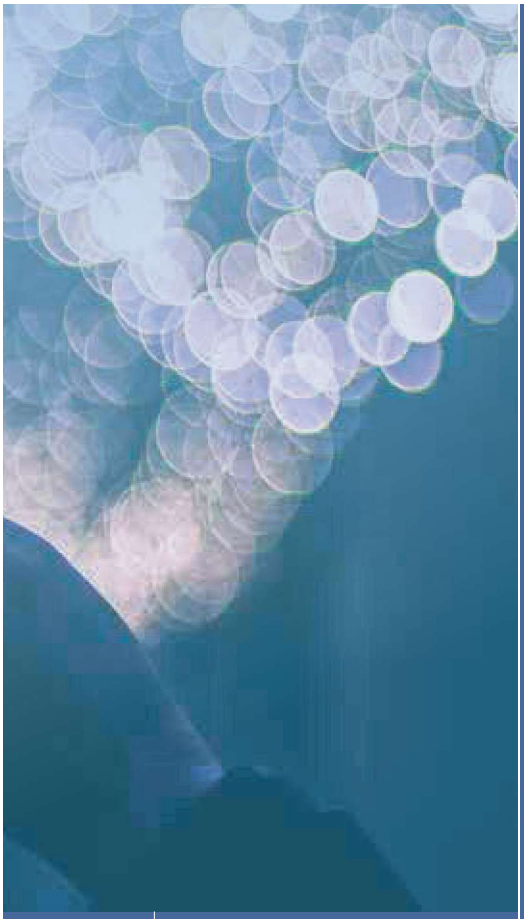
Within the Nanoelec/Smart Imager program, our aim is to develop the technologies needed for the next generation of imagers, which will enable the transition from capturing images to exploiting the information they contain. This exploitation will be performed by the sensor itself, so that it can perceive a scene, understand the relevant situation and intervene on it.

This is a truly disruptive paradigm shift, with the focus shifting to computing and memory challenges, in addition to image generation. The concept includes the implementation of artificial intelligence within the image sensor itself.

In 2024, work continued on developing the key technological building blocks: hybrid bonding, HD-TSV, heterogeneous integration and specific technologies for infrared applications. The development of a "dual damascene" structure is ongoing to improve the hybrid bonding connection. This reduces the number of interfaces between the various levels and thus the total resistance of the interconnections in the 3D stack. Numerous technological improvements have been made to the HD-TSV and have boosted their maturity, while continuing with the scaling roadmap.

Activity to develop heterogeneous integration technologies based on D2W approach grew this year, with the design of a new set of complex masks which will enable interconnection pitch reduction along with the development of different integration architectures. Finally, in-depth study of the use of 3D technologies for IR imager applications led to start developments based on D2W technologies in order to allow access to advanced 300mm CMOS technologies.

New integrated circuit design methodologies are being implemented to meet the two-fold challenge of introducing AI computing functions as close as possible to the sensors. The two design •••



platforms created in 2023 evolved in 2024 with the addition of new CAD design tools, thus completing the design stream for smart imagers.

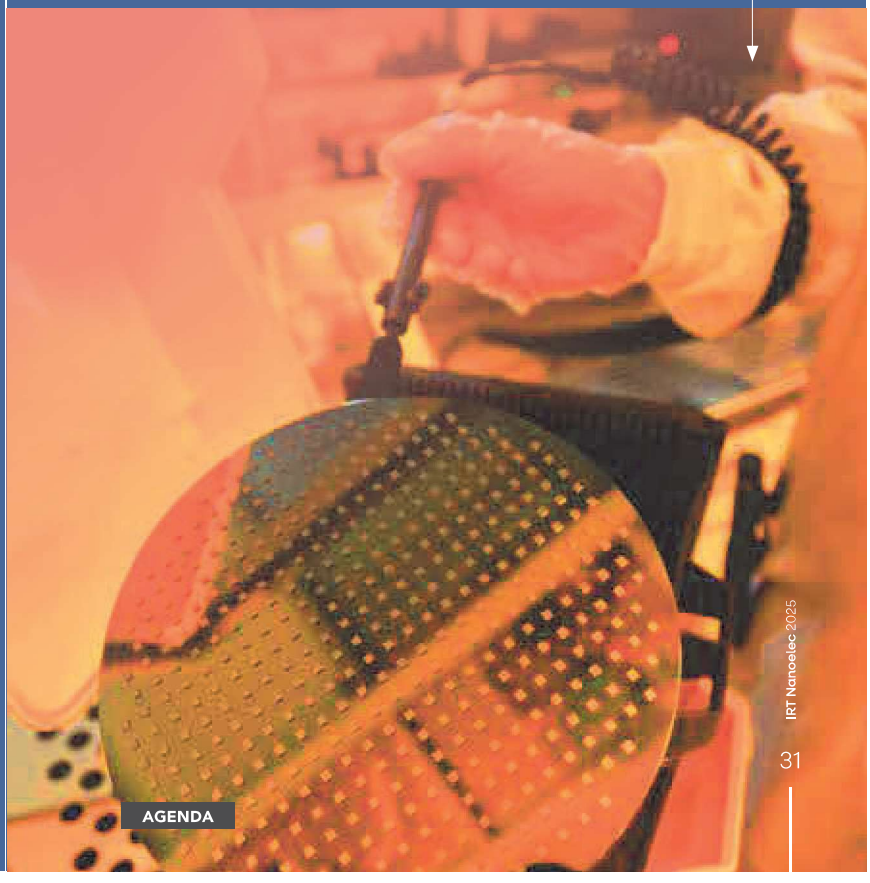
Our 3D multi-layer integration technology is progressing in terms of maturity and electrical performance: significant technological improvements have been made, integration efficiency has been improved, and more and more wafers are being completed, with improved morphological and electrical characteristics. With regard to electrical performance, the resistance values of the three-layer stack have been reduced and the electrical isolation at HD-TSV level has been significantly improved.Thanks to joint work by CEA and STMicroelectronics, the process design kit (PDK) including the HD-TSV contributions is moreover, place and route process has also been optimized to enable precise 3D design in order to meet performance requirements.

Finally, based on all these developments, 2 functional 3-layer smart imager demonstrators were studied under the program: one called J3DAI is virtual, and the other called EB3D/Tanzanite is slated to reach silicon demonstration level in the coming years. The first one intended for visible applications is based on an STMicroelectronics pixel with an AI accelerator from CEA, while the second one intended for event-based applications is based on a pixel designed by Prophesee. An innovative AI part (GNN) was developed by CEA and Prophesee, with the whole scheduled for manufacture in the STMicroelectronics and CEA cleanrooms. •

SMART IMAGER PROGRAM AT A GLANCE

- **Vision**
  The transition from imagers to vision sensors is generating new market opportunities
- **Ambition**
  To provide key HW and SW building blocks, to validate them through demonstrations ranging from test vehicles and proofs of concept to the prototyping of a smart, multi-layer imager
- **Mission**
  Stacking/3D technologies, embedded AI and data management, new architectures
- **Partners**
  CEA, Lynred, Prophesee, Siemens EDA, STMicroelectronics, Grenoble INP-UGA

3D CHIP MOUNTING AT CEA-LETI



Connecting layers by sharpening through silicon via HD-TSV are now available for multi-layer 3D integration

The demonstration of wafer level 3-layer integration including Face-To-Back (F2B) configuration received an award at the major ECTC 2024 conference. It combines two fine pitch Cu-Cu hybrid bondings with high-density connections up to an operational 3-layer test vehicle.

3D stacks offer multiple advantages for advanced components such as smart imagers and their assembly in a wafer-to-wafer (W2W) approach opens up access to very fine pitch interconnections. While hybrid bonding is commonly used to connect the layers, high-density (HD) TSV are mandatory for the signals to be transmitted through them.

For several years now, a CEA-Leti team has focused on the key enabling technology of TSV for the 3-Layer CMOS image sensors under development at Nanoelec, and every year it publishes several papers to report on its progress at the international ECTC conference.

At IRT Nanoelec, CEA and ST-Microelectronics demonstrated the feasibility of 3-layer stacking in 2023. This major result of the Smart Imager program was presented in the form of three publications at the major ECTC 2024 conference. One of them received a "best paper award" from the professionals.

"After having successfully demonstrated a 2-layer face-to-back (F2B) test vehicle (TV), we reached the next level of integration by achieving a 3-layer TV with fine-pitch Cu-Cu hybrid bonding (HB) technology and high-density (HD) Through Silicon Via (TSV); After demonstrating 3-layer TV functionality, the next step will be to implement this 3D technology in a functional advanced CMOS image sensor (CIS) in the next few years," says Stephan Nicolas, as a first author of the paper receiving the award.

"The 3-layer demonstrator is one of Nanoelec's major technological achievements," underlines Alexis Farcy, R&D Process Development Engineer - 3D Integration at STMicroelectronics. *"The three-layer structure will enable the image sensor to be equipped with an artificial intelligence function, which necessarily requires a lot of computing power and memory. Hybrid bonding has already been well developed as part of Nanoelec's programs since 2012. It is now industrial. And from there, the new building blocks of the Smart Imager begin. For us, these morphological and electrical results validate these building blocks, which are really the key elements that will now enable us to move on to the physical relationship of a much more ambitious functional demonstrator."*

FIB-SEM 3D CROSS-SECTION OF THE 3-LAYER TEST VEHICLE - PITCH IS 6 µm FOR THE BONDING PADS - HD TSV DIMENSIONS ARE 1X10µm.

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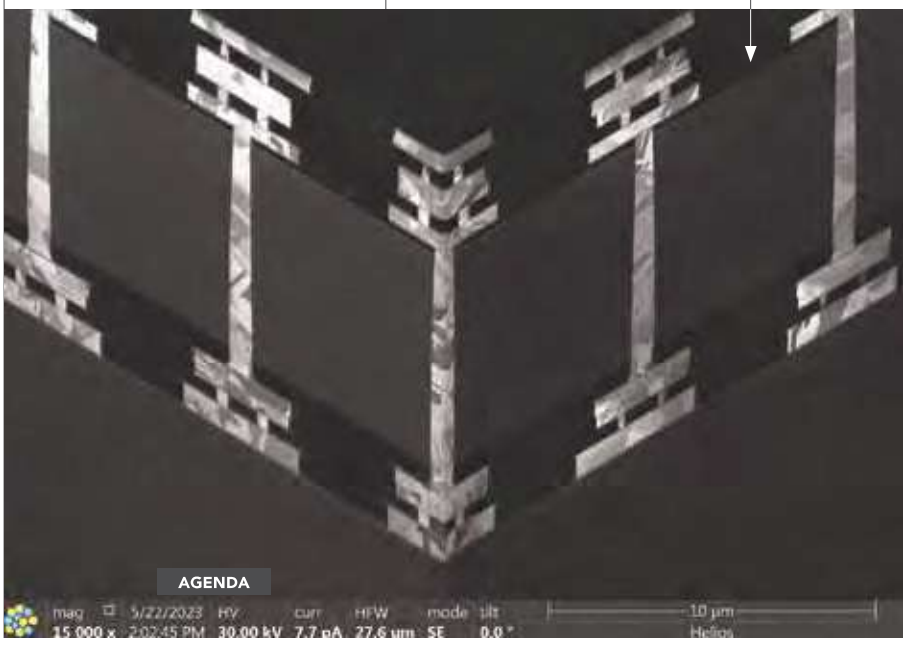
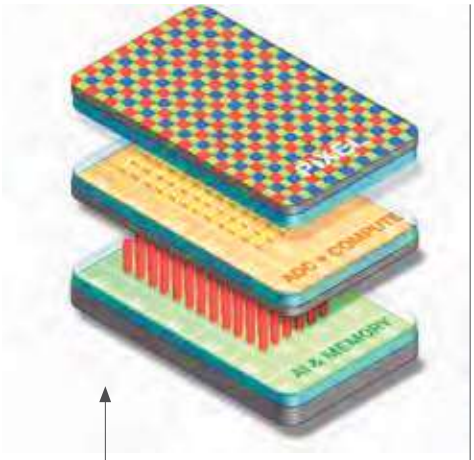


> ***"For several years now, a CEA-Leti team has focused on the key enabling technology of TSV for the 3-Layer CMOS image sensors under development at Nanoelec..."***

In-sensor computing for event-based imaging

On the occasion of the Nanoelec 2024 General Meeting, Pascal Vivet, CEA-Leti, reviewed the development of event-based imagers equipped with artificial intelligence.



SCHEMATIC OF A 3-LAYER SMART IMAGE SENSOR, WITH EMBEDDED AI

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Why develop event-based sensors?

P.V. Event-based imagers allow very high-rate acquisition of images, in that only the pixels which record a variation contribute to the data stream. The target applications are augmented reality, typically tracking of the hand, the eyes, gestures, presence tracking or detection.
Sensors incorporating AI functions are already available on the market, but our 3-layer concept offers greater performance and a wider range of applications. We start from an event-based 2-layer imaging architecture available at Prophesee. We propose adding a third electronic layer which will be strongly coupled to the imager. This third layer supports AI functionalities and this is called in-sensor computing.

What are the development constraints for such a very small sensor?

P.V. In Nanoelec/Smart Imager program, we are developing both the hardware part and the AI software highly optimized to reduce energy consumption and computing times. It will be possible to make extremely small objects capable of monitoring our environments at very low cost and running on batteries. Our sensor will measure barely more than one cubic millimeter, and will thus easily be installed in the limited space available inside a smartphone. Its electrical consumption is very low and its processing latency, that is acquisition and processing with embedded AI, will be about one millisecond. This project is the result of active collaboration, in which Prophesee provides the core of the 2-layer imager, CEA proposes and implements the specific AI accelerator in the third layer, Siemens EDA supplies the design tools (behavioral synthesis, DFT, sign-off), and STMicroelectronics participates in logical and physical implementation of the final circuit. The manufacturing of the demonstrator will use both STMicroelectronics and CEA-Leti clean-rooms

How to embed AI directly in the image sensor?

P.V. In an event-based imager, the principle is to generate a pixel event when there is a change in contrast. In this case, standard AI solutions are not easily applicable. The traditional Convolutional Neural Networks (CNN) used in AI mean that the image and the pixels must be integrated in time, which loses information on the precision of the events. SNN (Spiking Neural Network) type networks, based on spikes, even though closer to the nature of the pixel events, are not suitable as a type of coding. A network structure based on GNN (Graph Neural Network) was proposed to encode the sparsity of pixel events, while retaining an efficient computing method. The HUGNet processing architecture, based on GNN, was proposed, as it can be used to process different types of AI algorithms (monitoring, tracking, recognition, classification, etc.), with unparalleled memory and computing performance (> x100) by comparison with the best CNN solutions that could be imagined with an event-based sensor. The algorithm core was developed in 2024, a first high-level architecture model was developed at the end of 2024, and development of the RTL hardware building block is ongoing in 2025, with the circuit being sent for manufacturing at the end of 2025.

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PASCAL VIVET, FORMER SCIENTIFIC DIRECTOR OF THE DIGITAL CIRCUITS AND ARCHITECTURES DEPARTMENT AT CEA-LIST

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SÉBASTIEN THURIES, DEPUTY DIRECTOR OF NANOELEC/SMART IMAGER PROGRAM

Date Conference 2024

In April 2024, at the reference international conference in the field of circuit design, DATE[1], the Nanoelec/Smart Imager program teams took part in organizing a workshop on the challenges of 3D, more particularly in the field of imagers.

Sébastien Thuries, engineer at CEA-List and Deputy Director of the Nanoelec/Smart Imager program, presented the benefits of multi-layer technology for developing an image sensor with a low energy footprint.

"We are progressing in terms of silicon production with respect to integration of a third silicon wafer, thanks to Through Silicon Vias (TSV) at very high density (~1µm on a side)," he explains. *"The circuit design methodologies are also evolving and a suite of tools (design, simulation and verification) benefited from the circuits developed in the program."* Two circuits were presented, one for imaging in the visible spectrum and the other for event-based imagers: J3DAI, a multi-layer circuit with integrated AI accelerator for rapid and efficient processing of the AI algorithm, and HUGNet, also a multi-layer circuit for AI processing dedicated to the event-based imager thanks to the Graph Neural Network (GNN) and offering results several orders of magnitude better than traditional Convolutional Neural Networks (CNNs).

AGENDA

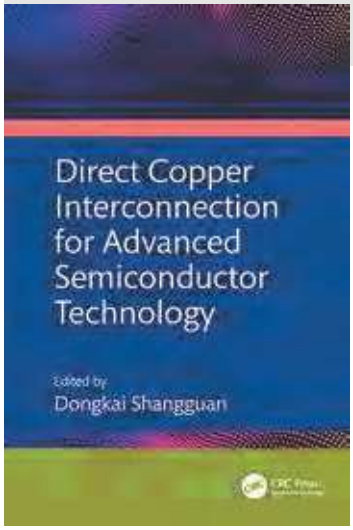
1. Date Conference, March 25 – 27, 2024 I Valencia, Spain

Characterization, Modeling, and Reliability for Direct Copper Interconnection

Hybrid bonding technology.

Stéphane Moreau, a senior expert at CEA-Leti in the field of integrated circuit interconnect reliability, and Dongkai Shangguan, an IEEE Fellow & IMAPS Fellow and President of Thermal Engineering Associates, Inc. and a strategic advisor to innovative companies in the global semiconductor and electronics industry, have written a book chapter addressing the advances and challenges related to "Direct copper interconnections for advanced semiconductor technologies".

They reviewed the most significant qualification and reliability achievements for hybrid bonding-based interconnects over the last ten years by the industry and the scientific community. An overview of 3D interconnects and their evolution, failure mechanisms, and related accelerated tests and associated standards for 3D packaging technology are analyzed. A discussion follows on the qualification and reliability testing results of the hybrid bonding technology by the industry and the scientific community. This book chapter is completed by a review of numerical simulation studies covering bonding physics, electrical and thermal performance and the reliability of hybrid bonding technology.



> ***"An overview of 3D interconnects and their evolution, failure mechanisms, and related accelerated tests and associated standards for 3D packaging technology are analyzed.***

Copper interconnections within cryogenic systems

Assessing robustness and electrical performance of copper HD-TSV at low temperatures.

A study led by CEA-Leti scientists evaluates copper High Density-Through Silicon Vias (HD-TSVs) in cryogenic environments, which are crucial for applications like quantum computing and astrophysics. The use of HD-TSVs notably allows for increased signal density, enabling device scaling. *"1,980 thermal cycles between 344 K and 77 K were conducted to assess the mechanical and electrical robustness of HD-TSVs to cryogenic conditions,"* explains Stéphane Moreau, as first author of the paper published in IEEE Electron Device Letters.

Additionally, one thermal cycle was carried out in a cryostat down to 2 K. In-situ and ex-situ electrical measurements show remarkable stability in the electrical resistances of the tested structures with a variation of less than ±3%, even after 1,980 thermal cycles. *"Our results confirm the robustness and electrical performance of copper HD-TSV at low temperatures, opening up prospects for their integration within cryogenic systems,"* Stéphane Moreau adds.