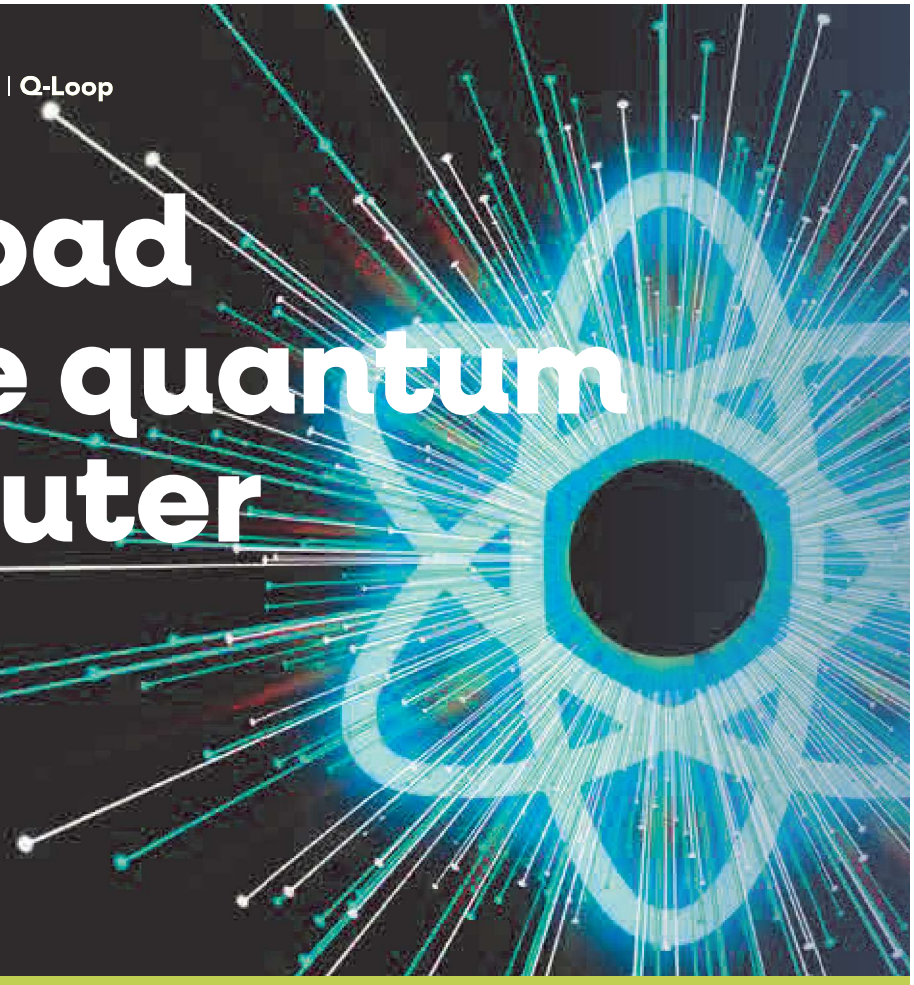
The road to the quantum computer



Providing France with the value chain needed to produce scalable electronics for fault tolerant quantum computer.

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The Q-Loop program brings together a host of academic and industrial partners to speed up the creation of a universal quantum computer. The aim is to tackle the challenge of scaling up solid-state qubit control and readout systems. The program's actors are focusing on developing software and hardware technologies for the qubit control chain, covering both control electronics and real-time quantum error correction.

The Grand Défi LSQ (LSQ great challenge) was launched by the French Government as part of its National Strategy for quantum technologies, and aims to overcome the obstacles scale up the qubit count. Scaling up entails the ability to acquire industrial processes for mass production and control of standardized, reliable quantum computing qubits.
To structure the technological value chain so that the actors needed for these industrial processes can emerge, Nanoelec is starting an unprecedented program dedicated to LSQ and directly connected to the French National Quatum Strategy. The aim is to demonstrate a control and readout chain validating the future capability to control a quantum computer with a large number of qubits.

Nanoelec's Q-Loop program focuses on developing the necessary technologies to enable qubits control and readout at scale. It brings together a wide variety of complementary actors along the value chain needed to produce and eventually maintain quantum computer control and command components. It creates strong collaboration between key industrial players in the semiconductor sector, centers of R&D excellence in quantum electronics and emerging actors in the quantum field.
The program was launched in 2024 and gathers 65 million euros of public and private funding over a six-year period. •

AGENDA

Q-LOOP AT A GLANCE

→ Vision
The advent of Quantum computing is deemed to impact many application domains and especially compute intensive R&D tasks, making it a key technology to master at the French & European level to ensure future digital sovereignty

→ Ambition
Structure the technological value chain of actors necessary for the emergence of scalable technologies and industrial processes needed to produce fault-tolerant quantum computers

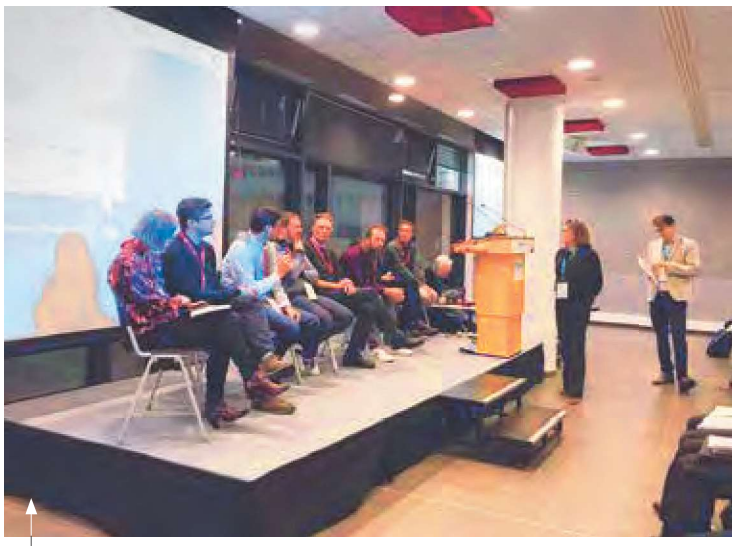
→ Mission
Take up the technological challenges, in particular for innovative solutions in electronics, integrated photonics and 3D stacking and packaging technologies compatible with operation at cryogenic temperatures, along with hardware acceleration for real-time error correction, and coupling them with accelerated capacity for transfer from R&D to industry

→ Partners
The project involves actors along the value chain including the main French research institutions in the domain, a CAD tools vendor, and a CMOS chips manufacturer, together with national startups specialized in solid-state qubits and enabling technologies

Program kick-off

Fruitful interaction

The kick-off meeting was successfully held on November 2024, demonstrating a high level of attendance with about 50 on-site attendees and 30 remote ones.
Technical workshops were organized the same day, dealing with different topics (architecture & system modelling / test needs / cryoelectronics / 3D integration / thermal simulation) and led to fruitful interaction between the attendees from the different entities.



Q-LOOP KICKOFF
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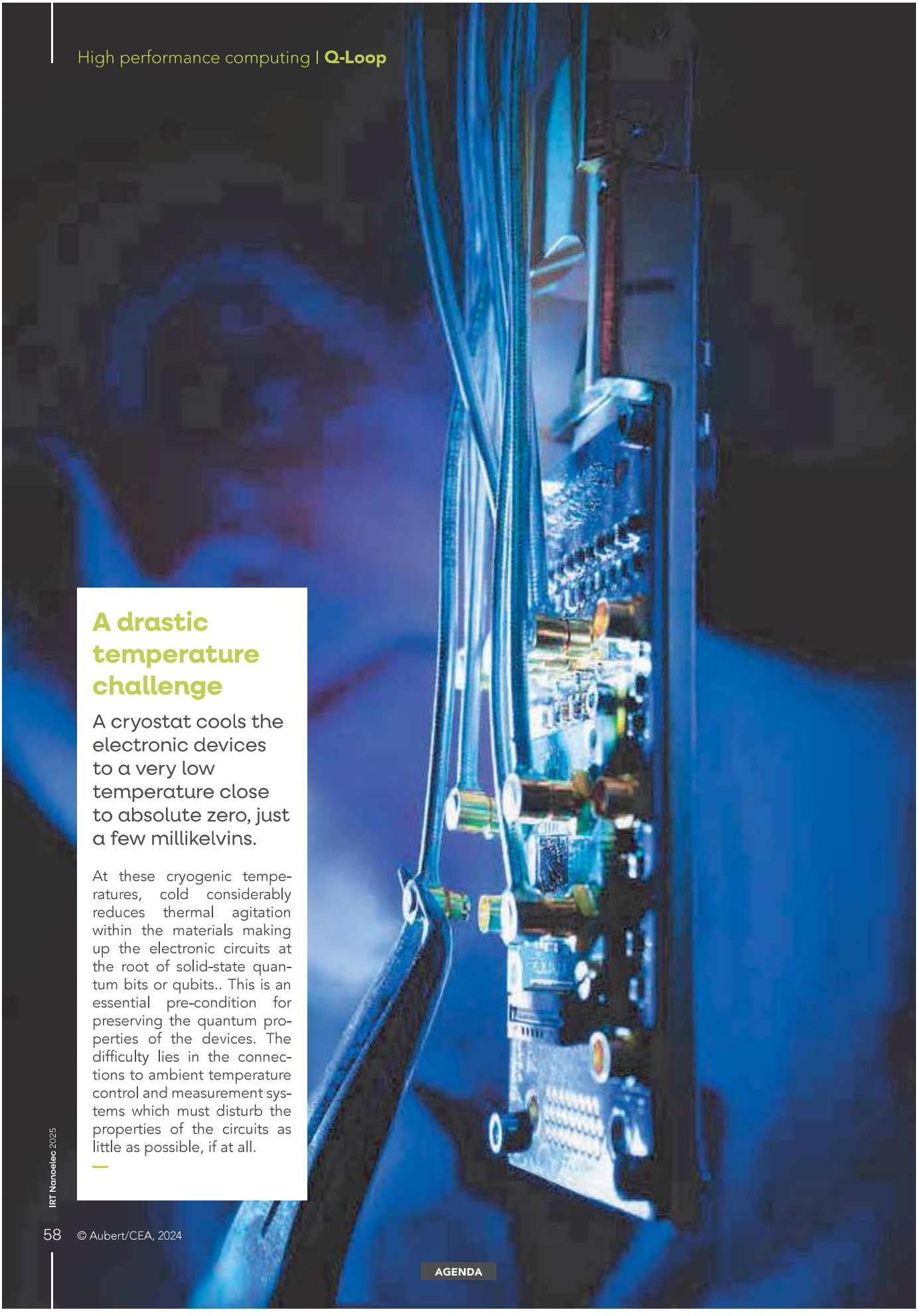
First test vehicles for cryo TSV

24 wafers, with different TSV Aspect Ratios.

Critical to enable greater integration while providing best-in-class signal conservation property, the definition of fabrication process for 2D and 3D interconnections using superconducting materials was addressed early in the project definition.

Following high expectations and expression of needs by startups, the first test vehicles process embedding TSV modules and related daisy chains was launched, in order to address the conformality study of several superconducting metal deposits. The experimental plan involves 24 wafers, with several TSV Aspect Ratios as well as various vacuum deposition techniques and metals.



A drastic temperature challenge

A cryostat cools the electronic devices to a very low temperature close to absolute zero, just a few millikelvins.

At these cryogenic temperatures, cold considerably reduces thermal agitation within the materials making up the electronic circuits at the root of solid-state quantum bits or qubits.. This is an essential pre-condition for preserving the quantum properties of the devices. The difficulty lies in the connections to ambient temperature control and measurement systems which must disturb the properties of the circuits as little as possible, if at all.

From qubit to supercomputing

A large number of entangled qubits.

By performing operations on qubits whose two quantum states are superposed and entangled with one another, the quantum computer should be able to represent a large number of possible states with a small number of qubits. A system such as this will be able to process several values simultaneously and thus significantly speed up certain processing operations by comparison with a conventional computer.
It could thus be used to solve complex problems which are hard or even impossible to solve with conventional computers, in a large number of application fields, notably solving combinatory optimization problems and/or those which require immense computing capacity: for example, in the fields of logistics or finance, to develop weather forecasting models and climatic services, AI applications, design new materials, or model chemical reactions at the molecular level to develop new medicines.

To achieve computing capacity such as this, we would need quantum computers with a large number of entangled qubits, with a low level of computing error in each basic operation.

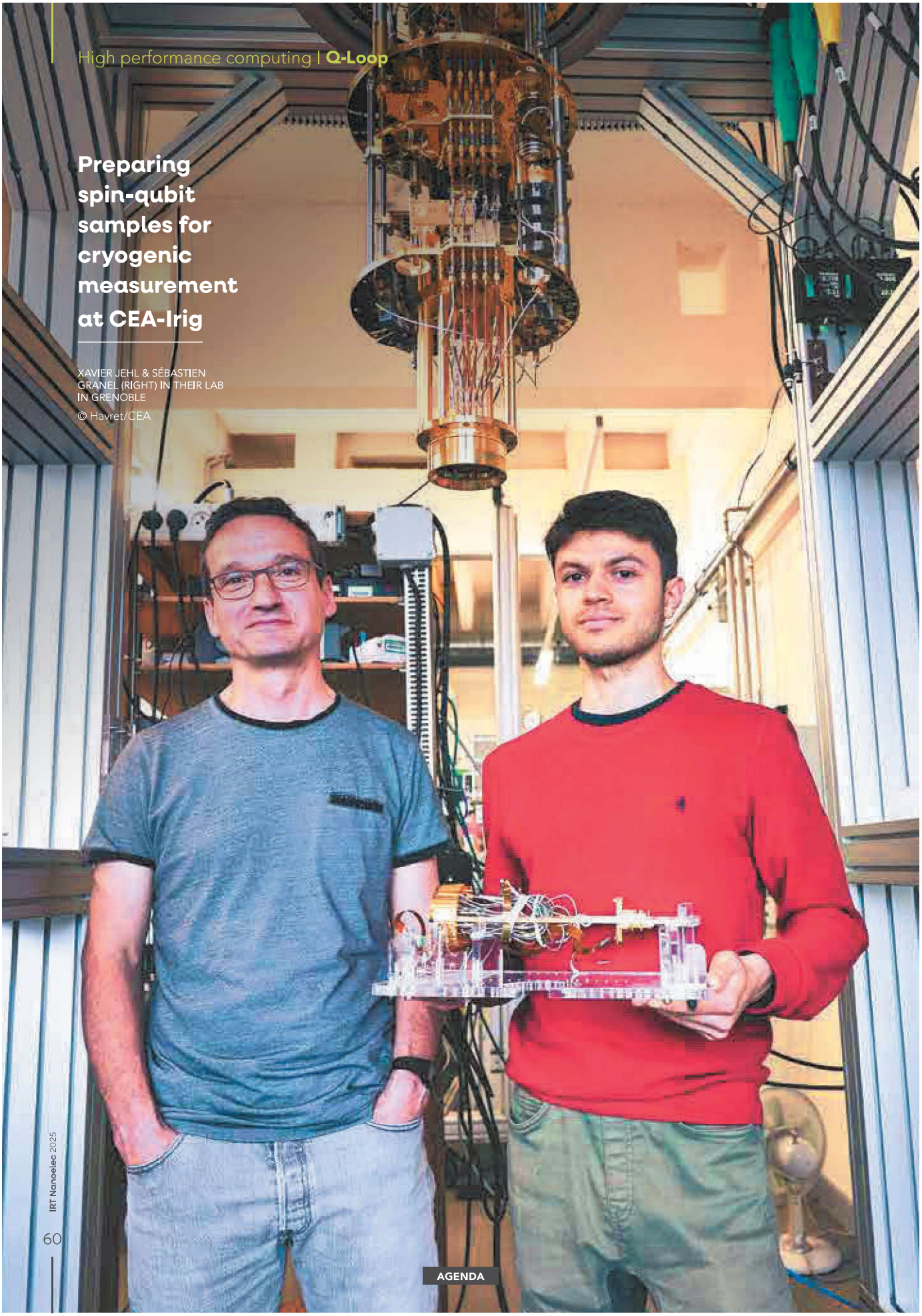
CRYOGENIC TEMPERATURE TEST BENCH FOR 300 MM INDUSTRIAL STANDARD WAFERS CARRYING CMOS TECHNOLOGY QUBITS, AT CEA-LETI
© Aubert/CEA

Cryo-CMOS

STMicroelectronics, Siemens EDA, CEA, Grenoble INP-UGA and CNRS joined forces.

STMicroelectronics, CEA, Grenoble INP-UGA and CNRS joined forces to thoroughly fine-tune the definition of the characterization and modelling plan necessary to reach a well-qualified Cryo-PDK within the first three years of the program. A BEOL (back-end-of-line) measurements plan was defined between partners for the development of interconnects. In addition, a preliminary FEOL (front-end-of-line) measurement plan (at room and cryo temperatures) was consolidated.

Preparing spin-qubit samples for cryogenic measurement at CEA-Irig



XAVIER JEHL & SÉBASTIEN GRANEL (RIGHT) IN THEIR LAB IN GRENOBLE

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Sound strategy to handle cryogenic thermal simulation

On EDA tools for quantum systems.

The gap analysis on existing EDA tools for quantum systems design started with a first identified aspect regarding thermal simulation in cryogenic conditions. Successive workshops between thermal simulation experts on the thermal range of standard electronic devices (Siemens), thermal simulation experts on cryogenic conditions (CEA), and physics experts on thermal phenomenon experiments at these temperatures (CNRS) have reached a strategy to support the thermal simulation of complex IC in these regimes where heat transfer depends on the wave behaviour of phonons and in particular to their bounces at material interface depending on their scale.

The feasibility of leveraging Non-equilibrium Green's function models (slow but more accurate) qualified by experiments, to tune existing EDA tools (fast but inaccurate in these regimes) was assessed. Future works will require significant efforts relying on experimental teams, low-level simulation for small systems and intermediate validation and EDA tools for the thermal evaluation of larger scale systems.

QEC code

Hardware acceleration using FPGAs.

Qubits, whatever their modality, are highly sensitive to noise and environmental disturbances that can alter their state. Given that QEC is an essential element in the construction of practical and reliable quantum computers, CEA & Inria experts carried out a very first review of the state of the art in quantum error correction (QEC) codes and associated decoders, underlining the specificities of four classes of decoding approaches for the well-studied surface codes. Future works will target hardware acceleration using FPGAs of most promising approach to scaling.

NANOELEC.

Q-Loop

Visibility of the program

A communication kit was produced, including a .pptx presentation template adapted from Nanoelec's theme; a logo for the program, consistent with the Nanoelec typography was defined, as well as web pages for the Nanoelec website in both French and English. It should be noted that during the summer of 2024, prior to the official launch, a communication kit for the official national strategy website was also produced.