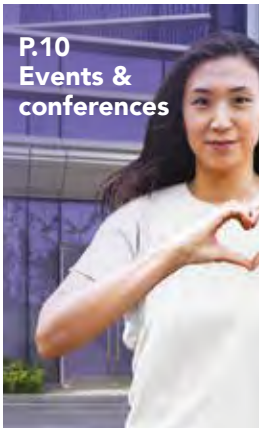
NANOELEC.

Scientific & technical highlights

2025 EDITION

AGENDA

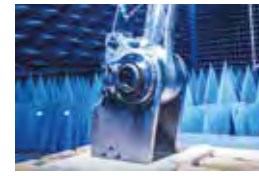


Images & Photons

High performance computing

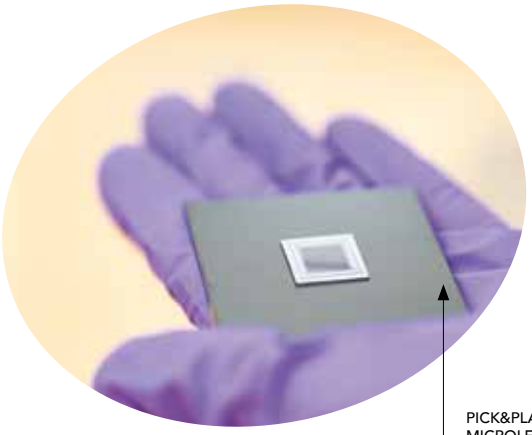
Digital trust

Dissemination



Exploring the future of electronics

IRT Nanoelec runs multi-partner programs to make the electronics industry more competitive and greener, and thus contribute to the sustainable development of society.



PICK&PLACE TOOL FOR MICROLED MASS TRANSFER

The Nanoelec technological research institute (IRT) is a consortium of private and public sector players, backed by CEA. Our mission is to help companies create value and enable their products to stand out on the digital transition stage.

Nanoelec contributes to the competitiveness of the electronics industry, in France and in Europe. Based in Grenoble, a world-class hub for research, innovation and production in its field, the Institute runs R&D programs built jointly by representatives from the academic and industrial worlds. These programs deal with the design and development of new processes, systems and components in the following fields:

- Images: new-generation of displays and imagers,
- Digital trust and frugality on connected objects and embedded AI
- High Performance Computing (via photonics and quantum computing)
- Characterization and resistance to radiation of components and systems by means of large instruments.

"A circle of trust to carry out responsible research and development programs to help businesses create value."

Nanoelec also designs training courses for emerging technologies and markets as well as technology dissemination programs for SMEs. We implement open innovation techniques as well as more conventional technological development methods.

Given the pervasive nature of digital technologies, Nanoelec is in contact with actors from all sectors ranging from goods to services, industry, infrastructures, and consumer products, as well as transportation, the environment and health.

Nanoelec is a member of FIT, a hub of technological research institutes (IRTs) and energy transition institutes (ITEs) set up by the French Government and financed by the France 2030 program (National Initiative for Investments for the Future). The network of institutes was created to pool academic and industrial players who could run collaborative R&D and innovation projects aimed at boosting the competitiveness of the French economy. •

OPTIONS FOR A NEW ARCHITECTURE TO SUPPORT AI AT THE EDGE IN A DISRUPTIVE SMART IMAGER

"Anticipating future human and technological needs in electronics."

Innovation in microelectronics

- Carry out world-class collaborative R&D in selected areas to produce innovative components and embedded systems: imagers, displays, photonics on Si design & devices for quantum computing and digital trust & security
- Develop and transfer these technologies to create the electronic circuits and components of the future
- Give industry players access to development, prototyping and advanced characterization resources, including large EU instruments for research

Technology dissemination

- Help businesses in the field of information and communication technologies meet the challenges of IoT through digital trust and security
- Provide expertise to help SMEs from various industrial sectors build new products and services with innovative components and embedded software
- Promote cooperation between SMEs, mid-caps and large companies
- Unveil new applications comprising environmental and social impact assessments through collaborative innovation

Development of human capital

- Attract young people to jobs in electronics that contribute to sustainable development
- Work with partners on parity and workplace equality
- Design training courses to meet the current needs of the electronics business
- Anticipate future skills requirements in the sector: sustainability, cross-skills, social and professional communities for innovation

NANOELEC AT A GLANCE

A consortium of **21** public & private members
as of December 2024

352 associated partners including **267** SMEs
since 2012

€48M average annual budget
(2020-2024)

784 scientific or technical publications & communications
since 2015

258 patents and **58** software filed
since 2012

200 full-time jobs
Yearly average 2020-2024

Trends notes: sovereignty & sustainability

IN 2024, NANOELEC LAUNCHED THE Q-LOOP PROGRAM DEDICATE TO THE DESIGN OF QUANTUM COMPUTER

© A. Havret/CEA

SÉBASTIEN DAUVÉ, DIRECTOR OF CEA-LETI AND PRESIDENT OF NANOELEC STEERING COMMITTEE

© C. Tresca/CEA

“The Grenoble ecosystem is ready to take up the major challenges of the microelectronics transformation, with regard both to sovereignty and the ecological transition.

Bringing together all the sector’s innovation actors

by Sébastien Dauvé

In a geopolitical context that we all know to be tense and uncertain, the semiconductor sector is faced with significant challenges, in terms of both sovereignty and the ecological transition. With the Chips Act, Europe holds a strong hand in its dealings with the two main leaders in this field, Asia and the United States: the Chips Joint Undertaking (Chips JU) brings together the main European microelectronics innovation ecosystems. On the Fames pilot line run by CEA-Leti, we will be able to advance the various key technologies in our ecosystem, notably FD-SOI, to bring down the energy consumption of embedded components, but also heterogeneous integration, which is vital to obtaining smarter and more frugal components.

In the French ecosystem, Nanoelec plays a crucial role in stimulating collaboration between the leading actors who are ready to take up the major challenges of the microelectronics transformation. In line with the slogan “Think global, act local,” the Institute brings together the sector’s innovation actors present in the Alpine region, along with everything they can bring to the table: a circle of trust enabling a wide variety of actors to share common goals, world-class technology platforms and unparalleled training resources to guarantee highly competitive human capital in the coming years. •

HUGUES METRAS,
DIRECTOR OF NANOELEC
© P. Jayet/CEA

Paving the way for sovereign and sustainable electronics

by Hugues Metras

In 2024, we launched our Q-Loop quantum computer program, which is mobilizing 65 million euros over six years, to enable France to pave the way for qubit control systems and develop the technologies needed for quantum computer control and command.
Ahead of the next financing tranche of the IRT Nanoelec (2026-2030), our Institute is already making profound changes to its activities: sovereignty and sustainable development will be the main pillars of our future programs, in which we will promote heterogeneous integration for imaging, photonics and computing.

The advent of more sustainable and more responsible electronic and digital systems is also an increasingly significant aspect of our activity:
➔ the very first national symposium on the subject[1], in December 2024 in Grenoble, attracted more than 40 original contributions and 200 French-speaking participants, making Grenoble the barycenter of eco-design and eco-innovation in our sector;
➔ to prepare for our 2026-2030 programs, we also spent twelve months playing a full role in the cycle of the *Convention des entreprises pour le climat* (corporate climate convention), the aim of which is to organize awareness-raising and transformation programs for economic decision-makers.

We will be continuing to explore relations between our subsidiary and society: Nanoelec has organized the second edition of the microelectronics poster competition[2] and promoted the creation of the "Women in tech in Isère" collective. •

"We will be promoting heterogeneous integration for imaging, photonics and computing.

IN 2024 & 2025, NANOELEC SUPPORTED THE CREATION OF THE "WOMEN IN TECH IN ISÈRE" COLLECTIVE
© CEA

IRT Nanoelec 2025

1. Organized by Nanoelec with PEPR Electronique, the Microélectronique-UGA labex and the *Pôle universitaire d'innovation* (PUI) Grenoble-Alpes.

2. Creations by the students of the Brassart school with Teledyne E2V, and the *Dauphiné libéré* newspaper for the Tech&Fest 2025 festival

SANDRINE MAUBERT, DEPUTY DIRECTOR OF NANOELEC

© P. Jayet/CEA

Giving meaning to our sector

by Sandrine Maubert

Pilot projects for eco-innovation are now under way in all the Nanoelec programs, notably lifecycle analysis and processes. The issues of systems and infrastructure frugality are also addressed and we are gradually taking on board the development of the digital models needed to design circuits, in order to integrate social and environmental responsibility parameters into the traditional figures of merit used in design in the electronics field[3].

By supporting the CEA teams participating in the EECONE (European ECOsystem for greeN Electronics) project, Nanoelec is looking at a new subject of interest concerning the fate of components once they have been used.

•••

3. The most common figure of merit takes account of computing power vs. energy consumption, surface area vs. the cost of the component (PPAC).

Finally, even if Europe acquires high-performance technical platforms, we will also need competent and motivated human resources to run our plants. At Nanoelec, we are therefore committed to training and awareness-raising in order to motivate the students, but also to get them thinking, because they will be the future guarantors of our sovereignty, competitivity, economic performance and respect for the planet's limits. •

> ***"Mobilizing future talents for sovereignty and sustainable electronics.***

IN 2024, NANOELEC INITIATED THE VERY FIRST SYMPOSIUM FOR SUSTAINABLE ELECTRONICS AND DIGITAL, WITH PUI GRENOBLE-ALPES, LABEX MICROELECTRONIQUE GRENOBLE-ALPES, PEPR ELECTRONIQUE, IN COLLABORATION WITH MINALOGIC AND IN PARTNERSHIP WITH TECH&FEST FESTIVAL.

© P. Jayet/CEA

EVENTS & CONFERENCES

January 2024

January 9

DIGITAL PASSPORT FOR PRODUCTS

Nanoelec/Human Capital Training Engineering program conducted an interactive masterclass on the emergence of the EU Digital Passport for products.

January 18

SOI 3D PHYSICAL DEMONSTRATOR

Webinar live form CEA-Leti Cleanrooms, on a 3D physical demonstrator to allow experts to easily explain the sequence of steps in the manufacturing of a transistor in a cleanroom.

January 19

WOMEN IN TECHNO-LOGICAL RESEARCH

Exhibition "Portraits of Women in Technological Research" at Grenoble Tourist Center.

© CEA/Legrand

January 22

AMBASSADORS WITH FAME UGA

Training for professionals to go in schools and colleges to present their jobs.

February 2024

February 1

INDUSTRY ATTRACTIVENESS AT TECH&FEST

45 graphic design students from the Brassart school to design a poster on the theme: "Microelectronics for a Better World" with Aniah, Schneider Electric, Teledyne E2V and Ebra/Le Dauphiné libéré.

February 6

INTERACTIVE SCREENS

Workshop for experts and students in electronics and management to consider the rebound effect in interactive screens.

© Grenoble INP-UGA

© Agence Grenoble-Alpes

March 2024

March 5

ELECTRONIC BUSINESS AMBASSADORS

IRT Nanoelec, the Agence Grenoble Alpes, and the Association Grenoble Alpes organized a networking event, and meetings with ambassadors of the region and the electronics sector.

March 6

FRUGALITY OF IOT

Webinar: an evaluation methodology for the frugality of connected devices such as IoT, using the specific case study of a sensor designed to control water consumption in domestic environments.

March 8

INTERNATIONAL WOMEN'S RIGHTS

Round-table: feminization of the workforce in the electronics sector, with STMicroelectronics, Limatech, CEA.

March 26

HETEROGENEOUS 3D

Workshop: "Heterogeneous 3D Architectures and Sensors" at DATE, The European Event for Electronic System Design & Test.

April 2024

April 2

WOMEN IN ENGINEERING

Nanoelec exhibition Women in Technological Research presented at STMicroelectronics Crolles and STMicroelectronics Grenoble.

May 2024

May 15

SOVEREIGNTY IN FRANCE

Naneolec supports the 2024 Geopolitics Conference a Grenoble Ecole de Management (GEM dedicated to the technological sovereignty of France.

May 28

AI-EMBEDDED CMOS IMAGE SENSORS

Three-Layer Integration Breakthrough for AI-Embedded CMOS Image Sensors : three papers presented at ECTC international conference.

June 2024

June 17

EXHIBITION AT TELEDYNE

Employee day dedicated to para-sports at Teledyne E2V included the exhibition "Microelectronics for a Better World," created for Tech&Fest 2024.

June 28

INTERNATIONAL WOMEN IN ENGINEERING DAY

Webinar: women's networks in large companies, in collaboration with the Women Engineers.

August 2024

August 18

3D PACKAGING

Achieving 3-layer stacking integration for future smart imagers, published in Chip Scale Review.

September 2024

September 3

ATTRACTING YOUNG PEOPLE IN SCIENCE AND MICRO-ELECTRONICS

Webinar: the opportunities for industries to take part in the Night of Orientation.

September 18

DIGITAL WORLD AND SMES

Boot and networking event with Minalogic and Captronic at Sido/Lyon. Seminar on AI & technology research for businesses by 7 FIT institutes: Nanoelec, B Com, System X, Bioaster, IPVF, Railenium & St Exupery.

October 2024

October 3

CONTROL SYSTEMS OF QUANTUM COMPUTERS

Nanoelec participated in the thematic day on quantum technologies organized by Minalogic.

October 16-17

CAREERS FORUM

Nanoelec supported the creation of a microelectronics Village at the Grenoble Careers Forum, organized by the local authority, with Lynred, Soitec, ST, CEA, and the Ministry of Education.

November 2024

November 8

CAREERS IN CYBERSECURITY

Serious games and frugal technology sensibilisation at CSAW, the world challenge for pupils and students in cybersecurity, EU node beeing yearly organized by Grenoble INP-UGA/Esisar.


© Grenoble INP-UGA

November 12

SCALING OF QUBIT CONTROL AND READOUT SYSTEMS

Kickoff ot the new Nanoelec/ Q-Loop program to accelerate the development of fault-tolerant quantum computers, by exploring novel control-command architectures and technologies.

November 14

NANOELEC GENERAL ASSEMBLY

Keynotes on AI form Christophe Cerin (Inria) and Lionel Cordesses (IRT Saint-Exupery).

November 22

GRENOBLE ORIENTATION NIGHT

A round table powered by Nanoelec, with UGA, Limatech, ST, Aniah, CEA, Grenoble INP-UGA, Siemens EDA.

December 2024

December 10

SUSTAINABLE INNOVATION

In the frame of the Pole Universitaire d'innovation Grenoble-Alpes, Nanoelec participated in a roundtable discussion on the expectations and initiatives for sustainable innovation in public research.

December 12

SUSTAINABLE ELECTRONICS & DIGITAL TECHNOLOGIES

Very first national symposium on Sustainable Electronics & Digital Technologies. With the Grenoble Alpes University Innovation Hub (PUI), the PEPR Electronics, and the Labex UGA Microelectronics.

December 17

HIGH-DENSITY THROUGH-SILICON VIAS (TSV)

Webinar: three years of results on combination of Hybrid Bonding technologies and High-Density Through-Silicon Vias (TSV).

© Jayet/Ebra

February 2025

Feb 5-6

TECH&FEST

Poster competition "A Wolrd of microelectronics" with Diseingers students of Ecoel bras art, Ebra/le Dauphiné libéré and Teledyne E2V. Demonstrator Gesturma, as a gamification of Nanoelec/ Addvisia platefom.

March 2025

March, 12

WOMEN RIGHT INTERNATIONAL DAY

Nanoelec supported the creation of a networking collective "Women in tech in Isère".

March 31-April2

DESIGN, AUTOMATION AND TEST

Nanoelec supported 2025 DATE, the European Event for Electronic System Design & Test.

April 2025

EASYTECH AT A GLANCE

Nanoelec and Minalogic powered a series of webinars on Easytech projects.

May 2025

May, 14 & 15

IRRADIATION HARDNESS

Nanoelec supported the annual workshop for industry on radiation hardness testing of semicondcutor devices and systems G-Radnext, at Ganil (France).

June 2025

June, 23

INWED'25

Annual international women in engineering day: Nanoelec supported a special event at CEA/Y. Spot with the networking collective "Women in tech in Isère".

July 2025

July 1st

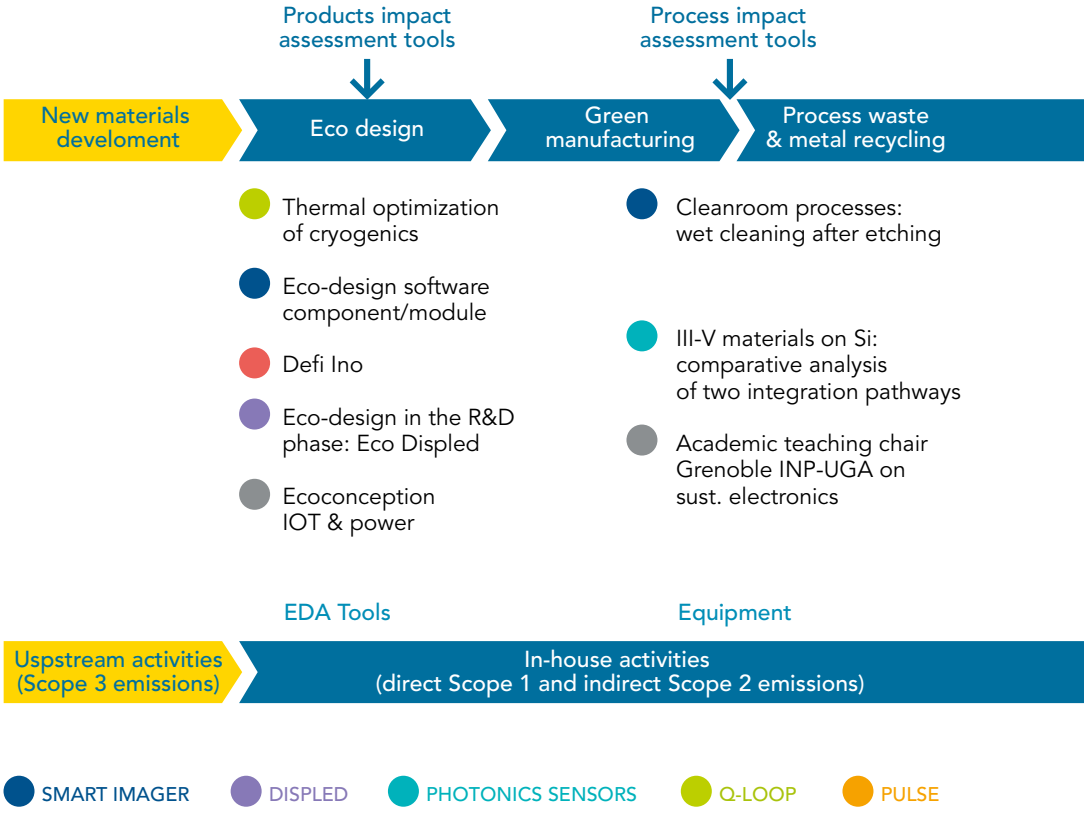
BIODIVERITY VS BUSINESS

As an output of the CEC cycle, Nanoelec and Decathlon Outdoor cooperated to organise a discovering walk of biodiversity in the contexte of the urban scientific polygon of Grenoble, with a visit of Schneider Electric Intencity sustainable building.

Sustainable development

The sustainable development actions initiated and carried out by the academic and industrial players in the electronics sector as part of Nanoelec meet at least 10 of the UN's objectives. They contribute to meeting today's national and European competitiveness challenges, and to making the sector even more relevant to tomorrow's world.

Since 2024, Nanoelec's roadmaps have included addressing challenges at the crossroads of sustainable development and sovereignty. There is no doubt that these challenges will be at the heart of Nanoelec's programs in the coming years. The Institute has already initiated a large number of pilot actions, represented below.



Products impact assessment tools

Use	2nd life	E-waste recycling
Sensor for smart buildings & energy saving		REPEX : components reuse
Frugal blockchain		EECONE : Electronic & electrical waste reduction
Frugal electronics		
Frugal AI		Digital Product Passport
Transformational issues of organizations & businesses		

Academic research chair UGA-CEA : sustainability, reliability and circularity of electronic technologies

Sold products use emissions reduction

Downstream activities (Scope 3 emissions)

CHARACTERISATION TECHNOLOGY HUMAN CAPITAL & TRAINING DESIGN

Between 2021 and 2024, IRT Nanoelec launched three cross-cutting initiatives to inform strategy and prepare for the development of future programs for 2026-30, and several pilot operational initiatives in all of its current programs. Here is an overview of the pilot initiatives.

SMART IMAGER

First lifecycle analyses for the smart imager design

As of the design phase

With a view to designing a smart imager, the first environmental impact assessment results were obtained in 2024. By halving the number of frames to be processed in the imager, we achieve a 31% gain in the climate change criterion, 29% water savings and 49% savings in critical resources.

In 2024, the teams at Nanoelec explored the methodological possibilities for including the estimation of the environmental impacts of a 3D circuit as of the design phase.

A multi-criterion environmental model was developed using the Appa LCA software developed at CEA-List, more specifically thanks to the environmental data obtained from CEA-Leti's cleanrooms. This environmental model was configured to compare the environmental impacts of different multi-layer imager architectures.

DISPLED

Smart Pixel

Water consumption by Chemical Mechanical Polishing

A Life Cycle Assessment of the Smart Pixel flow under development as part of the Nanoelec/Displed program was presented at Display Week 2023[1]. Since there are no component scale databases for microelectronics, or the literature is outdated and does not reflect current trends, this life cycle assessment (LCA) will provide new and previously unseen results. Data were included in the very first demonstration of a calculation tool dedicated to optimizing the key parameters of the environmental footprint of the associated process flow.

The 2024 teams involved in the Displed program focused on a study of water consumption by Chemical Mechanical Polishing (CMP) in hybrid bonding. The consumption of softened water in gas abatement of PECVD in the complete process flow drives the "water use" impact category.

PULSE

Towards a frugal blockchain

Building an alternative to energy-intensive proof of work (PoW)

Consensus protocols and peer-provided proofs are used to establish trust in blockchain systems. Verifiable proofs that guarantee an elapsed time based on security components have emerged as an alternative to the energy-intensive Proof of Work (PoW). *"In pursuit of developing a lightweight blockchain suitable for embedded systems, we studied the feasibility of constructing a proof mechanism attesting an elapsed time for use in a consensus protocol that is suitable for embedded systems, with low-power and that provides a security level at least equivalent to PoW,"* explains Quentin Jayet (CEA-Leti) at the IEEE International Conference on Blockchain[2]. The platform comprises System on Modules that feature an ARM Cortex-A7 processor with a Trusted Execution Environment (TEE) and a Trusted Platform Module (TPM).

1. Holo, Antonin, Dubarry, C., Lopes, J.-C., Dupont, M., Chabaud, S., & Templier, F. (May 12-17, 2023). MicroLED Display Life Cycle Assessment. Display Week, San Jose, USA. https://www.displayweek.org/2023/Program/Symposium

2. Jayet, Q., Hennebert, C., Kieffer, Y., & Beroulle, V. (2024). Embedded Elapsed Time Techniques in Trusted Execution Environment for Lightweight Blockchain. 2024 IEEE International Conference on Blockchain (Blockchain), 81-88. https://doi.org/10.1109/Blockchain62396.2024.00020

PULSE

Life cycle assessment of a building

Digital solutions for sobriety

Located on the Scientific Peninsula in Grenoble, Schneider Electric's IntenCity building[3] offers an ideal case study for assessing the pertinence of digital solutions from the viewpoint of the carbon and more generally the environmental footprint. IntenCity incorporates Schneider Electric digital solutions to optimize both occupant comfort and energy efficiency.

The teams from CEA, the UGA, STMicroelectronics and Schneider Electric collaborated in producing the first life cycle assessment (LCA) of a building zone: calculation of the carbon footprint (for the construction and use of the building), and dynamic thermal simulation (for operation).

More specifically, the study consisted in characterizing the influence of the digital systems on the building's carbon footprint, notably in the utilization phase. While digital equipment represents more than 40% of the footprint for the building construction phase, the Building Management System (BMS) only represents 5% of this annual consumption.

Reducing the greenhouse gas emissions from the production part is a key issue in the overall decarbonization of the BMS. It will thus be crucial in the rest of the program to study the optimization of the number of equipment items necessary for an efficient BMS, while reducing the impact of the production phase of this equipment.

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3. A 26,000 m2 office building in Grenoble, France, equipped with 990MWh photovoltaic capacity, 100kW battery storage capacity (Net-Zero in operations & 41kWh per m2/yr) SymposiumBlockchain62396.2024.00020

EASYTECH

Responsible Technology Dissemination

To commit companies

In 2024, the first flash diagnostics were implemented in some Easytech projects to help companies and their projects move towards an eco-design approach. With the Defi-Ino process, we are looking to develop an environmental diagnostic offering for SMEs, midcaps and start-ups wishing to work with us. Our priority is to help companies cope with the environmental issues of public innovation policies and to provide them with competitive advantages. The proposed diagnostic is quick and inexpensive. It does not replace an actual environmental assessment, nor a life cycle assessment (LCA). It aims to be a simple evaluation, which could encourage companies to commit to a more detailed study and change their environmental responsibility culture.

TECHNOLOGY

Eco-innovation for technological development

Technology assessment

An article in the Sustainability review published by a team from CEA and Grenoble INP-UGA collaborating within the Easytech initiative of the Nanoelec/technology dissemination program, examines the essential aspects of eco-design to be assessed in the initial phases of innovation and explores the involvement of decision-makers and entrepreneurs in the sustainability assessment process[4].

HUMAN CAPITAL & TRAINING DESIGN

Training Design for Green Electronics

Students pursuing electronics

The Nanoelec/Chif program is committed to transforming teaching methodologies by introducing more dynamic content, particularly with a focus on sustainable development. It emphasizes experiential learning and broad access to resources, providing a common platform for a diverse range of learners. Additionally, the Chif program is closely linked to the EU GreenChips-EDU project through Grenoble INP-UGA. The goal is to increase the number of students pursuing electronics and to enhance the professional development of industry workers, with a specific focus on the design and production of sustainable, energy-efficient microchips.

Q-LOOP

Performance and energy efficiency

Quantum Energy Footprint

Quantum technologies have the potential to shape safer and faster ways to extract, exchange, and process information. However, the question of their energy footprint has been a blind spot in current deployment strategies. By associating researchers who contribute to the Quantum Energy Initiative with its Q-Loop program, Nanoelec will integrate energy footprint evaluation into the design of its hardware and software demonstrators for a quantum computer. *"The path towards sustainable and energy-efficient quantum technologies requires in-depth fundamental and applied research on all energetic aspects of these technologies, but with luck this could evenutally bring out an energetic quantum advantage,"* stated Robert Whitney, CNRS Researcher *(Laboratoire de physique et modélisation des milieux condensés (UGA-CNRS Grenoble)* associated to Nanoelec/Q-Loop and cofounder of the Quantum Energy Initiative). The Quantum Energy Initiative (QEI) community gathers experts from various origins, from fundamental quantum physics to technology, from hardware to software, from research to industry, caring for the physical resource cost of emerging quantum technologies and willing to address the question in a scientific way. This requires to build new methodologies, language, and roadmaps.

4. Peigné, S., Ben Rejeb, H., Monnier, E., & Zwolinski, P. (2024). Navigating the Eco-Design Paradox : Criteria and Methods for Sustainable Eco-Innovation Assessment in Early Development Stages. Sustainability, 16(5), Article 5. https://doi.org/10.3390/su16052071

5. PRX Quantum 3, 020101 – Published 1 June, 2022, DOI: https://doi.org/10.1103/PRXQuantum.3.020101)

As far as qubit work at cryogenic temperatures is concerned, the question of the energy footprint of a quantum computer is included in current deployment strategies for quantum HPC. On this photo taken at CEA-Irig, a cryostat cools the electronic devices to temperatures close to absolute zero, just a few miliKelvins. At these cryogenic temperatures, cold considerably reduces the thermal agitation within the materials making up the circuits being studied (for example, an electronic component, or a quantum qubit). This is a necessary pre-condition for preserving the quantum properties of these devices.

CROSS-CUTTING INITIATIVES FOR SUSTAINABLE ELECTRONICS

Symposium for sustainable electronics and digital systems

To support its strategic and programming thinking in favor of developing sustainable electronics – with the help of three other actors in its ecosystem (the PUI Grenoble Alpes, PEPR Electronique and Labex UGA Microélectronique) – Nanoelec took charge of organizing the very first national symposium on sustainable electronics and digital systems. Researchers from all fields were invited to propose scientific contributions promoting their most recent advances regarding tools, methodology and demonstrators on this topic. The symposium was held in Grenoble on December 12, 2024: 42 spoken presentations & posters were given, and more than 200 professionals attended. The experience will be repeated by the end of 2025.

IRT Nanoelec 2025

AT THE VERY FIRST SYMPOSIUM FOR SUSTAINABLE ELECTRONICS AND DIGITAL SYSTEMS

© P.Jayet/CEA, 2024

360° vision

At the end of 2024, Nanoelec asked CEA's Bibliography and Marketing Studies Department to produce a study of the state of the art with a view to creating an overview of sustainable electronics, focused on the priorities established for Nanoelec's 2025-2030 vision. The aim is to highlight concepts and areas of research in order to evaluate subjects requiring development and greater maturity through collaborative research (academic, industrial) in priority fields: equipment/processes, design and tools, architecture (eco-design), management/optimization of the impact of data (storage and traffic), in addition to what each actor has already done at its own initiative.

Convention des entreprises pour le climat

(corporate climate convention)

From April 2024 to February 2025, two members of Nanoelec's management followed the complete cycle of the Convention des entreprises pour le climat (corporate climate convention), involving six two-day seminars distributed over the period. This included 45 companies and organizations with a wide variety of profiles, working together in a spirit of openness and breaking down the barriers between professional sectors, with exchanges of good practices and inspiring ideas, and working as an ecosystem. Training of this type makes it possible to take on board the main arguments underlying the need to take a fresh look at development models in the light of sustainable development, climate change, the planet's limits and the necessary social foundation; to link these highly macroscopic considerations to the contingencies specific to our sector; and to prepare proposals for a long-term roadmap incorporating sovereignty and sustainable development.

PARITY AND ATTRACTIVENESS OF THE MICROELECTRONICS INDUSTRY

For several years now, March 8 and June 23 have been dates on which Nanoelec focuses on the subject of parity and the role of women in our sector.

The first date corresponds to International Women's Rights Day and the second to International Women in Engineering Day. Nanoelec also actively participates in initiatives relating to the attractiveness of the microelectronics industry, its professions and those of technology as a whole.

To mark International Women in Engineering Day on June 23, 2024, Grenoble Ecole de Management (GEM) produced the "She impacts" podcasts with Siemens EDA, as part of the Nanoelec/Chif program. A webinar style roundtable was also organized on this occasion by Nanoelec, with the Association of Women Engineers, concerning diversity networks in the large companies, broadcasted live on June 28, 2024, with testimonials from CEA, Siemens EDA and HP.

ACTIVE PARTICIPATION BY NANOELEC IN COORDINATING ACTORS IN THE MICROELECTRONICS SECTOR, AT THE CAREERS FORUM IN GRENOBLE ALPES-MÉTROPOLE, OCTOBER 2024

© Laval/CEA

PRESENTATION OF "WOMEN IN TECHNOLOGY R&D" PORTRAITS AT THE GRENOBLE TOURIST OFFICE, ON 5 MARCH 2025, IN COLLABORATION WITH THE AGENCE GRENOBLE-ALPES, RESPONSIBLE FOR THE PROMOTION AND ATTRACTIVENESS OF THE REGION.

© P. Jayet/CEA

THE NANOELEC WOMEN IN TECHNOLOGICAL RESEARCH EXHIBITION WAS PRESENTED AT STMICROELECTRONICS CROLLES AND STMICROELECTRONICS GRENOBLE, ON APRIL 2024

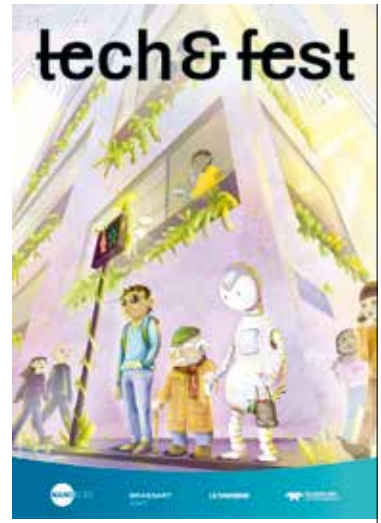
© CEA

Feminization of the workforce

On the occasion of International Women's Right Day, Nanoelec hosted a round-table discussion on the feminization of the workforce in the electronics sector. The debate was moderated by Sandrine Maubert, Deputy Director of IRT Nanoelec, with the participation of: Frédérique Le Grévès, President of the Strategic Committee for the Electronics Sector and President of STMicroelectronics France – Europe (via video conference), Hélène Wehbe-Alause, Research Director at STMicroelectronics Crolles, Florence Robin, Founder and President of Limatech, Anne Roule, Director of the Technology Platform Department at CEA-Leti.

POSTERS TO PROMOTE THE SECTOR

On the occasion of the very first Tech& Fest festival, in February 2024, 45 graphic arts students from the Brassart school took up the challenge from the microelectronics actors in the Alpine region, coordinated by Nanoelec: this was to design a poster on the subject "Microelectronics for living in a better world".



The operation was repeated in 2025: the students from the Brassart school worked on the subject after meeting experts from the various companies in the Nanoelec consortium. Responding to our "commission" as true professionals, the students' proposals reflect society's perception of the microelectronics sector. The best creations selected by a jury of Grenoble-based personalities from the fields of culture, science and industry will be included in a widely distributed catalogue and exhibition throughout the year, helping to raise the profile of our sector across the region. This collaboration with the *Dauphiné libéré* newspaper and the Brassart school enables us to reach out to society, beyond the boundaries of our ecosystem.

—

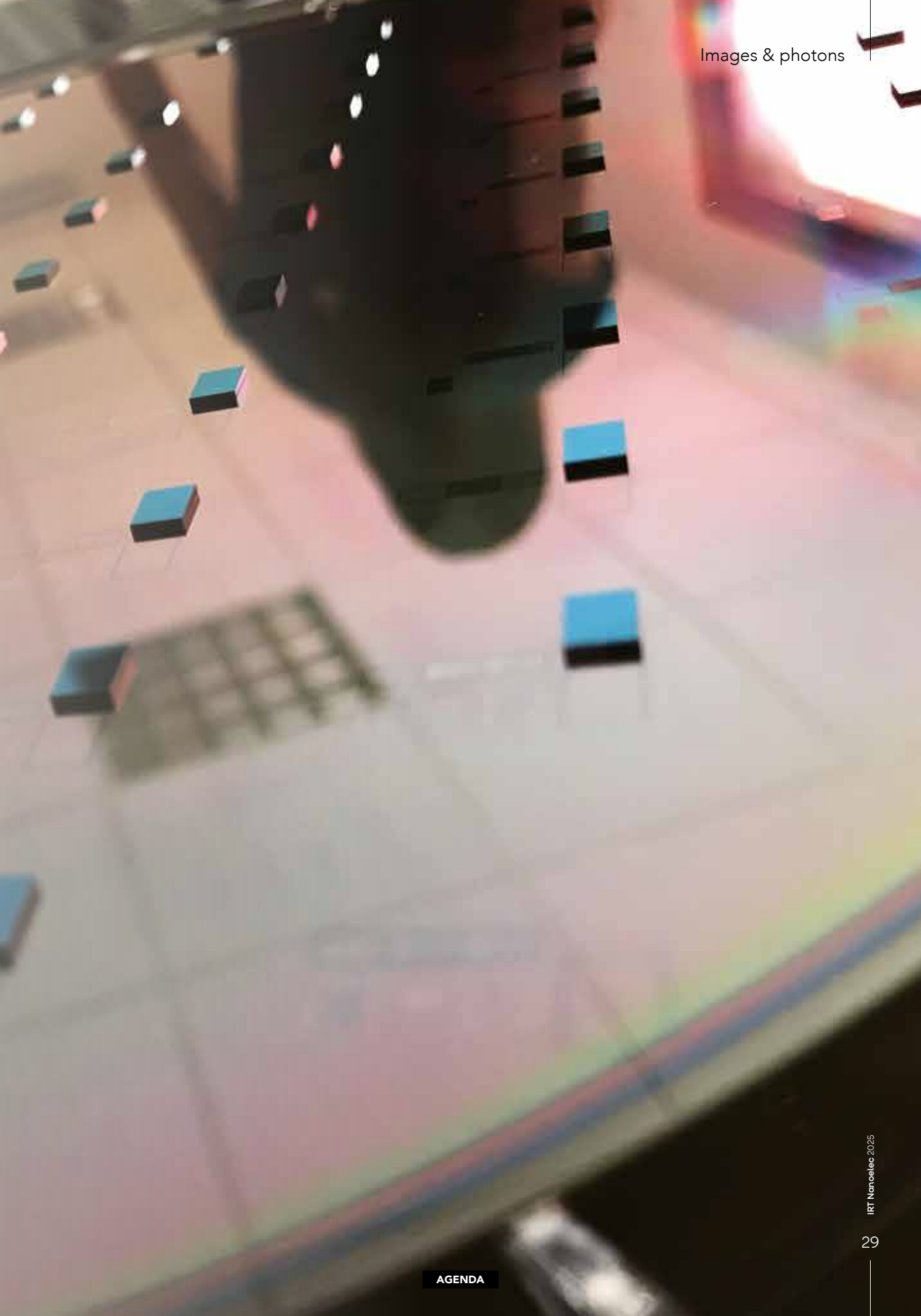
THE EXPERT PANEL SELECTED SEVEN POSTERS AMONG THE CREATIONS FROM THE BRASSART STUDENTS.

Heterogeneous integration

Displed, Smart Imager and Photonic Sensors are all based on the same multi-layer principle, initiated by the 3D integration program during the first ten years of IRT Nanoelec.

Nanoelec is positioned as a French center of excellence in the field of heterogeneous integration, with the capacity to address a variety of application markets, including embedded computing, high-performance computing, imaging, displays, and telecommunications. Heterogeneous integration is a technological solution that paves the way for embedding more AI power in components, with the ultimate goal of enabling learning at the level of the embedded system itself, locally. This will make it possible to offer differentiated solutions. As a result, the amount of data exchanged is reduced, thereby reducing the environmental impact.

Heterogeneous integration is a strong trend in the sector, which will require significant ambitious developments and will meet the expectations of manufacturers and market needs while addressing the challenges of sovereignty in the industry by ensuring that key components and system building blocks are controlled in France and Europe. •



From imaging to visioning

Providing relevant and real-time environment analysis by vision.

© Pixabay

ERIC OLLIER, DIRECTOR OF THE NANOELEC/ SMART IMAGERS PROGRAM

© P. Jayet/CEA

Within the Nanoelec/Smart Imager program, our aim is to develop the technologies needed for the next generation of imagers, which will enable the transition from capturing images to exploiting the information they contain. This exploitation will be performed by the sensor itself, so that it can perceive a scene, understand the relevant situation and intervene on it.

This is a truly disruptive paradigm shift, with the focus shifting to computing and memory challenges, in addition to image generation. The concept includes the implementation of artificial intelligence within the image sensor itself.

In 2024, work continued on developing the key technological building blocks: hybrid bonding, HD-TSV, heterogeneous integration and specific technologies for infrared applications. The development of a "dual damascene" structure is ongoing to improve the hybrid bonding connection. This reduces the number of interfaces between the various levels and thus the total resistance of the interconnections in the 3D stack. Numerous technological improvements have been made to the HD-TSV and have boosted their maturity, while continuing with the scaling roadmap.

Activity to develop heterogeneous integration technologies based on D2W approach grew this year, with the design of a new set of complex masks which will enable interconnection pitch reduction along with the development of different integration architectures. Finally, in-depth study of the use of 3D technologies for IR imager applications led to start developments based on D2W technologies in order to allow access to advanced 300mm CMOS technologies.

New integrated circuit design methodologies are being implemented to meet the two-fold challenge of introducing AI computing functions as close as possible to the sensors. The two design •••

platforms created in 2023 evolved in 2024 with the addition of new CAD design tools, thus completing the design stream for smart imagers.

Our 3D multi-layer integration technology is progressing in terms of maturity and electrical performance: significant technological improvements have been made, integration efficiency has been improved, and more and more wafers are being completed, with improved morphological and electrical characteristics. With regard to electrical performance, the resistance values of the three-layer stack have been reduced and the electrical isolation at HD-TSV level has been significantly improved.Thanks to joint work by CEA and STMicroelectronics, the process design kit (PDK) including the HD-TSV contributions is moreover, place and route process has also been optimized to enable precise 3D design in order to meet performance requirements.

Finally, based on all these developments, 2 functional 3-layer smart imager demonstrators were studied under the program: one called J3DAI is virtual, and the other called EB3D/Tanzanite is slated to reach silicon demonstration level in the coming years. The first one intended for visible applications is based on an STMicroelectronics pixel with an AI accelerator from CEA, while the second one intended for event-based applications is based on a pixel designed by Prophesee. An innovative AI part (GNN) was developed by CEA and Prophesee, with the whole scheduled for manufacture in the STMicroelectronics and CEA cleanrooms. •

SMART IMAGER PROGRAM AT A GLANCE

- **Vision**
  The transition from imagers to vision sensors is generating new market opportunities
- **Ambition**
  To provide key HW and SW building blocks, to validate them through demonstrations ranging from test vehicles and proofs of concept to the prototyping of a smart, multi-layer imager
- **Mission**
  Stacking/3D technologies, embedded AI and data management, new architectures
- **Partners**
  CEA, Lynred, Prophesee, Siemens EDA, STMicroelectronics, Grenoble INP-UGA

3D CHIP MOUNTING AT CEA-LETI

Connecting layers by sharpening through silicon via HD-TSV are now available for multi-layer 3D integration

The demonstration of wafer level 3-layer integration including Face-To-Back (F2B) configuration received an award at the major ECTC 2024 conference. It combines two fine pitch Cu-Cu hybrid bondings with high-density connections up to an operational 3-layer test vehicle.

3D stacks offer multiple advantages for advanced components such as smart imagers and their assembly in a wafer-to-wafer (W2W) approach opens up access to very fine pitch interconnections. While hybrid bonding is commonly used to connect the layers, high-density (HD) TSV are mandatory for the signals to be transmitted through them.

For several years now, a CEA-Leti team has focused on the key enabling technology of TSV for the 3-Layer CMOS image sensors under development at Nanoelec, and every year it publishes several papers to report on its progress at the international ECTC conference.

At IRT Nanoelec, CEA and ST-Microelectronics demonstrated the feasibility of 3-layer stacking in 2023. This major result of the Smart Imager program was presented in the form of three publications at the major ECTC 2024 conference. One of them received a "best paper award" from the professionals.

"After having successfully demonstrated a 2-layer face-to-back (F2B) test vehicle (TV), we reached the next level of integration by achieving a 3-layer TV with fine-pitch Cu-Cu hybrid bonding (HB) technology and high-density (HD) Through Silicon Via (TSV); After demonstrating 3-layer TV functionality, the next step will be to implement this 3D technology in a functional advanced CMOS image sensor (CIS) in the next few years," says Stephan Nicolas, as a first author of the paper receiving the award.

"The 3-layer demonstrator is one of Nanoelec's major technological achievements," underlines Alexis Farcy, R&D Process Development Engineer - 3D Integration at STMicroelectronics. *"The three-layer structure will enable the image sensor to be equipped with an artificial intelligence function, which necessarily requires a lot of computing power and memory. Hybrid bonding has already been well developed as part of Nanoelec's programs since 2012. It is now industrial. And from there, the new building blocks of the Smart Imager begin. For us, these morphological and electrical results validate these building blocks, which are really the key elements that will now enable us to move on to the physical relationship of a much more ambitious functional demonstrator."*

—

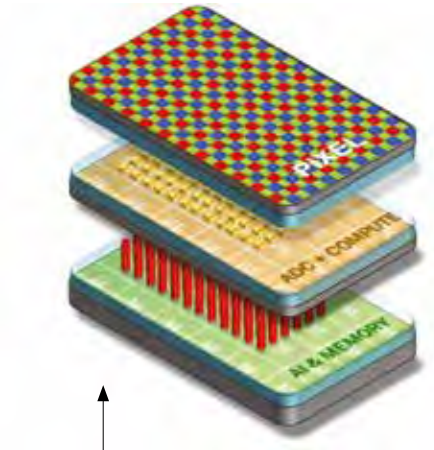
FIB-SEM 3D CROSS-SECTION OF THE 3-LAYER TEST VEHICLE - PITCH IS 6 µm FOR THE BONDING PADS - HD TSV DIMENSIONS ARE 1X10µm.

© CEA

> ***"For several years now, a CEA-Leti team has focused on the key enabling technology of TSV for the 3-Layer CMOS image sensors under development at Nanoelec..."***

In-sensor computing for event-based imaging

On the occasion of the Nanoelec 2024 General Meeting, Pascal Vivet, CEA-Leti, reviewed the development of event-based imagers equipped with artificial intelligence.



SCHEMATIC OF A 3-LAYER SMART IMAGE SENSOR, WITH EMBEDDED AI

© P. Jayet/CEA

Why develop event-based sensors?

P.V. Event-based imagers allow very high-rate acquisition of images, in that only the pixels which record a variation contribute to the data stream. The target applications are augmented reality, typically tracking of the hand, the eyes, gestures, presence tracking or detection.
Sensors incorporating AI functions are already available on the market, but our 3-layer concept offers greater performance and a wider range of applications. We start from an event-based 2-layer imaging architecture available at Prophesee. We propose adding a third electronic layer which will be strongly coupled to the imager. This third layer supports AI functionalities and this is called in-sensor computing.

What are the development constraints for such a very small sensor?

P.V. In Nanoelec/Smart Imager program, we are developing both the hardware part and the AI software highly optimized to reduce energy consumption and computing times. It will be possible to make extremely small objects capable of monitoring our environments at very low cost and running on batteries. Our sensor will measure barely more than one cubic millimeter, and will thus easily be installed in the limited space available inside a smartphone. Its electrical consumption is very low and its processing latency, that is acquisition and processing with embedded AI, will be about one millisecond. This project is the result of active collaboration, in which Prophesee provides the core of the 2-layer imager, CEA proposes and implements the specific AI accelerator in the third layer, Siemens EDA supplies the design tools (behavioral synthesis, DFT, sign-off), and STMicroelectronics participates in logical and physical implementation of the final circuit. The manufacturing of the demonstrator will use both STMicroelectronics and CEA-Leti clean-rooms

How to embed AI directly in the image sensor?

P.V. In an event-based imager, the principle is to generate a pixel event when there is a change in contrast. In this case, standard AI solutions are not easily applicable. The traditional Convolutional Neural Networks (CNN) used in AI mean that the image and the pixels must be integrated in time, which loses information on the precision of the events. SNN (Spiking Neural Network) type networks, based on spikes, even though closer to the nature of the pixel events, are not suitable as a type of coding. A network structure based on GNN (Graph Neural Network) was proposed to encode the sparsity of pixel events, while retaining an efficient computing method. The HUGNet processing architecture, based on GNN, was proposed, as it can be used to process different types of AI algorithms (monitoring, tracking, recognition, classification, etc.), with unparalleled memory and computing performance (> x100) by comparison with the best CNN solutions that could be imagined with an event-based sensor. The algorithm core was developed in 2024, a first high-level architecture model was developed at the end of 2024, and development of the RTL hardware building block is ongoing in 2025, with the circuit being sent for manufacturing at the end of 2025.

PASCAL VIVET, FORMER SCIENTIFIC DIRECTOR OF THE DIGITAL CIRCUITS AND ARCHITECTURES DEPARTMENT AT CEA-LIST

© Jayet/CEA, 2022

SÉBASTIEN THURIES, DEPUTY DIRECTOR OF NANOELEC/SMART IMAGER PROGRAM

Date Conference 2024

In April 2024, at the reference international conference in the field of circuit design, DATE[1], the Nanoelec/Smart Imager program teams took part in organizing a workshop on the challenges of 3D, more particularly in the field of imagers.

Sébastien Thuries, engineer at CEA-List and Deputy Director of the Nanoelec/Smart Imager program, presented the benefits of multi-layer technology for developing an image sensor with a low energy footprint.

"We are progressing in terms of silicon production with respect to integration of a third silicon wafer, thanks to Through Silicon Vias (TSV) at very high density (~1µm on a side)," he explains. *"The circuit design methodologies are also evolving and a suite of tools (design, simulation and verification) benefited from the circuits developed in the program."* Two circuits were presented, one for imaging in the visible spectrum and the other for event-based imagers: J3DAI, a multi-layer circuit with integrated AI accelerator for rapid and efficient processing of the AI algorithm, and HUGNet, also a multi-layer circuit for AI processing dedicated to the event-based imager thanks to the Graph Neural Network (GNN) and offering results several orders of magnitude better than traditional Convolutional Neural Networks (CNNs).

AGENDA

1. Date Conference, March 25 – 27, 2024 | Valencia, Spain

Characterization, Modeling, and Reliability for Direct Copper Interconnection

Hybrid bonding technology.

Stéphane Moreau, a senior expert at CEA-Leti in the field of integrated circuit interconnect reliability, and Dongkai Shangguan, an IEEE Fellow & IMAPS Fellow and President of Thermal Engineering Associates, Inc. and a strategic advisor to innovative companies in the global semiconductor and electronics industry, have written a book chapter addressing the advances and challenges related to "Direct copper interconnections for advanced semiconductor technologies".

They reviewed the most significant qualification and reliability achievements for hybrid bonding-based interconnects over the last ten years by the industry and the scientific community. An overview of 3D interconnects and their evolution, failure mechanisms, and related accelerated tests and associated standards for 3D packaging technology are analyzed. A discussion follows on the qualification and reliability testing results of the hybrid bonding technology by the industry and the scientific community. This book chapter is completed by a review of numerical simulation studies covering bonding physics, electrical and thermal performance and the reliability of hybrid bonding technology.

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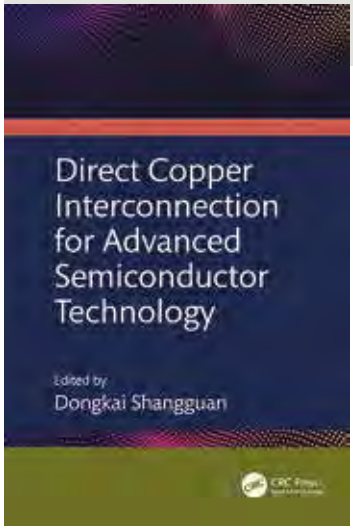

> ***An overview of 3D interconnects and their evolution, failure mechanisms, and related accelerated tests and associated standards for 3D packaging technology are analyzed.***

Copper interconnections within cryogenic systems

Assessing robustness and electrical performance of copper HD-TSV at low temperatures.

A study led by CEA-Leti scientists evaluates copper High Density-Through Silicon Vias (HD-TSVs) in cryogenic environments, which are crucial for applications like quantum computing and astrophysics. The use of HD-TSVs notably allows for increased signal density, enabling device scaling. *"1,980 thermal cycles between 344 K and 77 K were conducted to assess the mechanical and electrical robustness of HD-TSVs to cryogenic conditions,"* explains Stéphane Moreau, as first author of the paper published in IEEE Electron Device Letters.

Additionally, one thermal cycle was carried out in a cryostat down to 2 K. In-situ and ex-situ electrical measurements show remarkable stability in the electrical resistances of the tested structures with a variation of less than ±3%, even after 1,980 thermal cycles. *"Our results confirm the robustness and electrical performance of copper HD-TSV at low temperatures, opening up prospects for their integration within cryogenic systems,"* Stéphane Moreau adds.

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Towards Display Technology Leadership in Europe

NATACHA RAPHOZ, NANOELEC/DISPLED PROGRAM DIRECTOR

© Havret/CEA

MicroLED technology is revolutionizing the field of displays by offering exceptional image quality and immersivity, with display sizes ranging from smartphones to large TVs.

The Nanoelec/Displed program uses Smart-Pixel technology, a patented key technology which paves the way for the manufacture of displays based on new display concepts in Europe.

The goal is to produce extremely bright micro LEDs and assemble them with an underlying control circuit, broken down into very high performance pixels. We use techniques for hybrid bonding of different materials, as well as LED cutting to mount them onto the display support, with extreme precision, high density and high speed: this is the "mass transfer" challenge.

In 2024, the change in Aledia's market access strategy led to work being focused on large pitch 2D-LED technologies, while the small pixel, high-resolution 3D LEDs sector focused on blue smart-pixels.

Given the changing market demands, in 2024 the partners decided to focus their efforts on integration of the 200mm process in order to speed up its industrialization. We are thus developing a low-temperature process for hybrid bonding in order to tap new and promising markets. We are also exploring new solutions for very high-end displays, notably flexible ones. •

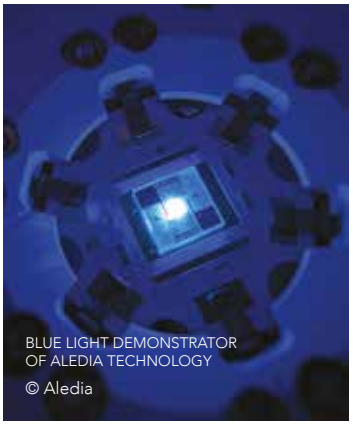
AGENDA

TESTING MACHIN FOR MASS TRANSFERT OF THE MICROLED
© Havret/CEA

The first LED light

In 2024, Aledia achieved its very first LED light-up with the process at Champagnier.

This first LED light-up has promising performance homogeneity and a VF (applied voltage) decrease at 3V.
Nanoelec's partners are collaborating to design and develop a high-end Virtual Reality glasses solution, using 2D smart pixel. The prototype was presented at the Eurodisplay 2024 symposium in Grenoble.



BLUE LIGHT DEMONSTRATOR OF ALEDIA TECHNOLOGY
© Aledia

Mass Transfer

The radically new techniques developed within Displed allow high-volume collective chip mounting with high-precision alignment.

At the Nanoelec general meeting in November 2024, Abdenacer Aitmani, a researcher at CEA-Leti working on the Nanoelec/Displed program, recalled the advantages of microLEDs. •••

DISPLED PROGRAM AT A GLANCE

- **Vision**
  A unique opportunity for a French & European ecosystem on large display technologies for immersive applications
- **Ambition**
  To design and demonstrate key microLED technologies for high-end, immersive displays
- **Mission**
  To develop process flows for microLED, Smart-Pixel fabrication and mass transfer onto the display
- **Partners**
  Aledia, CEA, EVGroup, SET

"In terms of brightness, this is the highest performance technology today available. This can create displays which remain legible even when exposed to direct sunlight, he explained. If packaged in optimal conditions, microLEDs can then function for 40,000 or even 50,000 hours, which smashes all lifetime records by comparison with existing light sources!".

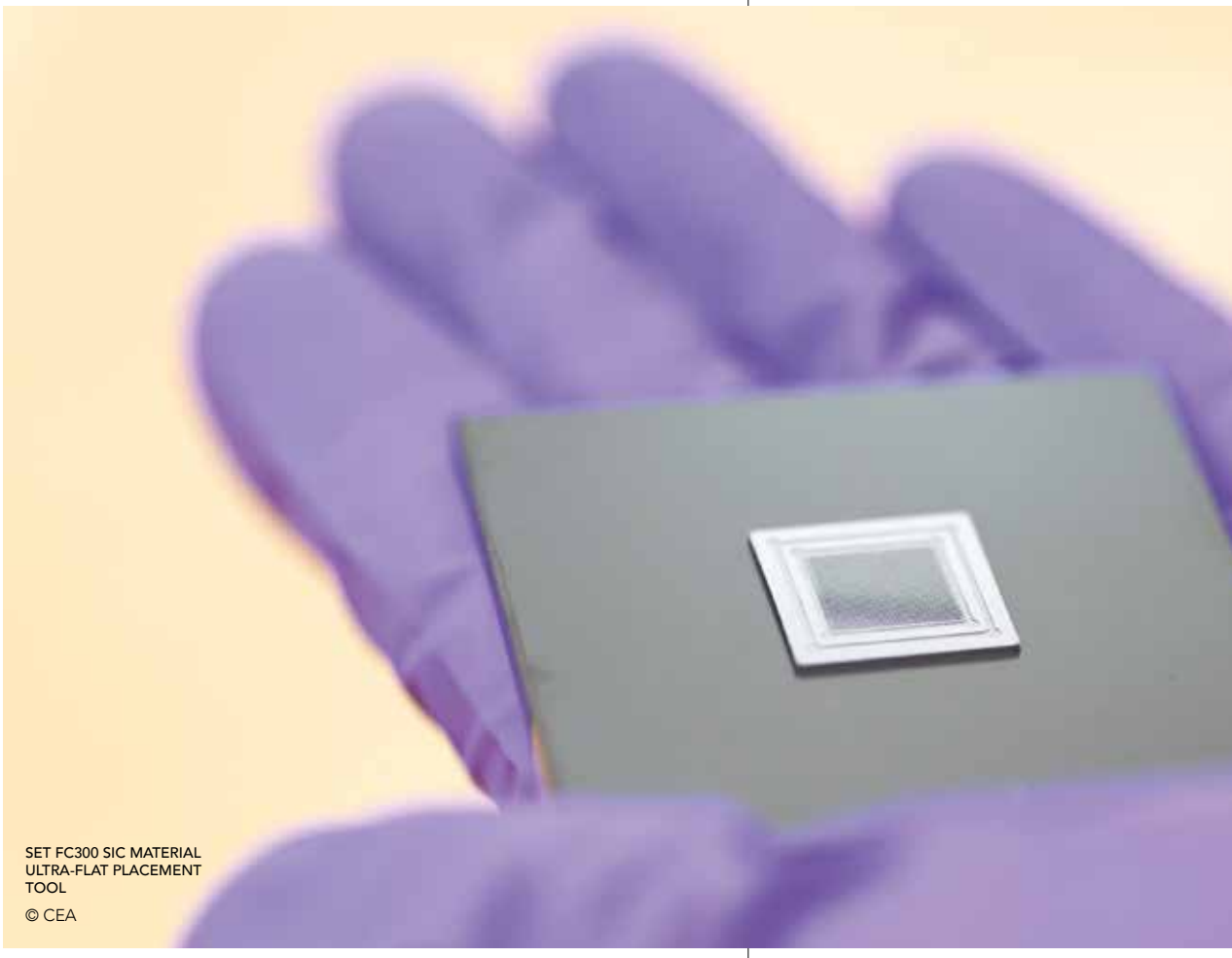
Abdenacer is more particularly interested in transfer to the display support, which is one of the major challenges for industrial deployment. *"A large number of chips have to be transferred, rapidly,"* he points out. This is the technological hurdle known as mass transfer.

"Let's take the example of a display, I would say an equivalent 8K[1] display. Today, if we wanted to manufacture it with microLEDs, based on gallium nitride, and if we assume three chips (red, green and blue), plus the related operations, that would mean more than 100 million chips to be transferred to the display, according to Abdenacer's calculations. Even if the most sophisticated automated instruments can achieve 100,000 components per hour, that's not enough to obtain an end-product that is economically affordable for the public."

As part of the Displed program, the SET and EVG companies, along with CEA, are developing strategies for handling brighter chips and placing them rapidly on the display support.

"These operations must be performed with no chip losses, no alignment errors and no damage to the chips being handled." The process must also enable defective chips to be replaced: *"Just think, you are transferring millions of chips and five or six of them are defective, you would be unable to sell that display,"* adds Abdenacer. •••

1. According to Samsung's definition, an 8K television has a display consisting of 7,680 horizontal pixels and 4,320 vertical pixels, or a total of almost 33 million pixels.



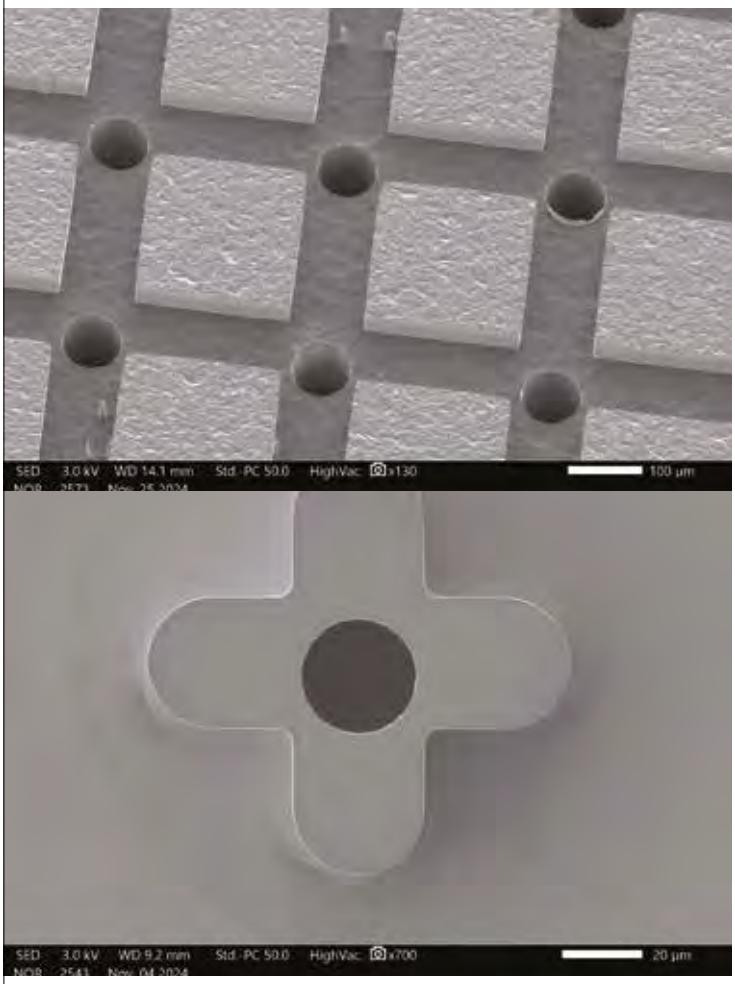
SET FC300 SIC MATERIAL ULTRA-FLAT PLACEMENT TOOL

© CEA

The radically new techniques developed under Displed allow high-speed, collective chip mounting with high-precision alignment.The processes developed could thus make it possible to take hundreds, thousands or even tens of thousands of chips at a time.

"All these tasks are the preliminary steps needed to develop the industrial equipment essential to the deployment of a display production industry in France or in Europe," concludes Abdenacer.

HANDLING MICRO-TOOL FOR MASS TRANSFER OF MICROLEDS
© CEA



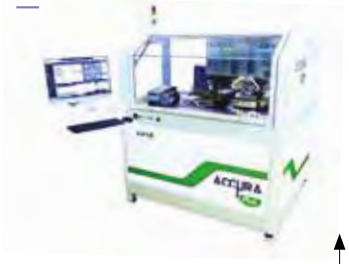
Abdenacer Aitmani, researcher at CEA-Leti for the Nanoelec/Displed program, inspects prototype large-scale chip transfer tools

Frédéric Berger (CEA-Leti) testing new tools for mass transfer of microLEDs

Vacuum bonding of LED chips

Within Nanoelec, SET and CEA teams have used equipment from their portfolio to test transfer of small dies, individually and collectively.

"We're developing a silicon micro-tool, in which holes are made, which suck in many chips at once and move them from an original wafer to a display," explains Pascal Metzger, Managing Director of SET. The first-generation vacuum-based micro-tool for mass transfer of microLEDs is undergoing testing on an upgraded version of the SET-FC300 tool. *"We have already obtained some encouraging proofs of concept, handling individual tiny chips. To improve accuracy pick-up for smaller dies, we have modified the entire closed-loop system of the robot on one of our machines, adds Pascal Metzger, Our goal is to finish the R&D phase by end of 2025, and then 2 or 3 years to start prototyping and industrialization."* The redesign of the robot of the SET/ACCµRA Plus has achieved better placement accuracy of the dies, as required by their tiny dimensions and the small pitch. The results are encouraging, either when handling one single die, or performing mass transfer. All these experiments will be continued in order to adjust the different parameters for efficient mass transfer and optimized bonding.



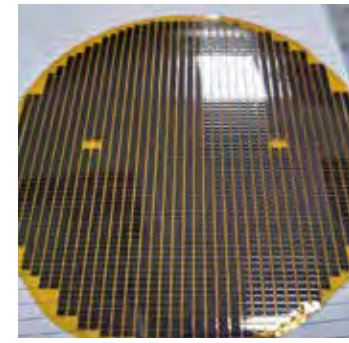
ACCµRA PLUS FROM SET IS USED TO TEST THE PICK-AND-PLACE STRATEGY FOR THE MASS TRANSFER OF DIES

© SET

The move to flexible displays

Advanced applications of the Smart-pixel microLED displays concept, such as flexible displays, or the new functionality based on the addition of sensors, are truly promising.

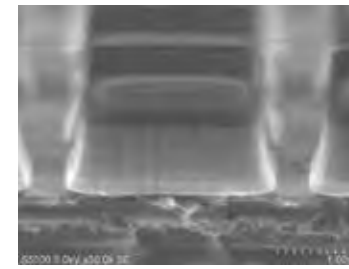
The Augmented Reality market is notably the most demanding in terms of performance. The teams involved in the Displed program identified the design and technical challenges for development, such as pixel-pitch reduction, high-density interconnects reliability. Specimen wafers based on a new process flow have been prepared by CEA-Leti and delivered to Aledia in 2024.



Nanoscale layer etching

A tool capability to etch GaN-based µLEDs has been tested: one process was implemented, based on inputs from Lam Research.

The tool supplier Lam Research and Nanoelec collaborate on a joint development program aimed at advancing nanoscale layer etching processes for a wide range of applications from GaN microLEDs to materials used in RF devices and MEMS.
One process evaluated using Lam Research equipment is the etching of a GaN-based µLED stack, preventing damage to the underlying aluminum contact layer. The landing capability has been successfully demonstrated despite the minimal etch rate difference between Al and GaN.



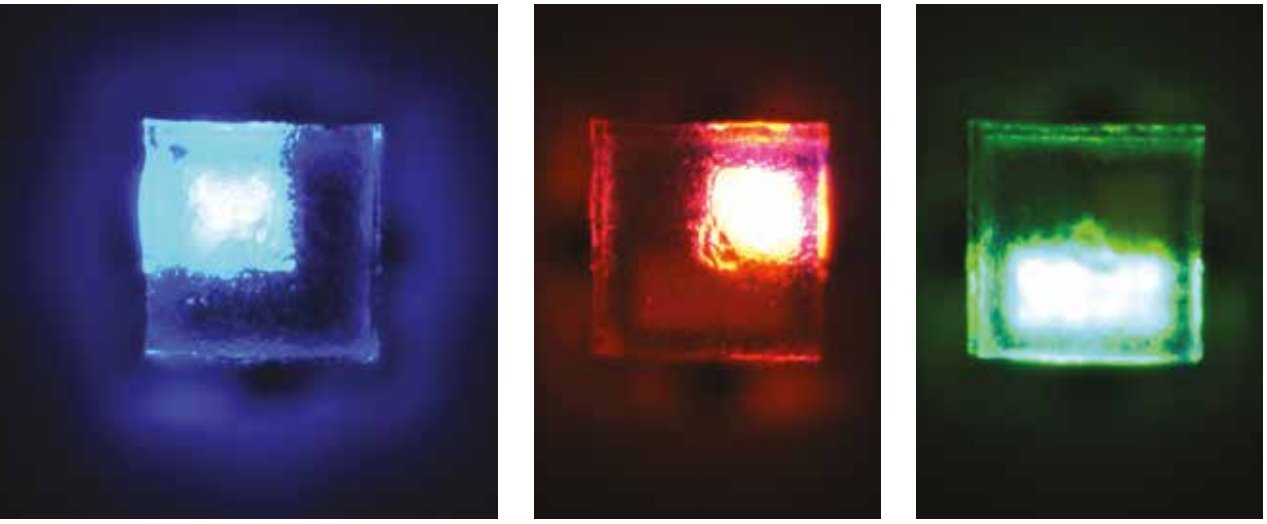
© Lam Research

Blue digital LED product

In 2024, Aledia built a demonstrator including a matrix of new-generation 2D-LED Smart Pixels on a fully operational PCB. Severine Cheramy, Product Line Manager at Aledia, presented results at two international conferences[2].

"Active-matrix BLU using Aledia Blue Digital LED is now demonstrated as a possible solution for Virtual Reality applications, and other high-end BLU LCDs could also benefit from it in the medium term," commented Séverine after the Touch Taiwan conference (April 2024).
The Aledia Digital LED Manufacturing Roadmap was presented, including the present ramp-up for the production of the blue digital LED product.

2. LIDs (Grenoble, June 2024) and Touch Taiwan (Taipei, April 2024).



FOR THE DEMONSTRATION OF FULL-COLOR UNITS, THE TEST VEHICLE IMPLEMENTED BY ALEDIA TEAMS SHOWED BLUE EMISSION COMING FROM THE NANOWIRES, AND GREEN AND RED EMISSION BASED ON QD CONVERSION

© Aledia

Full-color unit demonstrator

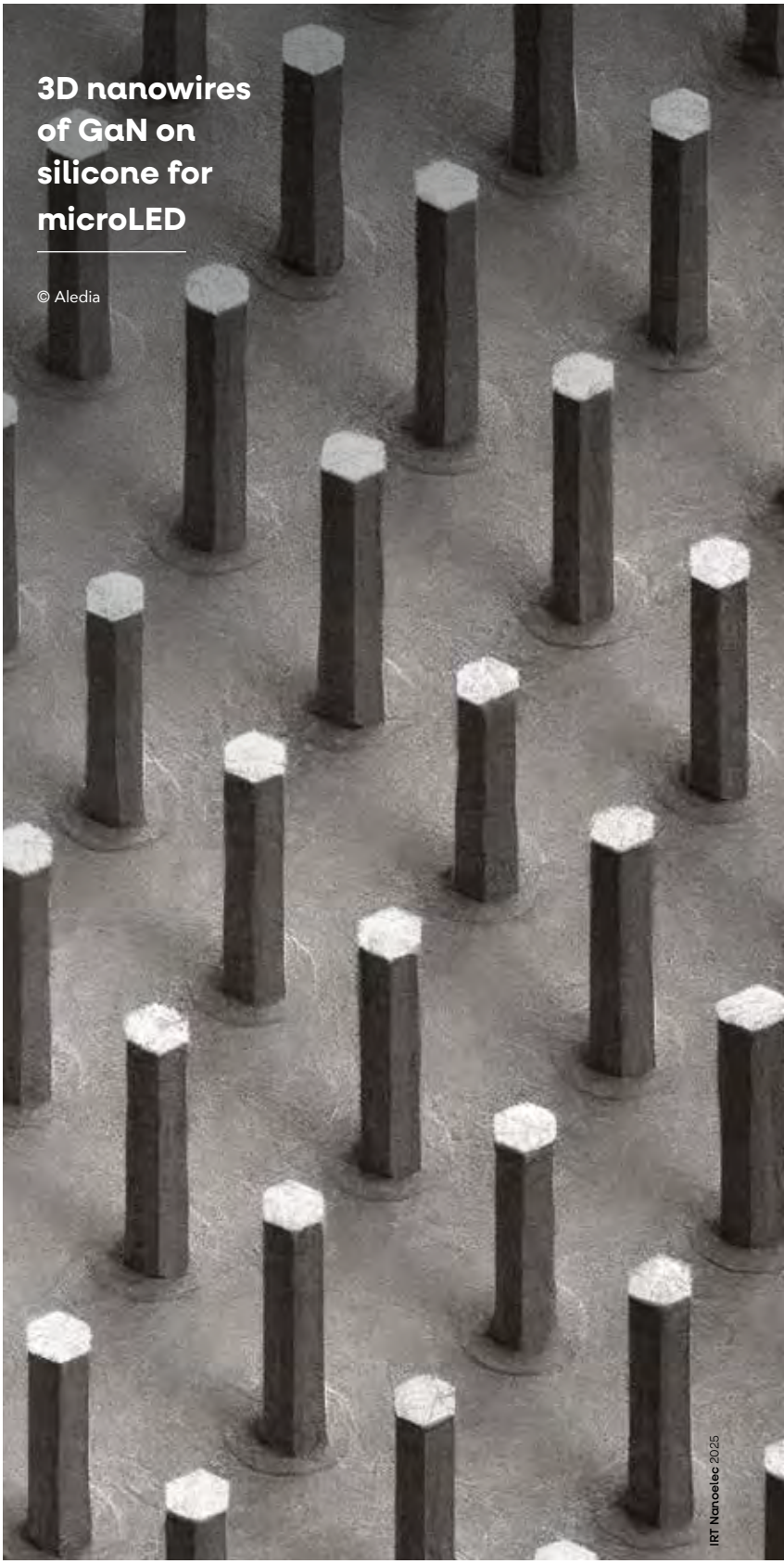
A demonstrator including a matrix of new-generation 2D-LED Smart-Pixels on a PCB is fully operational and major improvements have been obtained on the roadmap towards 300mm microLED production.

LED growth on the 300mm MOCVD system installed at Aledia/Echirolles showed an emission wavelength centered on 446.4nm with very low standard deviation among the LEDs.
3D-LED Smart-Pixel process integration was successfully demonstrated, involving two metal levels, hybrid bonding and backside grinding. For the demonstration of full-color units, the test vehicle implemented by Aledia teams showed blue emission coming from the nanowires and green and red emission based on QD conversion.

Production building now completed at Champagnier

In 2024, Aledia completed construction and installed 25 systems in the Champagnier plant (SDM). The plant now has 34 machines installed.

IRT Nanoelec 2025



3D nanowires of GaN on silicone for microLED

© Aledia

IRT Nanoelec 2025

New opportunities based on large-scale 300 mm silicon photonic technologies

The aim of the Nanoelec/ Photonic Sensors program is to produce a complete range of solutions designed to facilitate the adoption of photonics on silicon by new applications requiring complex detection functions, such as 3D detection in mobile phones, self-driving vehicles, or biochemical detection for health care purposes and environmental monitoring.

STÉPHANIE GAUGIRAN (CEA), HEAD OF THE NEW PHOTONIC APPLICATIONS SECTION AT CEA-LETI & DIRECTOR OF THE NANOELEC/PHOTONIC SENSORS PROGRAM

The main key technological challenges for this type of sensor are measurement precision, miniaturization, data processing and transfer and compatibility with mass production. The unique properties and performance of integrated photonics are essential in meeting these challenges.

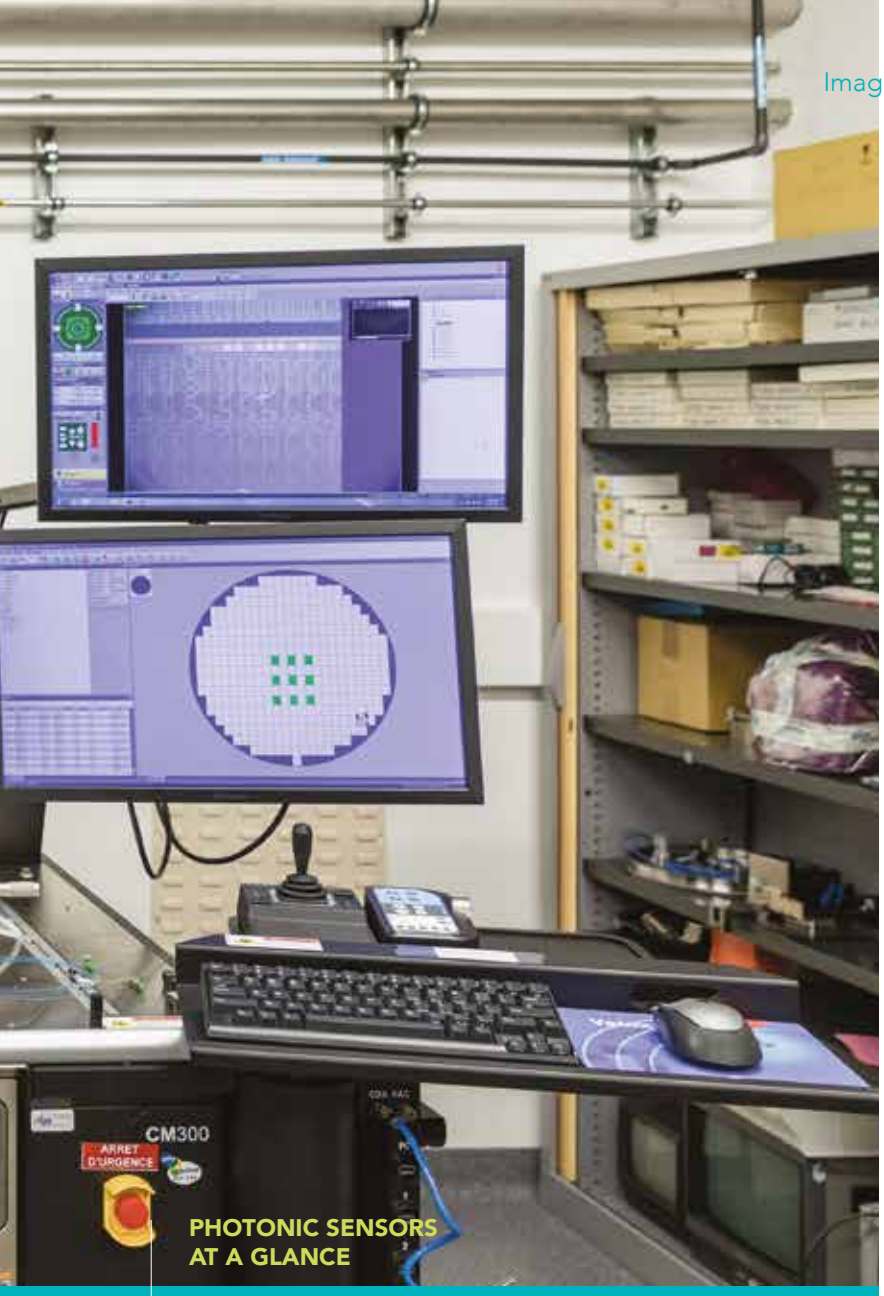
In 2024, a first demonstration of ethanol detection without substrate functionalization was performed using a two-wavelength Mach Zehnder interferometer. Initial results are highly promising.

Our teams performed a study of a physical phenomenon limiting long-range LIDAR applications, which require high power levels: the non-linear two-photon absorption (TPA) phenomenon. The process was transferred to STMicroelectronics at the end of the year.

Work on very low loss SiN guides improved the platform's results and its performance is now world-class.

Finally, the year was marked by the production of the 300mm laser batch and the first structures were successfully tested. •

AGENDA



PHOTONIC SENSORS AT A GLANCE

➜ **Vision**
New sensor opportunities based on large-scale 300mm silicon photonic industrial technologies

➜ **Ambition**
Provide the Nanoelec partners with a complete chain of solutions – from EDA to mass production – designed to facilitate the adoption of photonics on silicon by new applications requiring complex detection functions such as 3D detection in mobile phones, autonomous vehicles, or biochemical detection for health care and environmental surveillance

➜ **Mission**
Our main technological challenges for such sensors are measurement precision, miniaturization, data processing and transfer, and also compatibility with mass production. The unique properties and performance of integrated photonics are essential in being able to meet these demands and these challenges

➜ **Partners**
Almae, CEA, CNRS, Siemens EDA, STMicroelectronics

MZI based ethanol detection

CEA is developing an application measuring the ethanol concentration using an MZI without functionalization on the STMicroelectronics platform, within Nanoelec.

Measurements down to 0.2% alcohol concentration in water were achieved, with a detection limit evaluated at 0.025%. A CMOS photonics on silicon interferometer allows measurement of very small quantities of liquid. The application could be of interest to the agri-food industry and the health care sector.

Millimeter-length antennas for optical-phased arrays

Improving the scanning accuracy.

A team gathering scientist from CEA, STMicroelectronics, C2N (CNRS & Université Paris-Saclay) studied the behavior of mm-long BIC-effect and dual-layer antennas for silicon photonics based optical phased-arrays (OPAs).

"The designed and fabricated antennas are simulated and characterized in terms of divergence and directivity in order to achieve precise scanning of the environment," underlines Louise-Eugénie Bataille (STMicroelectronics) as first author of the paper awarded as the "IEEE Silicon Photonics Conference 2024 - Best Student Paper"[1].

In further work, BIC-effect and dual-layer Si-SiN SWGAs will be integrated in active OPA with carrier depletion phase control. The apodisation of the gratings period is foreseen for next designs. *"This should confirm the potential of scanning the environment with mm long SWGAS in order to expand the OPA to several hundreds of channels and improve the scanning accuracy of OPA-based sensing applications,"* concludes Louise-Eugénie Bataille.

—

Laser integration

Silicon photonics technology and devices for machine learning.

Benoît Charbonnier & al. (CEA-Leti) demonstrated how silicon photonics for AI is suited to use cases where high computational speed is required.
"CEA Leti's SiPho platform offers state of the art performance for photonic accelerators," underlines Benoit Charbonnier. *"In the future, wafer scale (spiking) laser integration could be a good candidate to support full analog neural networks."* These results were presented at Photonic West (January 2024, San Francisco, USA), the conference attracting more than 24,000 attendees from 70 countries.[2]

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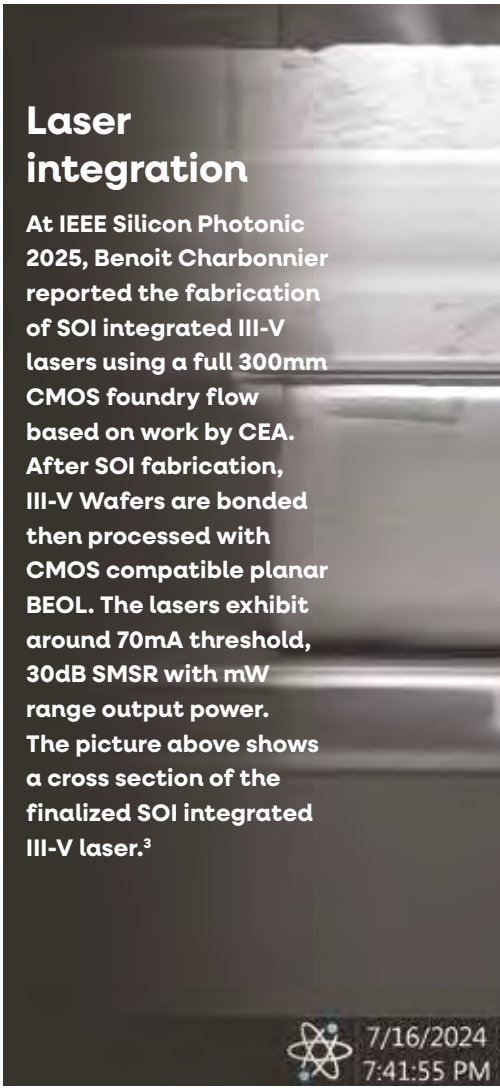


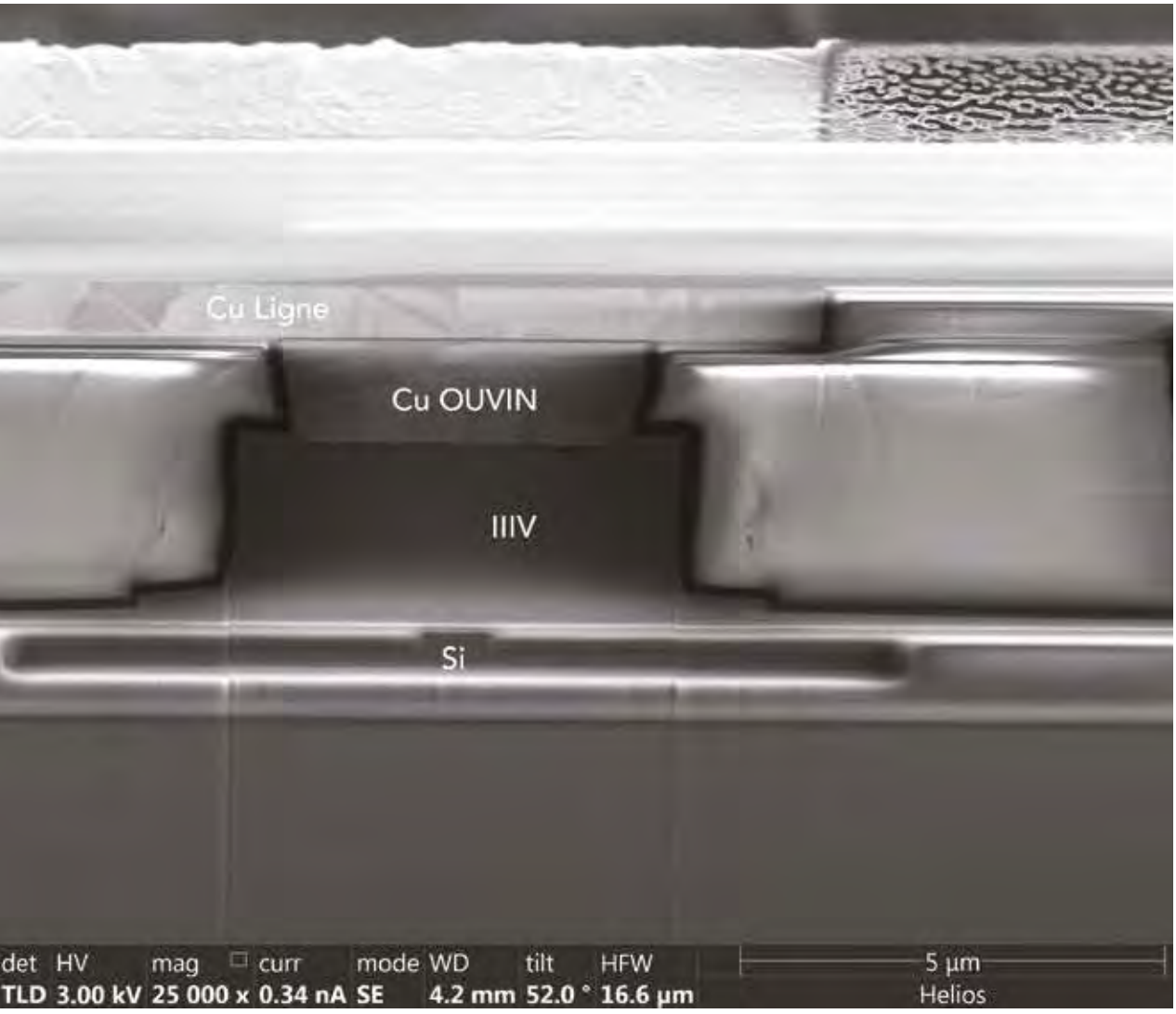
Laser integration

At IEEE Silicon Photonic 2025, Benoit Charbonnier reported the fabrication of SOI integrated III-V lasers using a full 300mm CMOS foundry flow based on work by CEA. After SOI fabrication, III-V Wafers are bonded then processed with CMOS compatible planar BEOL. The lasers exhibit around 70mA threshold, 30dB SMSR with mW range output power. The picture above shows a cross section of the finalized SOI integrated III-V laser.[3]

1. Silicon Photonics Conference (SiPhotonics, April 2024, Tokyo, Japan).

2. Charbonnier, B., Malhouitre, S., Ramez, V., Bellemin-Comte, A., Ribaud, K., Coppola, G., Faure, T., Dafonseca, J., Thibon, T., & Jany, C. (2024, janvier 30). Silicon photonics technology and devices for machine learning. Photonic West.

3. Charbonnier, B., Bellemin-Comte, A., Adelmini, L., Mathieu, V., Stigliani, M., Castan, C., Philip, P.-E., Hebras, D., Hartmann, J.-M., Ribaud, K., Szelag, B., & Hassan, K. (2025). 300mm IIIV on SOI laser integration process, fabrication and prototyping. 2025 IEEE Silicon Photonics Conference (SiPhotonics), 1-2. https://doi.org/10.1109/SiPhotonics64386.2025.10985732



GaAs for photonic and optoelectronic devices

III-V monolithic integration on silicon compatible with CMOS processes.

The integration of III-V compound semiconductors on a silicon platform has emerged as a transformative approach to enhancing the performance and functionality of photonic and optoelectronic devices.

A team from CNRS/LTM, CEA, Grenoble INP-UGA and UGA associated within Nanoelec presented recent achievements, challenges, and future prospects of GaAs monolithic integration on silicon with specific focus on the development of near-infrared (NIR) emitters and photodetectors. *"We address the challenges associated with III-V monolithic integration on silicon and its compatibility with CMOS processes. These challenges include lattice mismatches, thermal management, and process scalability,"* explains Thierry Baron (CNRS/LTM) as first author of the paper presented at Smart Photonic and Optoelectronic Integrated Circuits 2024 (January 2024, San Francisco, California).

The latest results were obtained on near-infrared resonant cavity enhanced photodetector and light emitting devices integrated onto a nominal Si(001) substrate. *"The device structures have been optimized by incorporating active regions based on InGaAs/GaAsP strained-layer super-lattices and GaAs/AlGaAs distributed Bragg Reflectors. We also show an alternative solution for fabricating low-threshold emitters based on III-As membranes and lateral injection devices,"* Thierry Baron says.

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MZI based ethanol detection

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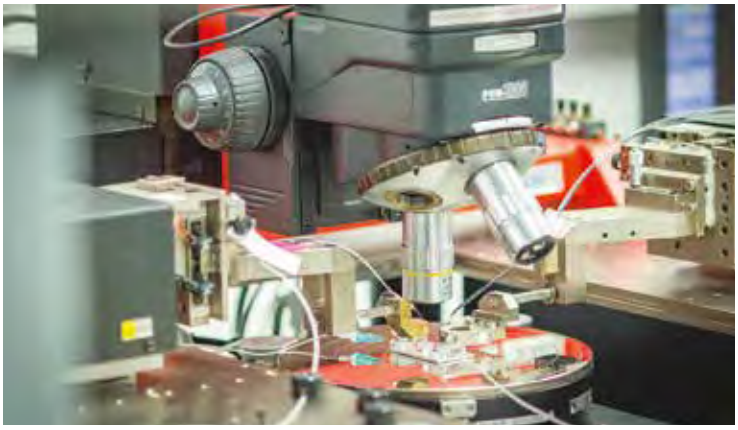

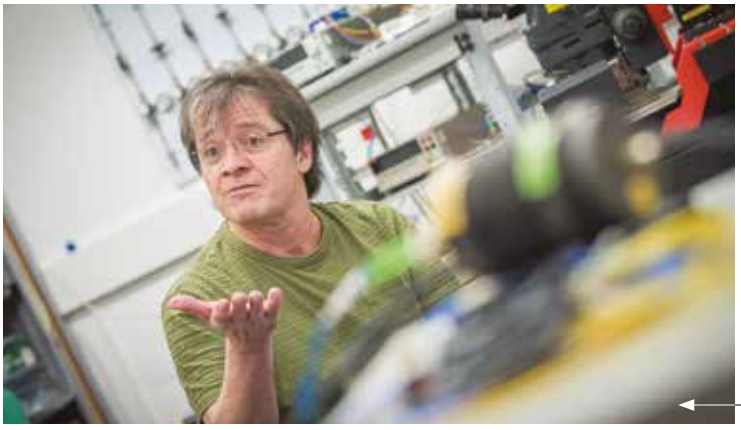

PIERRE LABEYE (CEA-LETI), DEVELOPING A SENSOR FOR ALCOHOL DOSE TITRATION

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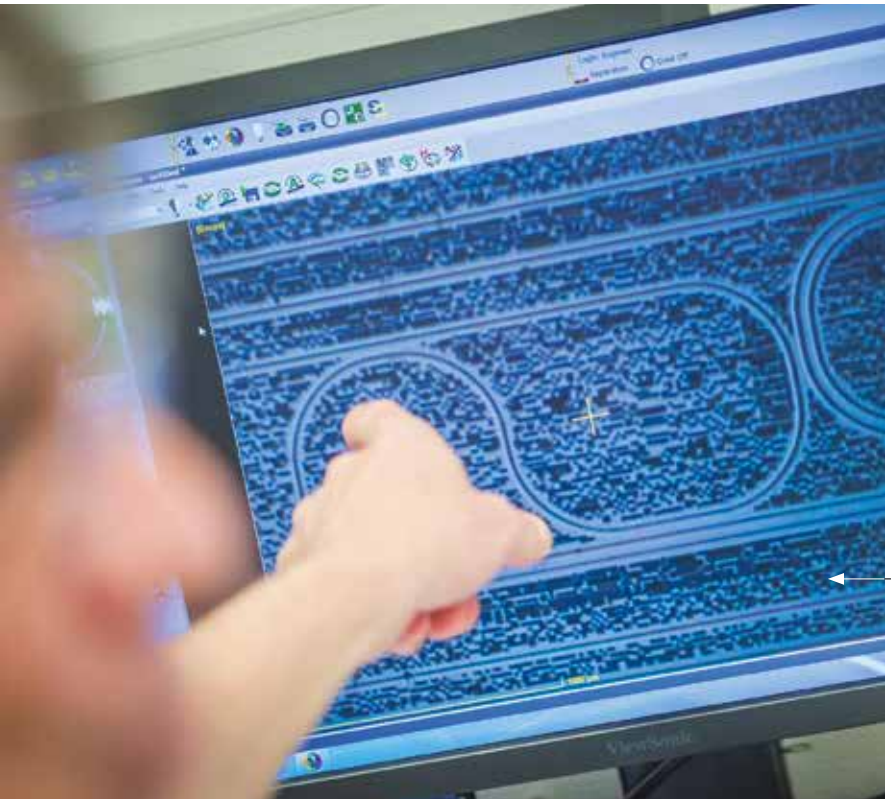
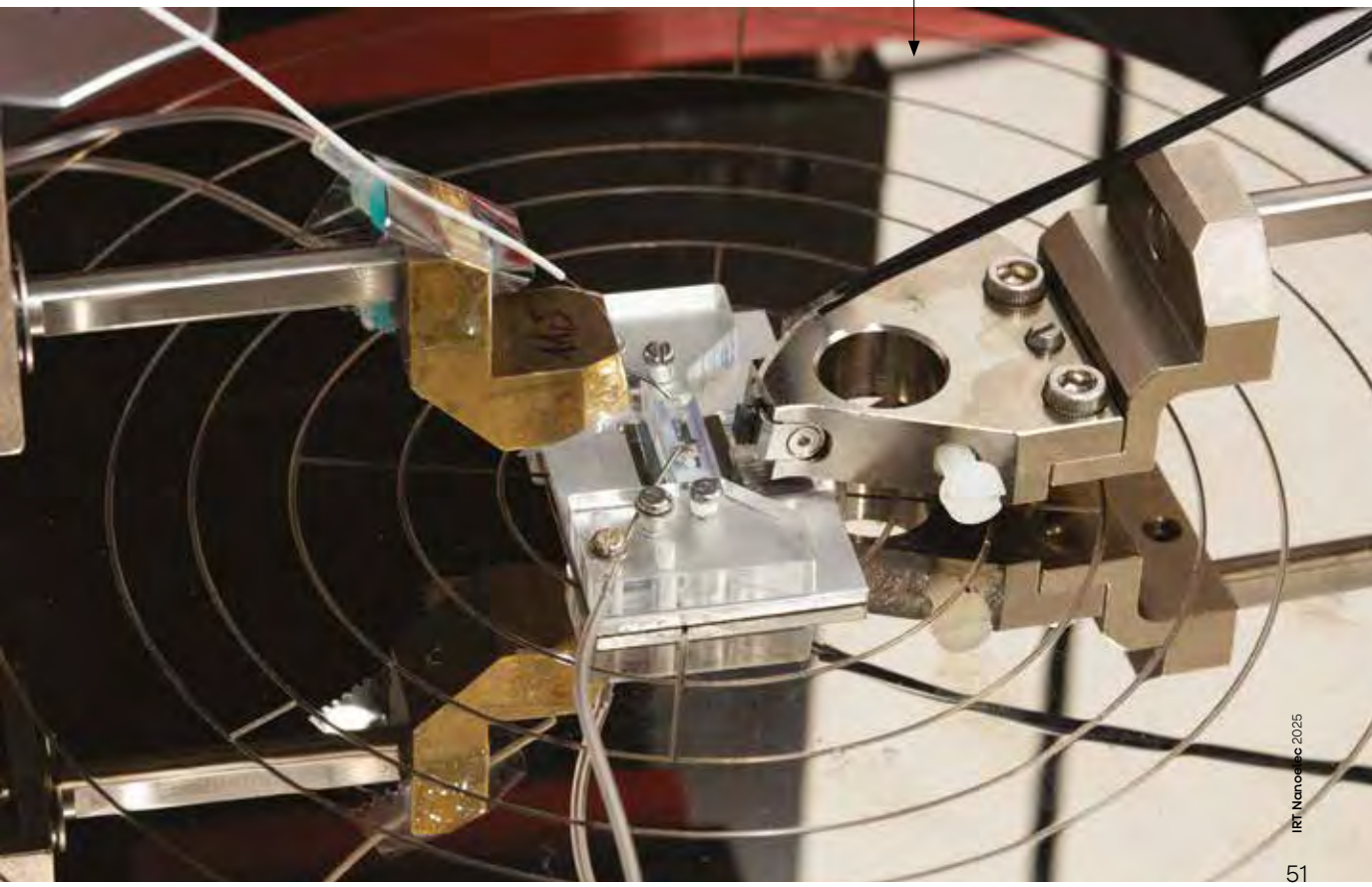


MICROSCOPE VIEW OF THE PHOTONIC MZI CIRCUIT DESIGNED AND PRODUCED AT CEA-LETI FOR ALCOHOL DOSE TITRATION

TESTING THE VERY FIRST PROTOTYPE OF A PHOTONIC SENSOR FOR ALCOHOL DOSE TITRATION



Micro light-emitting diodes

How to Enhance MicroLED Performance.

Within Nanoelec, a team from CEA, CNRS and the Public University of Navarre conducted a synoptic review of III-V Semiconductor Technology to enhance performance of micro light-emitting diodes (microLEDs).

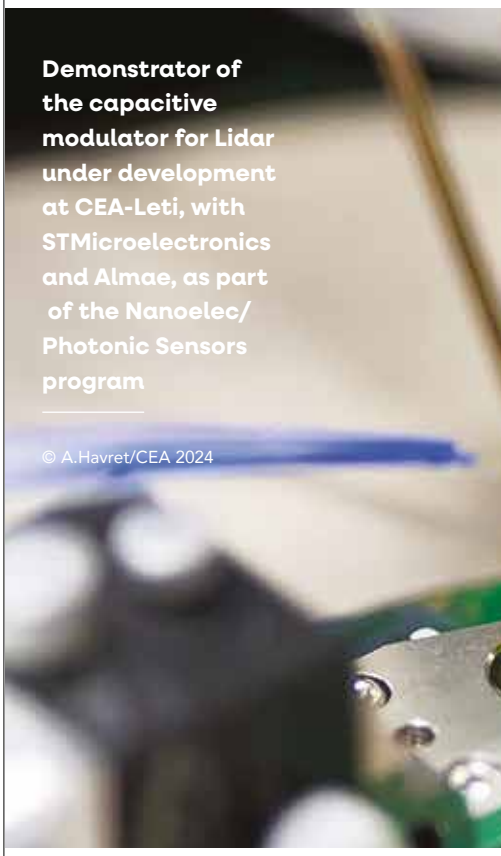
III-V semiconductors, known for their optoelectronic properties and versatile engineering capabilities, play a crucial role in the fabrication of microLEDs. Recent advances in research underscore the fact that the optoelectronic performance of microLEDs can be significantly enhanced using various strategies, such as passivation and distributed Bragg reflectors (DBRs), the incorporation of metamaterials and plasmonics, and the integration of 2D materials. The study was published in Advanced Optical Materials.[4]

Photonic interconnection for AI

The LEAF Light product family.

The Scintil Photonics start-up, which uses technologies developed within Nanoelec, is focusing on a multi-wavelength a laser source dedicated to co-packaged optics.

"This circuit will in particular be used to ensure interconnections between routing (switch) and computing (GPU) components, and support the growing needs for communication between AI and Machine Learning chips," explains Matthew Crowley, CEO of Scintil Photonics, which is positioning itself on the artificial intelligence and super-computing markets.



Demonstrator of the capacitive modulator for Lidar under development at CEA-Leti, with STMicroelectronics and Almae, as part of the Nanoelec/ Photonic Sensors program

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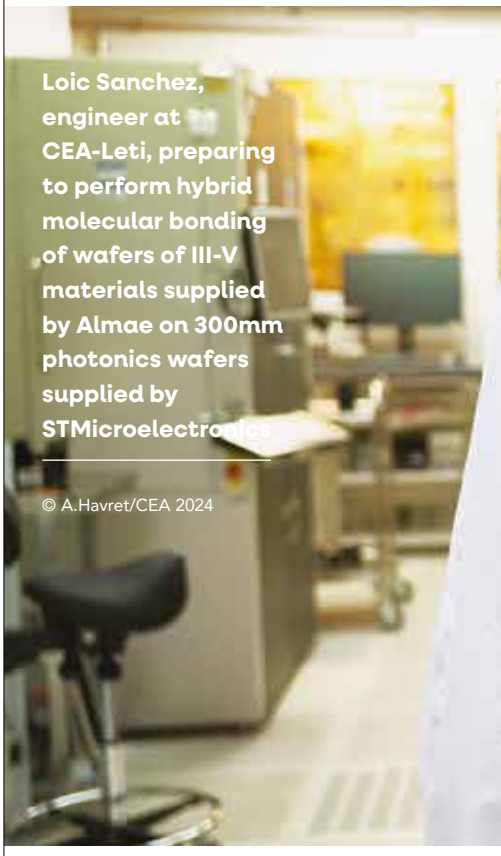
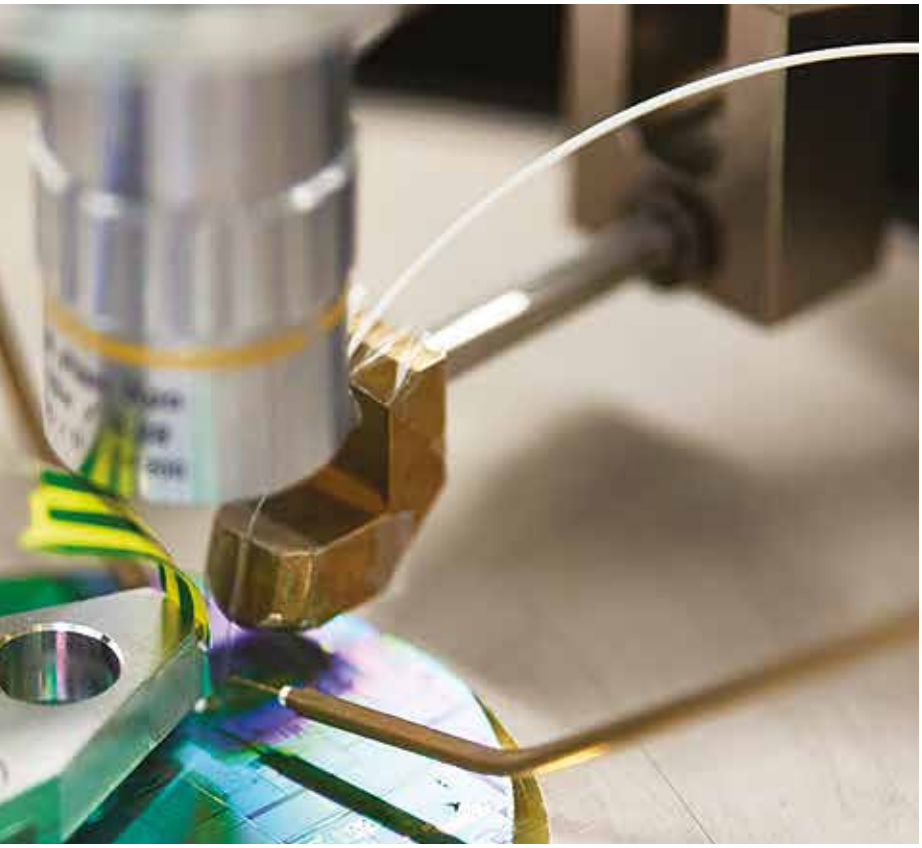


Loic Sanchez, engineer at CEA-Leti, preparing to perform hybrid molecular bonding of wafers of III-V materials supplied by Almae on 300mm photonics wafers supplied by STMicroelectronics

© A.Havret/CEA 2024

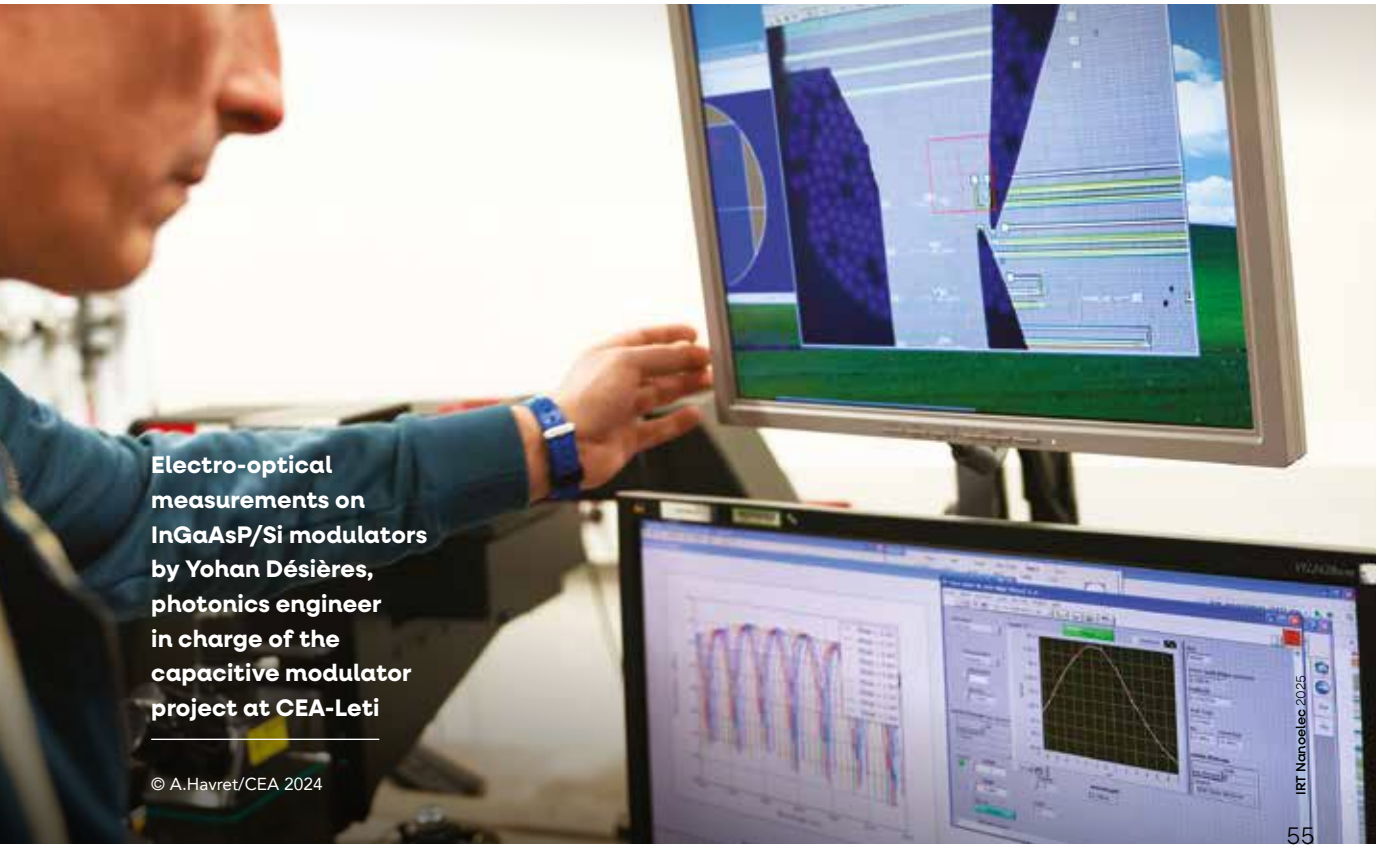
4.Mouloua, D., Martin, M., Beruete, M., Jany, C., Hassan, K., & Baron, T. (s. d.). Exploring Strategies for Performance Enhancement in Micro-LEDs : A Synoptic Review of III-V Semiconductor Technology. Advanced Optical Materials, n/a(n/a), 2402777. https://doi.org/10.1002/adom.202402777

AGENDA



Clément Castan, CMP (chemical & mechanical polishing) engineer at CEA-Leti, loads 300mm silicon wafers into the machine which is used for planarizing before molecular bonding of the IIIV materials

Tristan Faure, technician at CEA-Leti, supervises the III-V materials lithography step for the capacitive modulator demonstrator



Electro-optical measurements on InGaAsP/Si modulators by Yohan Désières, photonics engineer in charge of the capacitive modulator project at CEA-Leti

The road to the quantum computer

Providing France with the value chain needed to produce scalable electronics for fault tolerant quantum computer.

AUDREY MARTINENT, QUANTUM TECHNOLOGIES PROGRAM MANAGER AT CEA-LETI AND CO-DIRECTOR OF THE NANOELEC/Q-LOOP PROGRAM

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TANGUY SASSOLAS, QUANTUM COMPUTING PROGRAM MANAGER AT CEA-LIST AND CO-DIRECTOR OF THE NANOELEC/Q-LOOP PROGRAM

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The Q-Loop program brings together a host of academic and industrial partners to speed up the creation of a universal quantum computer. The aim is to tackle the challenge of scaling up solid-state qubit control and readout systems. The program's actors are focusing on developing software and hardware technologies for the qubit control chain, covering both control electronics and real-time quantum error correction.

The Grand Défi LSQ (LSQ great challenge) was launched by the French Government as part of its National Strategy for quantum technologies, and aims to overcome the obstacles scale up the qubit count. Scaling up entails the ability to acquire industrial processes for mass production and control of standardized, reliable quantum computing qubits.
To structure the technological value chain so that the actors needed for these industrial processes can emerge, Nanoelec is starting an unprecedented program dedicated to LSQ and directly connected to the French National Quatum Strategy. The aim is to demonstrate a control and readout chain validating the future capability to control a quantum computer with a large number of qubits.

Nanoelec's Q-Loop program focuses on developing the necessary technologies to enable qubits control and readout at scale. It brings together a wide variety of complementary actors along the value chain needed to produce and eventually maintain quantum computer control and command components. It creates strong collaboration between key industrial players in the semiconductor sector, centers of R&D excellence in quantum electronics and emerging actors in the quantum field.
The program was launched in 2024 and gathers 65 million euros of public and private funding over a six-year period. •

Q-LOOP AT A GLANCE

→ Vision
The advent of Quantum computing is deemed to impact many application domains and especially compute intensive R&D tasks, making it a key technology to master at the French & European level to ensure future digital sovereignty

→ Ambition
Structure the technological value chain of actors necessary for the emergence of scalable technologies and industrial processes needed to produce fault-tolerant quantum computers

→ Mission
Take up the technological challenges, in particular for innovative solutions in electronics, integrated photonics and 3D stacking and packaging technologies compatible with operation at cryogenic temperatures, along with hardware acceleration for real-time error correction, and coupling them with accelerated capacity for transfer from R&D to industry

→ Partners
The project involves actors along the value chain including the main French research institutions in the domain, a CAD tools vendor, and a CMOS chips manufacturer, together with national startups specialized in solid-state qubits and enabling technologies

Program kick-off

Fruitful interaction

The kick-off meeting was successfully held on November 2024, demonstrating a high level of attendance with about 50 on-site attendees and 30 remote ones.
Technical workshops were organized the same day, dealing with different topics (architecture & system modelling / test needs / cryoelectronics / 3D integration / thermal simulation) and led to fruitful interaction between the attendees from the different entities.

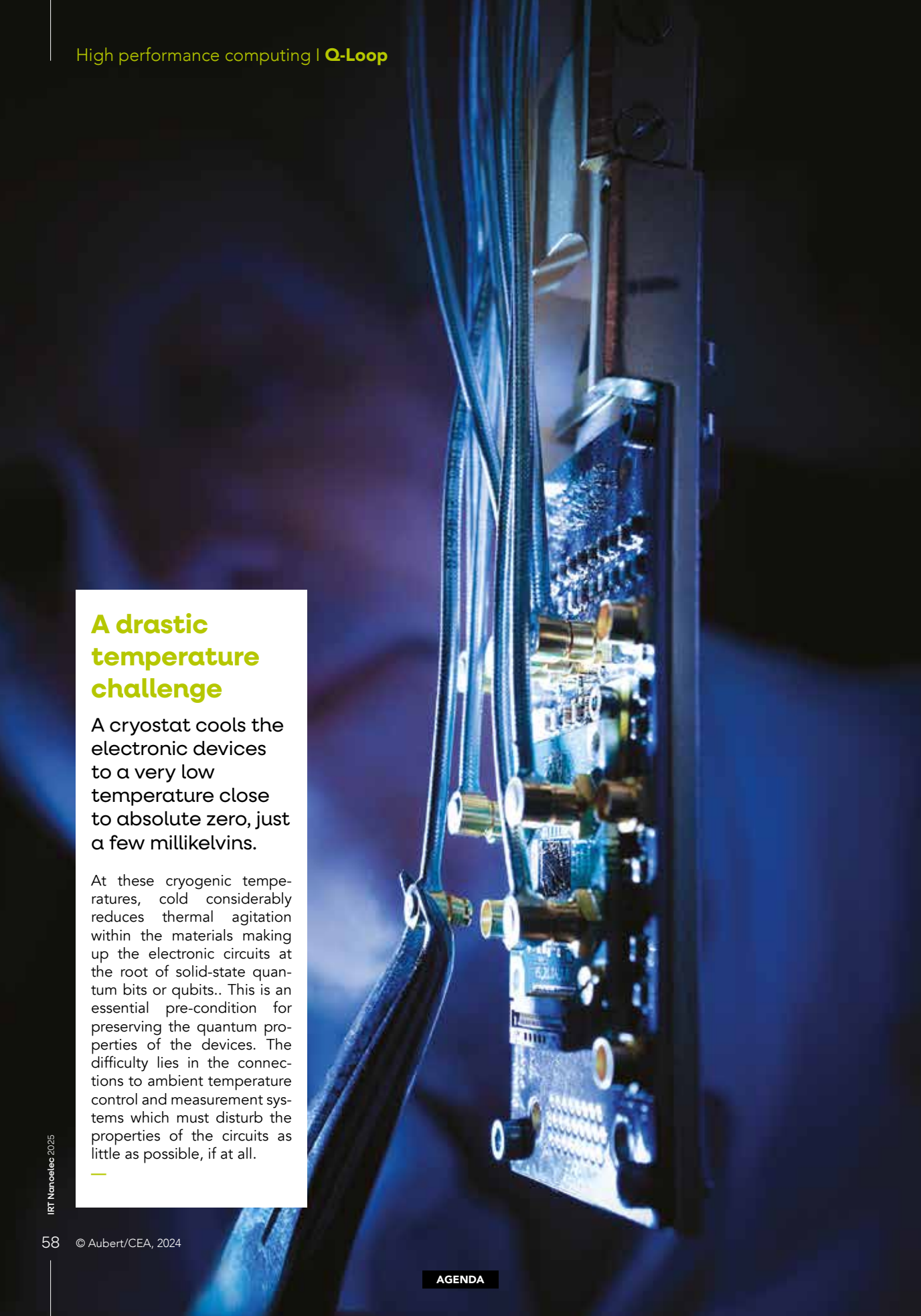
Q-LOOP KICKOFF
© Metras /CEA

First test vehicles for cryo TSV

24 wafers, with different TSV Aspect Ratios.

Critical to enable greater integration while providing best-in-class signal conservation property, the definition of fabrication process for 2D and 3D interconnections using superconducting materials was addressed early in the project definition.

Following high expectations and expression of needs by startups, the first test vehicles process embedding TSV modules and related daisy chains was launched, in order to address the conformality study of several superconducting metal deposits. The experimental plan involves 24 wafers, with several TSV Aspect Ratios as well as various vacuum deposition techniques and metals.



A drastic temperature challenge

A cryostat cools the electronic devices to a very low temperature close to absolute zero, just a few millikelvins.

At these cryogenic temperatures, cold considerably reduces thermal agitation within the materials making up the electronic circuits at the root of solid-state quantum bits or qubits.. This is an essential pre-condition for preserving the quantum properties of the devices. The difficulty lies in the connections to ambient temperature control and measurement systems which must disturb the properties of the circuits as little as possible, if at all.

From qubit to supercomputing

A large number of entangled qubits.

By performing operations on qubits whose two quantum states are superposed and entangled with one another, the quantum computer should be able to represent a large number of possible states with a small number of qubits. A system such as this will be able to process several values simultaneously and thus significantly speed up certain processing operations by comparison with a conventional computer.
It could thus be used to solve complex problems which are hard or even impossible to solve with conventional computers, in a large number of application fields, notably solving combinatory optimization problems and/or those which require immense computing capacity: for example, in the fields of logistics or finance, to develop weather forecasting models and climatic services, AI applications, design new materials, or model chemical reactions at the molecular level to develop new medicines.

To achieve computing capacity such as this, we would need quantum computers with a large number of entangled qubits, with a low level of computing error in each basic operation.

CRYOGENIC TEMPERATURE TEST BENCH FOR 300 MM INDUSTRIAL STANDARD WAFERS CARRYING CMOS TECHNOLOGY QUBITS, AT CEA-LETI

© Aubert/CEA

Cryo-CMOS

STMicroelectronics, Siemens EDA, CEA, Grenoble INP-UGA and CNRS joined forces.

STMicroelectronics, CEA, Grenoble INP-UGA and CNRS joined forces to thoroughly fine-tune the definition of the characterization and modelling plan necessary to reach a well-qualified Cryo-PDK within the first three years of the program. A BEOL (back-end-of-line) measurements plan was defined between partners for the development of interconnects. In addition, a preliminary FEOL (front-end-of-line) measurement plan (at room and cryo temperatures) was consolidated.

Preparing spin-qubit samples for cryogenic measurement at CEA-Irig

XAVIER JEHL & SÉBASTIEN GRANEL (RIGHT) IN THEIR LAB IN GRENOBLE

Sound strategy to handle cryogenic thermal simulation

On EDA tools for quantum systems.

The gap analysis on existing EDA tools for quantum systems design started with a first identified aspect regarding thermal simulation in cryogenic conditions. Successive workshops between thermal simulation experts on the thermal range of standard electronic devices (Siemens), thermal simulation experts on cryogenic conditions (CEA), and physics experts on thermal phenomenon experiments at these temperatures (CNRS) have reached a strategy to support the thermal simulation of complex IC in these regimes where heat transfer depends on the wave behaviour of phonons and in particular to their bounces at material interface depending on their scale.

The feasibility of leveraging Non-equilibrium Green's function models (slow but more accurate) qualified by experiments, to tune existing EDA tools (fast but inaccurate in these regimes) was assessed. Future works will require significant efforts relying on experimental teams, low-level simulation for small systems and intermediate validation and EDA tools for the thermal evaluation of larger scale systems.

QEC code

Hardware acceleration using FPGAs.

Qubits, whatever their modality, are highly sensitive to noise and environmental disturbances that can alter their state. Given that QEC is an essential element in the construction of practical and reliable quantum computers, CEA & Inria experts carried out a very first review of the state of the art in quantum error correction (QEC) codes and associated decoders, underlining the specificities of four classes of decoding approaches for the well-studied surface codes. Future works will target hardware acceleration using FPGAs of most promising approach to scaling.

NANOELEC. Q-Loop

Visibility of the program

A communication kit was produced, including a .pptx presentation template adapted from Nanoelec's theme; a logo for the program, consistent with the Nanoelec typography was defined, as well as web pages for the Nanoelec website in both French and English. It should be noted that during the summer of 2024, prior to the official launch, a communication kit for the official national strategy website was also produced.

Cyber-security is a major challenge for digital trust

The rise of the Internet of Things (IoT) has sparked an explosion of innovative services, powered by a variety of heterogeneous connected devices and sophisticated data management.

CHRISTOPHE VILLEMAZET, DIRECTOR OF THE NANOELEC/PULSE PROGRAM

Yet, this digital revolution comes with a dark side: a surge in cyberattacks that is forcing public and institutional bodies to confront the risks of unchecked digital transformation.

New hardware and software vulnerabilities are being exposed at an alarming rate, as medical devices, vehicles, industrial, and urban infrastructure become increasingly interconnected and autonomous. These vulnerabilities, and the exploits that target them, are eroding public trust in connected services and products. The repercussions are vast, affecting corporate reputations, societal stability, economic growth, and individual privacy. Inadequate protection can even jeopardize the legal and social accountability of both public and private entities.

Moreover, cybersecurity is often relegated to an afterthought in digital product design, seen as a constraint that should not impede primary functions, whether health, mobility, or manufacturing, nor compromise cost, performance or ergonomics.

The Nanoelec/Pulse program rises to this challenge, seeking to harness electronic technologies to address this new reality. Our mission is to pioneer technologies that enable the development of connected products and services, fortified with enhanced security, robust data protection, and simplified cybersecurity strategies. We are committed to safeguarding the confidentiality, authenticity, and integrity of digital data, and ensuring privacy protection. Our focus lies in three critical domains: fortifying the cybersecurity of industrial systems, safeguarding healthcare products, and securing autonomous robotic systems and vehicles. •••

AGENDA

PULSE AT A GLANCE

→ Vision
Due to the rise in cybercrime, Internet of Things (IoT) cybersecurity is a major challenge for digital trust. Strengthening and hardening critical embedded, increasingly interconnected and smarter systems is now vital

→ Ambition
New smart and intrinsically secure nanocomponents to reinforce the resistance of systems to future cyberattacks + improved security of smart embedded systems throughout their lifecycle (including AI algorithms) + safer deployment environments through digital ID, data sovereignty and secure interactions between smart systems

→ Mission
To develop and test new security features for components and systems in three fields of application: Industry 4.0, homecare and robotics

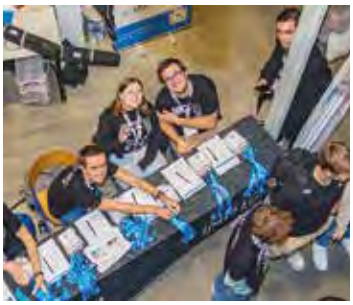
→ Partners
CEA, Grenoble INP-UGA, Inria, Schneider Electric, STMicroelectronics, UGA

In 2024, the teams involved in the Nanoelec/Pulse program achieved significant milestones in both post-quantum cryptography and the securing of embedded AI. We now possess a secure, open-source microprocessor core platform (RISC-V). Our teams are developing advanced modeling and evaluation capabilities for digital components in building management, crane control systems, and the secure implementation of blockchain on embedded systems.

This progress underscores our commitment to pushing the boundaries of cybersecurity and ensuring that our technological advances are both innovative and secure. As we continue to explore these frontiers, we remain dedicated to creating solutions that protect data integrity, enhance system reliability, and fortify the digital infrastructure of the future. •

Pulse at international events

The Nanoelec/Pulse program teams took part in the 2024 editions of the InCyber Forum (Lille, Oct. 31 – Nov. 4, 2024), European Cyber Week (Rennes, Nov. 18-21, 2024), RISC-V Summit Europe (Munich, June 24-28) and CSAW (Valence, Nov. 7 and 8) to present their work, notably concerning intrinsically secure application processors.



IRT Nanoelec 2025

Thomas Loubier, embedded systems cybersecurity research engineer in the Systems Department of CEA-Leti, testing the security of communication protocols at the physical and wireless interfaces, on CEA-Leti's SCIBE (Secure Communication Interface BEnch), developed with IRT Nanoelec.

PhDs AT PULSE

Numerous students connected to the Nanoelec/Pulse program defended their theses in 2024.

Confidentiality of embedded machine learning models

The deployment of Deep Learning (DL) models on embedded platforms is becoming increasingly widespread.

These models are required to perform tasks and handle sometimes sensitive data, so they must be secure, notably for European regulatory projects. Raphaël Joud studied threats to the confidentiality of DL models through hardware attacks, more particularly side channel attacks. Based on these results, Raphaël then assessed various countermeasures aimed at reinforcing the confidentiality of embedded models[1].

Collision avoidance in robotics

Mobile robots and autonomous vehicles must navigate in complex, unstructured environments, such as urban spaces shared with humans.

Although simple and effective, object representations often fail to model these uncertain scenes. The approach adopted by Thomas Genevois[2] aims to facilitate the integration of dynamic occupancy grids for collision avoidance, thus improving the connectivity between perception and navigation. The solutions were tested on three different robots, including a robotic car, in real conditions.

Security of post-quantum cryptographic implementations

Side channel attacks are a threat to the security of post-quantum cryptography.

After identifying the vulnerabilities in these implementations, three attacks on the HQC scheme were analyzed. The countermeasures identified by Guillaume Goy[3] include masking and mixing of the data handled in order to protect sensitive operations. His work demonstrates the ineffectiveness of existing countermeasures and underlines the need to reinforce the security of post-quantum implementations.

Cameras to study the effects of overweight and obesity

Overweight and obesity are a major public health issue. Balance and walking problems are frequently observed in overweight or obese people, which can sometimes lead to falls. To measure the effects of overweight and obesity when dealing with an obstacle while walking, Matthias Chardon[4] analyzed a set of experimental data. This data included five space-time parameters for walking and three obstacle clearance parameters measured on each foot by means of a system of ten infrared cameras filming the gait and obstacle clearance of 43 young adults. Even if the initial results suggest that overweight has minimal impact on tripping when clearing an obstacle while walking, additional work should evaluate overweight individuals of different ages and with different health conditions.

1. St Etienne University thesis, defended on January 18, 2024, prepared with the Centre Microélectronique de Provence - Site Georges Charpak (CMP-GC)

2. Grenoble Alpes University thesis, defended on June 19, 2024, prepared with Inria

3. Limoges University thesis, defended on June 24, 2024, prepared with the XLIM laboratory (UMR CNRS 7252)

4. Grenoble-Alpes University thesis, defended on September 20, 2024, prepared with the Ageis laboratory

AGENDA

Insight into age-related changes in gait

Since walking has a crucial role in maintaining independence, changes in gait should be identified and prevented at an early stage.

Walking speed predicts many clinical outcomes in old age. However, a comprehensive assessment of how walking speed affects accelerometer-based quantitative and qualitative gait measurements in younger and older adults is lacking.
The objective of this thesis was to gain insight into the possible mechanisms underlying age-related changes in gait.
A better understanding of age-related changes in gait patterns is provided through digital monitoring of gait (walking speed, walking conditions) with accelerometers. Gait speed is considered as the most commonly and widely used measurement to assess the locomotor performance of older adults. Iris Hagoort[6] has contributed to clarify the different functional properties contributing to age-related changes.
One of the conclusions is that the relationship between walking speed and quantitative and qualitative gait measurements, as well as the effects of age on this relationship, depends on the type of gait measurement studied.

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Safety-security convergence of industrial control systems

Nowadays, industrial control systems (ICS) incorporate information technologies and are interconnected with the outside world, such as the internet, thus exposing their infrastructures to cyberattacks.

Cyberattacks have become new threats for industrial system operators, more particularly for continuity of service, reliability and security. Mike Da Silva[5] presents a complete assessment of the cybersecurity threat to the security of industrial control systems. His method differs from the state of the art in its high level of automation and its ability to model complex ICSs.

—

Acceptance of digital technologies in rheumatology

Telemedicine can be used for remote consultation, diagnosis, treatment and monitoring of patients, thereby facilitating their access to healthcare.

By studying 12 automatic learning algorithms for predicting the willingness to use tele-medicine by patients suffering from rheumatic and musculo-skeletal disorders, Felix Mühlensiepen studied the social, economic and psychological determining factors influencing the acceptance and use of digital health technologies in rheumatology, both by the patients and by the health professionals. If the use of these technologies is generally well accepted by the patients and health professionals, there are nonetheless access barriers which could lead to a digital divide.

—

Simulating cyberattacks on industrial control systems

Reinforcing the cybersecurity culture in industry.

After a systematic review of all the anomaly detection methods based on the system calls described in the literature, the teams from CEA and Schneider Electric, within Nanoelec, set up a testing and attack platform representative of an industrial system. Its aim is to test security solutions and notably to generate datasets to train AI models to automatically detect intrusion. The test bench proposes the greatest diversity and attack coverage in the MITRE ATT&CK matrix on Programmable Logic Controller and industrial gateway type devices, by comparison with the other state-of-the-art test benches.
Restoration mechanisms were also implemented for each of the attacks in order to return the system to a normal operating state. The aim is to be able to execute all attacks and extract internal signals from the device without having to reprogram or restart the target after each attack. All these developments are scheduled to be released as open source in 2025.
The WonderPOT honeypot was expanded to make for easier deployment. The aim is to provide a solution capable of capturing IoT-oriented malware while remaining stealthy so as not to be detected as a decoy system.

—

5. Grenoble-Alpes University thesis, defended on October 15, 2024, prepared with the LIG laboratory

6. Grenoble-Alpes University and RIJKSUNIVERSITEIT GRONINGE thesis, defended on November 1, 2024, with the Ageis laboratory

7. Grenoble-Alpes University thesis, defended on November 7, 2024, with the Ageis laboratory

Safe and autonomous smart hoisting system

A more autonomous overhead crane thanks to artificial intelligence.

Within the framework of Nanoelec, the teams from Schneider Electric and INRIA are developing a learning pipeline for artificial intelligence dedicated to the automatic control of load sway during autonomous movements of an overhead crane.

"The aim is to increase the autonomy of the overhead crane without compromising safety while reducing equipment maintenance and parameter setting times," says Charles Blondel, Head of R&D Dept. of the Industrial Automation Business Unit at Schneider Electric. *"Automation of hoisting systems requires the use of advanced sensors, such as scanners and cameras, as well as algorithms to interpret a whole range of data to generate reliable and safe decisions."*

Robotics is becoming increasingly present in plants, notably to improve productivity and safety when moving heavy loads. *"Autonomous Intelligent Vehicles (AIVs) or Autonomous Mobile Robots (AMRs) are now integrated into production lines, including with remote sensors around the infrastructure,"* explains Charles Blondel. It is possible to integrate this new Integrated Autonomous Crane System (IACS) without endangering the production line, surrounded by human employees. Following mathematical modelling of an overhead crane, the teams at Nanoelec defined an approach to the problem of crane control aiming to optimize the parameter settings of the existing controllers. An AI learning pipeline incorporating a simulator developed by Schneider Electric was then set up.

"We have generated datasets for simulations by varying the system parameters (acceleration, deceleration, maximum linear speed, overall time delay) across the range of control algorithm coefficients. A total of 32 distinct crane models were simulated," says Charles Blondel. *"The new approach, validated using a simplified model (3 degrees of freedom), enables automated deployment during the commissioning phase, ensures more consistent performance without human intervention, and delivers a 10% to 20% production increase on the SE bridge."*

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SCHNEIDER ELECTRIC TEST BENCH FOR THE DEVELOPMENT OF A SAFE AND AUTONOMOUS SMART HOISTING SYSTEM

© Schneider Electric

8. With the collaboration of Grenoble INP - UGA and INRIA

NUMEROUS EXPERIMENTS ARE BEING CARRIED OUT IN EUROPE AND AROUND THE WORLD, MOSTLY AROUND LOCALIZED AND LIMITED AUTONOMOUS SHUTTLES

Validated perception solutions for autonomous vehicles

Multimodal perception systems for mobile robotics.

Within Nanoelec, Inria has been developing probabilistic perception and navigation systems for autonomous vehicles for years, enabling safe and explainable fusion and filtering of information and decision-making. The developed systems are particularly effective at dealing with multimodal data sources, coming from different types of embedded or deported sensors, making them particularely well-suited to complex dynamic environments. This core technological framework, in constant evolution, supports various transfer and associated research projects, empowering diferent indoor and outdoor autonomous mobile robots. Mainly focused this year on engineering issues, the work on the significant software and technology base has enabled much greater modularity and robustness, integrating into our solutions the latest developments in the mobile robotics community (ROS2, NAV2).

As explained by Lukas Rummelhard, research engineer at Inria working in the scope of Nanoelec, if the current improvement rate of data-driven AI systems might pave the way for large-scale deployment of autonomous vehicles in some environments, diffusion of such breakthrough technologies in many other use-cases may be hindered by a lack of sufficient relevant data and dedicated compute power, or validation and regulatory concerns.

Core to these developments, GPU optimization of methods and software have always been a key focus of effort to enable this probabilistic framework to be embedded. Such optimizations of data transfers have been the topic of a presentation at ROSConfr, by Hugo Bantignies, "The ROS2-type adaptation, a gateway to GPU hardware acceleration"[10].

Jean-Baptiste Horel (PhD at Inria) presented a Navigation-Based Evaluation Metric for Probabilistic Occupancy Grids at ITCS 2023[10]. *"We unveiled a new navigation-based metric for occupancy grid similarity evaluation. Our method addresses the limitations of existing metrics by evaluating the differences in pathfinding behavior between the ground truth and the inference occupancy grids,"* he states.

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AGENDA

9. Hugo Bantignies at ROSConFr - Nantes, June 19, 2024 "The ROS2-type adaptation, a gateway to GPU hardware acceleration".

10. Horel, J.-B., Baruffa, R., Rummelhard, L., Renzaglia, A., & Laugier, C. (2023). A Navigation-Based Evaluation Metric for Probabilistic Occupancy Grids : Pathfinding Cost Mean Squared Error. ITCS 2023 - 26th IEEE International Conference on Intelligent Transportation Systems, 1-6. https://hal.science/hal-04211125

Digital identity management on a robotic system

Preventing identity theft.

Within Nanoelec/Pulse, the CEA teams are developing a demonstrator in response to the need to identify a person face-to-face via the anonymous trace of a record on a blockchain-type digital system. *"We are studying the question of digital identity in the industrial context and are producing the prototype of a connection interface for robotic system users,"* says Christine Hennebert, in charge of the project at CEA-Leti.

The goal is to guarantee user confidentiality on the digital system, while enabling the traceability of actions and the accountability of those involved to their employer or auditors. *"We are also developing solutions to prevent identity theft on the robotic system. The smart contracts technology is being used to implement an end-to-end confidentiality protocol between the user connection interface and the remote register, while respecting embedded system constraints."*

Blockchain hardware implementation

Following on from the "blockchain and digital identification" white paper, and in order to envisage the technology readiness level (TRL) of the demonstrators, Nanoelec is a member of the "Alliance Blockchain France" association. The Alliance Blockchain France recently joined the ACN (Alliance for digital trust) as GT4 "Blockchain".
On the technical side, a third version of the testnet was deployed with a significant increase in maturity on the production and security side. A 4th version of the testnet is currently being prepared, to replace the consensus protocol at the heart of the blockchain.

An intrinsically secure processor

A modular design based on the Risc-V open standard.

After carefully identifying the vulnerabilities of the most common processors (microcontrollers, processors for IoT, personal computers and servers) in award-winning work in 2019[11], a team from CEA-Leti is continuing its work under the Nanoelec/Pulse program on 64-bit NaxRiscV, a Risc-V open standard processor[12]. *"By separately examining each logic level of the processor, we are looking to implement the "intrinsically secure processor" concept. The approach is in response to the worrying exponential increase in cyberattacks and the impossibility of guaranteeing a fault-free software code. It is then up to the intrinsically secure processor to prevent these vulnerabilities from being exploited,"* explains Olivier Savry, a researcher at CEA-Leti[13].

"The unique feature of this highly advanced processor is its modular design: we can thus study countermeasures proportionately to different levels of attack.

OLIVIER SAVRY, CYBERSECURITY EXPERT AT CEA-LETI

© Havret/CEA

11. Olivier Savry, Thomas Hiscock, Mustapha El Majihi "Sécurité matérielle des systèmes", Dunod, 2019

12. CIAMH : Confidentiality, Integrity and Authentication across the Memory Hierarchy, AIT LAHSSAINE Karim, SAVRY Olivier, RISC-V Summit Europe 2025

13. Comprehensive Lockstep Verification for NaxRiscv SoC integrating RISCV DV, RVLS, and Questa/UVM, IGHILAHRIZ Billal, SAVRY Olivier, RISC-V Summit Europe 2025

Secure implementation of post-quantum cryptography

The NIST reaches a new milestone in post-quantum cryptography by selecting the HQC scheme to which IRT Nanoelec made significant contributions.

The international process to select the best post-quantum cryptography algorithms set up by the National Institute of Standards and Technology (NIST) has reached an important milestone with the selection of the HQC scheme with a view to standardization. This decision completes the first selection phase initiated in 2016 to define a new asymmetrical encryption standard able to withstand future quantum attacks.

Since 2020, the teams at IRT Nanoelec have been involved in studying HQC, addressing all the challenges represented by a new standard. Most of the work done consisted in a security analysis of HQC in the face of physical attacks. Most of the physical attacks published on HQC come from the work done by Nanoelec, underlining the expertise of its teams.

"We proposed a software implementation of HQC with the smallest memory footprint capable of embedding HQC on components with resource constraints," explains Antoine Loiseau, who is conducting research at CEA-Leti, within the framework of Nanoelec/Pulse. *"We also proposed a more advanced hardware architecture in terms of agility, making it possible to accelerate the main PQC schemes recently standardized."*

Post-quantum cryptography (PQC) will become the standard in the coming years and will replace the existing cryptography. The NIST in the United States, the ANSSI in France and the BSI in Germany have begun the technological and industrial cryptography transition.

The results of this research are published in open source so that the entire community can benefit from implementation of the performance on an embedded system.

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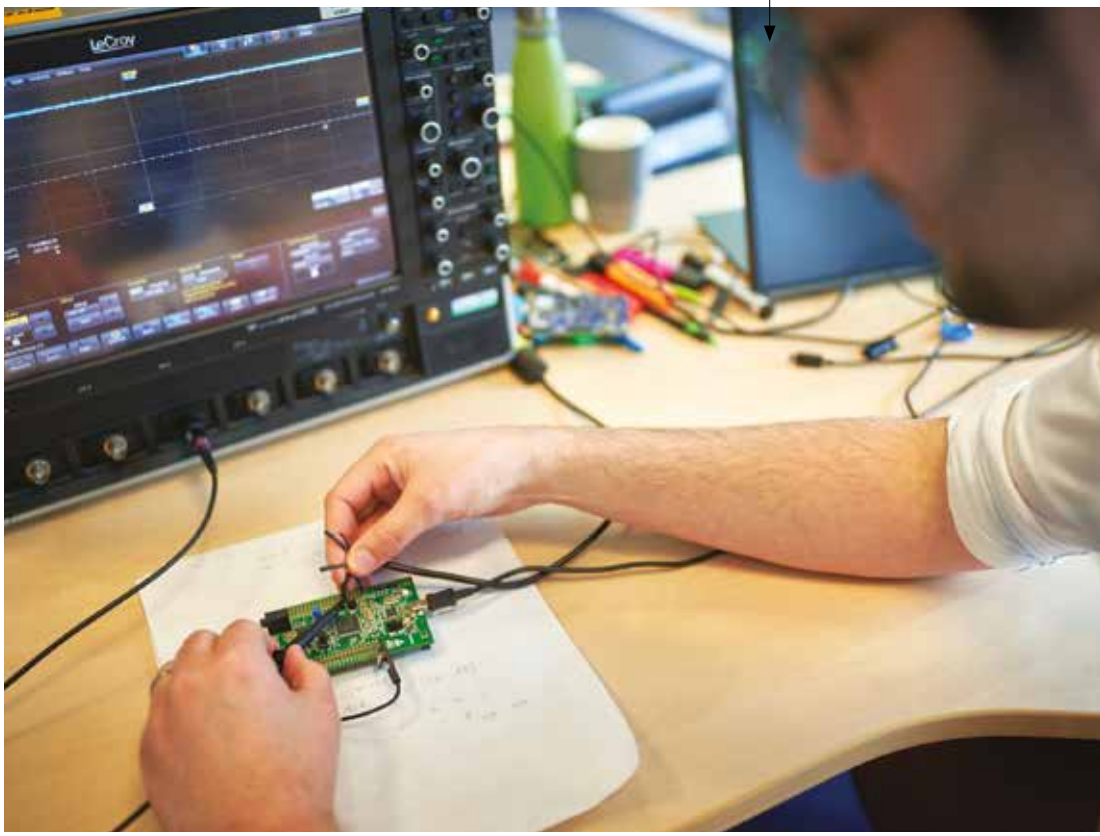
WITHIN NANOELEC, RESEARCHERS FROM CEA HAVE PUBLISHED A FIRST LEVEL OF OPTIMIZATION FOR THE IMPLEMENTATION OF A COMMUNITY-ACCLAIMED STANDARDIZED POST-QUANTUM ALGORITHM (NIST COMPETITION), IN OPEN SOURCE



Large scale instruments for characterization

Nanoelec's Characterization program is part of the institute's digital trust offering in support of the digital transition. Ennio Capria, Programme Director, sheds light on the achievements of 2022.

ENNIO CAPRIA, DEPUTY HEAD OF BUSINESS DEVELOPMENT AT ESRF AND DIRECTOR OF THE NANOELEC CHARACTERIZATION PROGRAM

© P. Jayet/CEA

Through the Nanoelec Characterization program, industrial firms and researchers have access to world-class tools to study the effects of ionizing radiation on electronic devices and systems, to characterize the properties of their materials and to inspect their components, contributing to the quality of their products and processes. Thanks to the high penetrating power of neutrons and synchrotron X-rays, these evaluations can be performed non-destructively, without the need to open or damage the objects, and in many cases while they are operating.

In 2024, the Characterization program continued to play a central role, offering innovative solutions and strengthening its collaborations with key partners, including STMicroelectronics, Soitec, Schneider Electric and Iroc Technologies. The year was marked by increased demand for non-destructive imaging (NDI) techniques at ESRF, driven by the spectacular advances made possible by the new EBS synchrotron source. •

AGENDA

Correlative Material characterization

The ESRF BM05 beamline, X-ray Beam Induced Current analysis brings correlations between charge collection efficiency and defects in the materials.

A new instrument capable of performing correlative analyses between XBIC (X-ray Beam Induced Current) and X-ray Diffraction Imaging is now available at the ESRF BM05 beamline. *"We successfully developed and implemented a new XBIC setup that allows characterization of semiconductors. This technique was shown to complement existing techniques (such as RCI, spectroscopy, XRF microscopy, etc.). The characterization of different diamond samples enabled us to identify the correlations between charge collection efficiency and defects like dislocations, growth boundaries and growth sectors, impurities, and color centers,"* explains Thu-Nhi Tran-Caliste, industrial liaison engineer at the ESRF, who is taking part in the study for the Nanoelec Characterization program.
Further investigations were conducted in 2024 with other semiconductors (GaN, SiC or CdTe) to fully evaluate the potential of this technique coupled with Bragg diffraction imaging.

Pierre Everaere, an engineer at ESRF, presented the first results obtained within Nanoelec on the international stage at NDNC 2024 Conference[1] and the French Japanese Workshop on Diamond Electronic Devices 2024[2].

1. Everaere, P. (May 30, 2024). Coupling X-ray Beam Induced Current, ToF-XBIC and X-ray Diffraction Imaging to characterize diamond plates used as semiconductor-based detectors. Workshop NDNC 2024, Sydney (Australia)

2. EEveraere, P., Caliste, T. N. T., Baruchel, J., Benichou, S., & Dowek, R. (June 14, 2024). Coupling X-ray Beam Induced Current, ToF-XBIC and X-ray Diffraction Imaging for semiconductor characterization. French Japanese Workshop on Diamond Electronic Devices 2024, Cap Estérel

PROGRAM AT A GLANCE

→ Vision
The unmatched performance of large-scale instruments must be adopted by industrial users as a cutting-edge tool to perform advanced characterizations of electronic components and devices

→ Ambition
Develop a competence center for testing radiation hardness of electronic components

→ Mission
Continue to make unique scientific instruments & methodologies available to meet the new challenges of the electronics industry, for the serenity and sovereignty of the digital transition

→ Partners
CEA, CNRS/LPSC, ESRF, ILL, Schneider Electric, Soitec, STMicroelectronics, Iroc Technologies

SIMON BENICHOU AND THU NHI TRAN-CALISTE ARE OPERATING NANOELEC GIANT GONIOMETER FOR X-RAY REFLECTOMETRY AND DIFFRACTOMETRY AT ESRF BM05 BEAMLINE

Soft errors caused by neutron irradiation

Correlation between the sensor sampling frequency and the rate of SEU-induced mismatch failures in the case-study system.

A team from Telecom Paris, Tima laboratory (CNRS, Grenoble INP-UGA, UGA), and Institut Laue-Langevin revealed the impact of increasing the sensor sampling frequency on the reliability of a typical edge processing system operating under the effects of 14-MeV neutrons and thermal neutrons[3].
The results of two types of accelerated radiation tests indicate that the failure rates induced by soft errors caused by 14-MeV and thermal neutrons grow as a function of the sensor sampling frequency. The failure rates caused by 14-MeV neutrons rose by a factor of 2.2 by shifting the sensor sampling frequency from around 140 to 430 Hz. The results also suggest that the design and calibration of edge processing systems should consider the sensor sampling frequency as a parameter for adjusting the computing speed of the system in order to improve reliability in tolerating soft errors caused by neutrons..

RICHARD DAVIES, INDUSTRIAL APPLICATIONS SCIENTIST AT ILL & NANOELEC/ CAR PROGRAM AND EMMANUEL ATUKPOR, ILL RESEARCH ENGINEER RESPONSIBLE FOR NANOELEC/TENIS

3. de Carvalho, M. M., Laurini, L. H., Atukpor, E., Naviner, L., & Bastos, R. P. (2024). Impact of Scaling Up the Sensor Sampling Frequency on the Reliability of Edge Processing Systems in Tolerating Soft Errors Caused by Neutrons. IEEE Sensors Letters, 8(9), 1-4. IEEE Sensors Letters. https://doi.org/10.1109/LSENS.2024.3435677

Neutron reflectometry for improved photolithography

Coatings on epoxy resin were investigated.

To protect polymer resins used in the semiconductor industry for patterning through photolithography, a hard coating can be applied to the polymer to prevent surface degradation.

Different coatings on epoxy polymer resin under ambient conditions have been investigated with in-situ neutron reflectometry in a vacuum and a D2O-saturated atmosphere. Results were published by authors from Institut Laue-Langevin and STMicroelectronics and Uppsala University (Sweden) collaborating within Nanoelec[4].

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Emulating heavy ions irradiation on components through pulsed X-rays

Alternative to heavy ions testing of components.

Tynchrotron X-rays may be used to emulate the interaction between heavy ions and electronic devices for next generation space applications. The capability of synchrotron pulsed X-rays to deposit critical charges on electronic components has been demonstrated at the ESRF, in the frame of the PAC-G[5] driven, innovation led long term project for microelectronics industry. It can be used for fault injection, pre-screening and sensitivity characterization. As presented at GB-RADNext 2024[6] and IEEE Space Environment Workshop, also the possibility to characterize encapsulated components has been demonstrated, though the experiment should be carefully designed.

Reviewing potentially suitable facilities for pulse X-Ray irradiation, Françoise Bezerra (Cnes) presented at the Thematic Day of the RADECS2024 conference a selection of results collected at the ESRF ID09 beamline in the frame of the Nanoelec/PAC-G platform. *"More and more components are difficult or impossible to test under heavy ions, she said. Either because of limitation in the sample preparation/decapsulation (cost, delay, yields), or because the energy is not high enough to properly represent realistic conditions in space or because of strict conditions needed in the sample packaging, probing and conditioning close to the ion source."*

Results for several kind of components like Silicon based COTS (commercial Off the shelf), various diodes (Si, SiC or GaN) and finally power devices were presented at the RADECS2024 Thematic Workshop[7].

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4. Chevreux, F., Letiche, M., Vorobiev, A., Wolff, M., & Chapelon, L.-L. (2024). Moisture Diffusion in PECVD a-SiOxNy:H and a-SiOx:H Coated on Polymer Resins : A Neutron Reflectometry Study. ACS Applied Electronic Materials, 6(7), 4864-4868. https://doi.org/10.1021/acsaelm.4c00239

5. Nanoelec/PAC-G provides a range of services, from consultancy work to executing sample characterization experiments and analysing data. This includes access to large-scale facilities, such as synchrotron and neutron sources, and offers a cost-effective and rapid service tailored to the micro- and nanoelectronics industry. Through PAC-G, industry can gain access to cutting-edge characterization tools, without going through selection processes, and to some of the world's most knowledgeable experts in the field of material characterization

6. Capria, E. (June 13, 2024). The use of synchrotron X-rays to emulate the interaction between heavy ions and electronic devices for next generation space application. GB-RADNEXT 2024, Didcot (United Kingdom). https://indico.cern.ch/event/1353707/

7. Bezerra, F., Dubos, S., Coic, L., Guillermin, J., Levantino, M., & Capria, E. (2024, September). Perspectives and Current Status on SEE Testing with Pulsed X-rays. Mas palomas, RADECS2024 Thematic Workshop

NANO FOCUSING ON ID01 BEALINE AT THE ESRF DEDICATED TO MICRODIFFRACTION IMAGING
© A.Havret/CEA 2024

Testing hard coating for resins in photolithography

Since the 1970s, polymer resins have been widely utilized in the semiconductor industry for patterning through photolithography. In state-of-the-art image sensors, permanent resins are used in arrays of microlenses to optimize the path of light and increase its yield.

The variety of resin compositions, their tunable refractive indices, and their shapes allow them to meet the high standards required in microelectronics manufacturing. Moreover, the polymer layer is moisture-resistant and prevents water from penetrating into the sensor. Unfortunately, polymers have soft surfaces and are easily damaged by mechanical stress. A hard coating can be applied to the polymer to prevent surface degradation. In a paper published in ACS Applied Electronic Materials[8], a team from STMicroelectronics, Laue Langevin Institute and Uppsala University, supported by Nanoelec, used X-ray photoelectron spectroscopy (XPS) and ToF-SIMS to study the uptake of water by thin films of SiOxNy and SiOx hard coatings as-deposited on epoxy polymer resin by PECVD.

8. Chevreux, F., Letiche, M., Vorobiev, A., Wolff, M., & Chapelon, L.-L. (2024). Moisture Diffusion in PECVD a-SiOxNy:H and a-SiOx:H Coated on Polymer Resins : A Neutron Reflectometry Study. ACS Applied Electronic Materials, 6(7), 4864-4868. https://doi.org/10.1021/acsaelm.4c00239

Optical transceivers under heavy ions

SEE sensitivity and testing constraints

Latest generation high data-rate optical transceivers are considered innovative and strategic products for future space missions.

A team from TRAD Tests & Radiation and Cnes, partially supported by the Nanoelec/Carac program, investigated heavy ion SEE sensitivity and testing constraints using various test facilities for such products, including synchrotron focused pulsed X-rays. This work, presented at RADECS 2024[9], reinforces the interest in these products and shows that even high-frequency optical transceivers can be tested, with minimal preparation. In the end, the data shows that the products tested as part of this study can be of interest for telecoms missions.

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9. Aubry, Laborde, Coic, L., Garcia, P., Dubos, S., Guillermin, J., Dufour, & Mekki. (September 16, 2024). Study of the heavy-ions sensitivity of latest generation high data-rate optical transceivers. Actes RADECS 2024, Mas Palomas (Spain)

Single-Event Upsets Induced by Thermal Neutrons in SRAMs

No need for a very large amount of nitride to cause a substantial number of upsets in SRAMs.

Investigations of single-event upsets (SEU)[10] induced by thermal neutrons continued in 2023 at the Thermal and Epithermal Neutron Irradiation Station (TENIS ILL/Nanoelec beamline)[11]. Thermal neutrons are an important contributor to any radiation environment where spallation reactions and neutron moderation are involved. This is the case in the atmosphere (ground level to flight altitudes) as well as in high-energy physics accelerators. Thermal neutrons can trigger single-event upsets (SEUs) in memory-based devices through indirect ionization following their nuclear absorption in 10B atoms that may be present within or near sensitive cells.

Combining experiments at Tenis, as part of the Nanoelec/Carac program, with simulations, a pan-European collaboration was published in the IEEE Transactions on Nuclear Science Review[12]. *"We introduce the possibility that thermal neutron SEUs may not only be caused by the interaction with 10B in the proximity of the SV, but also by the interaction with 14N that may result in the release of low-energy protons (LEPs)[13],"* explains Andrea Coronetti (Cern) as first author of the paper.

Typically, nitrogen is used in thin barrier layers made of TaN or TiN or even as an insulator in the form of Si3N4. The presence of nitrogen in these thin barrier layers can be enough to justify the experimentally observed thermal neutron SEU cross-section for a static random-access memory (SRAM). Nevertheless, the expected SEU cross-section from thermal neutrons is usually a few orders of magnitude lower than that of high-energy particles, and does not therefore represent a major threat in atmospheric applications. At the same time, for high-energy accelerators, the contribution to the total soft error rate could become substantial, although easy to handle by means of margins.

"The devices that may be affected are therefore only those showing a marked sensitivity to LEPs. At the same time, there is no need for a very large amount of nitrides (TaN, TiN, or Si3N4) to cause a substantial number of upsets in these kinds of devices," warns Andrea Coronetti.

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10. The terms single-event upset (SEU), single-event effect (SEE) or single-event latch-up (SEL) refer to the highly localized deposition of energy by single particles or their reaction products causing adverse effects in a sensitive node of a microelectronic device

11. In 2023, ten external experiments took place on the TENIS instrument (Thermal and Epi-Thermal Neutron Irradiation Station), although the ILL reactor did not deliver any neutrons from October 2021 to March 2023, due to a major maintenance and upgrade program

12. Coronetti, A., Alía, R. G., Lucsanyi, D., Letiche, M., Kastriotou, M., Cazzaniga, C., Frost, C. D., & Saigné, F. (2023). An Analysis of the Significance of the 14N(n, p) 14C Reaction for Single-Event Upsets Induced by Thermal Neutrons in SRAMs. IEEE Transactions on Nuclear Science, 70(8), 1634-1642. https://doi.org/10.1109/TNS.2023.3239407

13. When a capture of thermal neutrons releases low-energy protons into the material

French reliability center

Nanoelec joins the national community of reliability experts.

Since the end of 2023, Nanoelec has been a member of the French Reliability Center (CFF), a grouping of reliability experts for electronic systems and components. The CFF is a national body and includes academic and industrial entities, laboratories and research units, large groups and SMEs/mid-caps.

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A VIEW OF THE DEUTERIUM IONS SOURCE ON THE GENESIS ACCELERATOR[14]. A NEUTRON BEAM (14 MEV) IS GENERATED BY THE NUCLEAR REACTION OF DEUTERIUM NUCLEI ON A TRITIUM TARGET. THE GENESIS INSTALLATION IS MAINLY USED TO TEST THE EFFECTS OF A SINGLE EVENT IN THE FIELD OF MICROELECTRONICS, ON DIAMOND OR SILICON WAFERS. ACCESS TO THIS UNIQUE INSTRUMENT IS INCLUDED IN THE PAC-G SERVICE FOR INDUSTRIAL STAKEHOLDERS.

© F.Legrand/CEA

A gateway to large-scale instruments dedicated to electronics industry needs

PAC-G provides a single access point to large-scale facilities such as synchrotron and neutron sources through a cost-effective and rapid service tailored to innovation in electronics.

PAC-G provides the electronics industry with quick and easy access to some of the world's most advanced characterization facilities. Under the Nanoelec/Carac program, PAC-G also provides an extremely broad portfolio of individual but complementary characterization techniques.

A dedicated pipeline has been established to ensure that all proofs-of-concept validated within the program are successfully transferred and adopted by the relevant R&D partners.

"The partnership between Schneider Electric and PAC-G is vital, whether for service design— such as quality control or methodology development—or to bring our research and technology initiatives forward with the right expertise," comments Damien Bachellerie, Ph.D, Global Insulation & Dielectrics Technical Leader in the Innovation & Technology division at Schneider Electric.

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PAC-G IS A DEDICATED GATEWAY GIVING THE MICRO- AND NANO-ELECTRONICS INDUSTRY QUICK AND EASY ACCESS TO SOME OF THE WORLD'S MOST ADVANCED CHARACTERIZATION FACILITIES

© Havret/CEA, 2024

14. At the subatomic physics and cosmology laboratory in Grenoble (CNRS – UGA)

Sustainable integration of digital devices in SME processes

As far as the digital transition is concerned, technologies and components have little mass market focus and companies sometimes lack the information and the in-house skills needed to integrate new technologies. However, these technologies are also opportunities to expand their offering and strengthen their commercial position.

THE TECHNOLOGY DISSEMINATION PROGRAM IS MANAGED BY FLORENT BOUVIER (MINALOGIC), WHO LEADS THE EASYTECH INITIATIVE, AND CHRISTOPHE VAUTEY (CEA), IN CHARGE OF THE SYSTEM LAB INITIATIVE

FLORENT BOUVIER (MINALOGIC)

© P. Jayet/CEA

CHRISTOPHE VAUTEY (CEA)

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With the Technology Dissemination program, the partners in Nanoelec are promoting and accelerating the dissemination of emerging devices and new technologies in a variety of application fields; they are drawing more particularly on R&D skills in imaging, artificial intelligence, embedded software and electronic systems design. .

The program comprises two initiatives:

• The aim of the System Lab initiative is to exploit innovative imager components developed by the major industrial partners involved in R&D programs at Nanoelec. •••

AGENDA

PROMOTING THE ADOPTION OF EMERGING TECHNOLOGIES IN NEW APPLICATION FIELDS IS THE MOTIVATION BEHIND THE NANOELEC/ TECHNOLOGY DISSEMINATION PROGRAM

© Olivier Devise/Grenoble INP-UGA

• In the Easytech initiative, we make advanced electronic blocks and embedded software accessible to SMEs and mid-cap businesses, including those whose core business is anything but digital. The aim is to enable them to take part in the digital transition, to improve the added value of their products or their manufacturing processes. In 2024, Easytech assisted businesses positioned on a variety of markets and more particularely in the electronic components and embedded systems sector.

TECHNOLOGY DISSEMINATION PROGRAM AT A GLANCE

→ Vision
Sovereignty in the electronics industry requires efficient dissemination of innovative components and their adoption by national and European integrators and end-users

→ Ambition
To identify weak signals from the market and to accelerate the time to market of technologies developed by Nanoelec partners with fast prototyping and testing and access to emerging markets

→ Mission
- To help component and software manufacturers better understand the needs/possibilities of new applications,
- To provide companies, notably SMEs, with information to plan ahead for the arrival of new technologies,
- To contribute to the ambition of re-industrializing France and Europe,
- To strengthen investor confidence in IRT industrial partners

→ Partners
CEA, Minalogic, Grenoble-INP, Captronic/ Jessica France, STMicroelectronics, Lynred, Prophesee, GEM

AGENDA

Objective: Impact

Two startups which benefited from the Easytech initiative inaugurated their first plants in 2024.

An impact assessment within the program was carried out in November 2024 on a representative sample of SME/mid-caps that had been supported since 2012. It confirmed that the system is warmly welcomed by entrepreneurs owing to its flexibility and its reactivity. 78% of the projects lead to concrete follow-up in different ways: additional development, industrialization or commercialization.

Last July, the Limatech startup opened its first lithium batteries production plant in Voreppe, near Grenoble, with an investment of 10 million euros. This new industrial site, covering 1,200 m^2, will host three production lines with the aim of producing 10,000 batteries per year by 2030.

Last September, Dracula Technologies opened its Green Micro Power Factory in Valence, with an annual production capacity of 150 million cm^2 of printed organic photovoltaic cells.

INAUGURATION AT LIMATECH, IN 2024

© P.Jayet/Limatech

Easytech

Driven by the technology cluster Minalogic, Easytech is one of the Nanoelec IRT's technology dissemination tools. It focuses on the dissemination of technology blocks and the resulting extension of the product offering, based on a market pull approach, where SMEs express their needs. It helps SMEs, the main targets of the program – even if other types of businesses could take part in certain actions that fall within the scope of Easytech – are to diversify and improve their existing product or their manufacturing process, by adding intelligence. The targets of the tool are SMEs/mid-caps, in all activity sectors, which have an ambitious project to develop their activity based on innovation in the field of microelectronics.
Since 2021, 322 Easytech projects have been carried out, 70% of them with companies based in the Auvergne Rhône Alpes region[1].

Lidars for the automotive sector

Specifying a hardware/software implementation architecture.

To meet the needs of the automotive sector, the Steerlight startup and CEA developed a digital processing simulation chain to estimate the distance of lidar[2] targets, improve performance by means of advanced processing and specify a hardware/software implementation architecture.
The simulation tool includes state-of-the art parameters, allows calculation of the achievable performance in terms of range, distance and speed estimation precision, an operational processing chain and a proposed implementation architecture.

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LIDAR, THE AUTOMOBILE'S NEW ELECTRONIC EYE?
© RussPhotographer/ Pixabay

A network of foot-powered sensors

Connected insoles help prevent diabetic foot ulcers, blisters and neuropathies.

A patent has been filed as a result of Easytech's expertise implemented by Captronic for the Solecooler company. The company's goal is to retrieve energy from walking in order to power pressure and temperature sensors integrated into an insole. Solecooler, specializing in thermodynamic soles, is looking to instrument its insoles to transmit data to a smartphone. These connected insoles would be able to map the pressure and temperature across the sole of the foot, helping prevent diabetic foot ulcers, blisters and neuropathies.

The main difficulty in this project lies in the instrumentation of the insole to validate energy harvesting type operation.

The work performed within Easytech, with the support of CAP'TRONIC, includes the creation of a prototype silicon insole incorporating 150 battery-free measurement points, consuming only 1 mW. A consumption analysis was performed to extrapolate the energy needs of 50 sensors with Bluetooth transmission.

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1. The European Earashi program, whose French node is coordinated by the CEA as part of the Nanoelec/Pulse program, enables similar actions to be carried out at Community level.

2. Remote detection by laser is a distance measurement technique based on analysis of the properties of an artificially generated beam of light reflected back to the transmitter by the target.

Waste heat

Sensors, system and protocol to exploit industrial discharges.

The Hevatech company is looking to create a complete diagnostic service to characterize sources of waste heat, a major industrial issue.

"The economic and environmental impacts are significant, because the utilization of waste heat and its conversion into electricity and useful heat are ways of reducing energy bills and CO_2 emissions." As part of an Easytech project, the Hevatech engineers worked with students from Grenoble INP-Esisar – UGA to develop a system including autonomous temperature, pressure and flow rate measurement in industrial smoke discharges, at a frequency of 1 to 10 minutes over a period of one month. The data can be sent to a cloud, stored, processed and displayed. The system must be reusable and upgradable.

The work done includes identification of the existing appropriate sensors, communication protocols, acquisition units and software, as well as the development of a new acquisition unit and communication architecture and software for collecting, processing and displaying the data.

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EXPLOITING SOURCES OF WASTE HEAT, A MAJOR INDUSTRIAL ISSUE

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A miniature broad-band antenna

3D positioning for industry.

The Wheere company has developed a precise 3D positioning system (tracker), capable of operating both outdoors and indoors, with one-meter precision and one-kilometer range, using VHF signals and innovative processing. This system is independent of GPS, quick to set up and has low energy consumption.

Within Easytech, Captronic and Wheere evaluated the feasibility and performance of a specific antenna for the tracker with far greater wavelengths than the dimensions available in the package. Its expertise enabled a compact antenna to be designed and optimized, offering performance equivalent to a standard antenna. 20 prototypes were produced and used for demonstrations in the defense and oil & gas sectors.

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Electronics for music

Identifying a guitar's impedance to reproduce its behavior.

The Monday Noise startup is developing innovative electronic effects pedals for musicians. It is looking to rationalize its product development phase, testing in particular, which was hitherto primarily performed empirically.
The lack of scientific references on microphone circuits and their electronic interactions are a major stumbling block for a detailed understanding of the phenomena involved, thus limiting innovation in this field.
The Easytech project, developed in 2024 with Grenoble INP-UGA, designed an experimental module capable of recording, analyzing and playing back the signal of an electrical guitar, while faithfully reproducing the non-linear behavior of its impedance. This module can identify the impedance characteristics of each instrument and simulate their effect on the audio signal.
A dedicated software interface was developed to use these functionalities intuitively. It thus facilitates the test and research phases, while improving understanding and control of the electroacoustic interactions within the effects circuits.

THE LACK OF UNDERSTANDING OF THE NON-LINEAR PHENOMENA BETWEEN THE ELECTRONIC COMPONENTS AND THE SOUND PICKED UP BY A BASS GUITAR'S MICROPHONES CONSTITUTES A REAL TECHNOLOGICAL HURDLE IN THIS FIELD

© egonkling/pixabay

The need for a more integrated approach to eco-innovation

Aligning technological development with sustainable development criteria.

An article in the Sustainability review published by a team from CEA and Grenoble INP-UGA collaborating within the Easytech initiative of the Nanoelec/technology dissemination program, examines the essential aspects of eco-design that must be evaluated in the initial phases of innovation and explores the involvement of the decision-makers and entrepreneurs in the sustainability assessment process[3].
The study identifies the essential key criteria for assessing sustainable development criteria at an early stage, such as description of the innovation, the systemic vision, the functionality and the involvement of the stakeholders.

The results will help guide the political decision-makers, researchers and practitioners in the eco-innovation field, by providing a complete framework for assessing and promoting sustainable innovations right from the outset. The conclusions show the importance of obtaining expert knowledge in the eco-innovation diagnostic process. They also show the need for a more integrated approach to eco-innovation.

3. Peigné, S.; Ben Rejeb, H.; Monnier, E.; Zwolinski, P. Navigating the Eco-Design Paradox: Criteria and Methods for Sustainable Eco-Innovation Assessment in Early Development Stages. Sustainability 2024, 16, 2071. https://doi.org/10.3390/su16052071

System Lab/Addvisia

The Addvisia technology platform, sponsored by a CEA team and derived from an IRT Nanoelec initiative, creates a community of interest around the topic of multimodal and multispectral imaging, in order to explore the full potential of combined imagers and identify new applications.

This modular platform brings together technology suppliers, integrators and users around common objectives: better understanding why and how imagers can be combined for new uses, in an agile experimentation environment. In 2023, the platform was implemented for numerous use cases, including snowpack analysis, observation of soil core sampling for environmental analysis, as well as trajectory analysis and physiological effort monitoring.

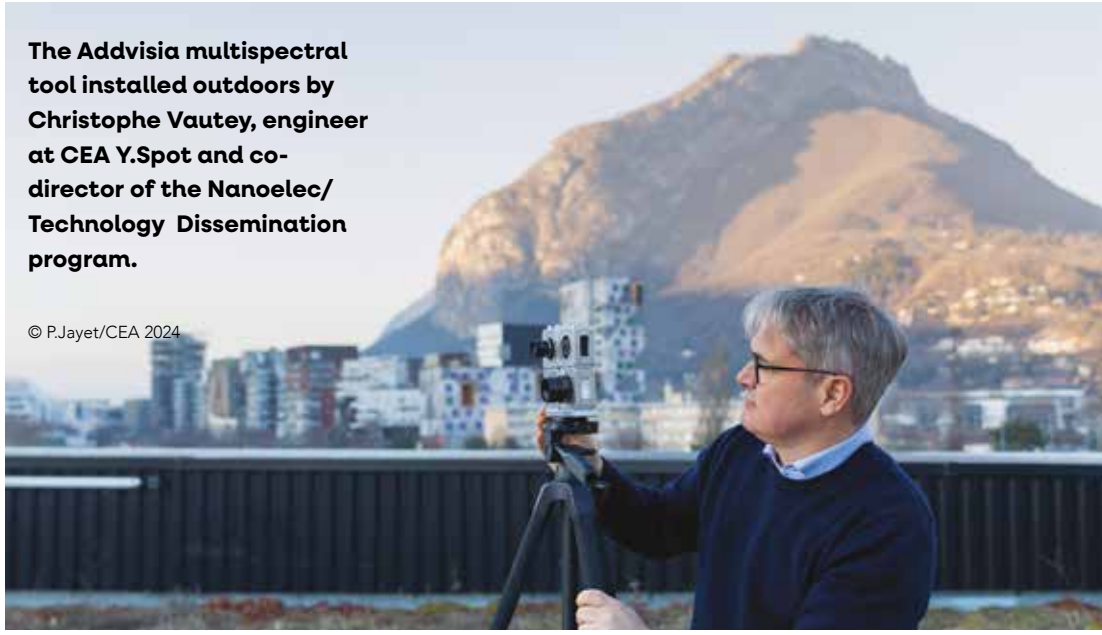
ADDVISIA PLATFORM UNDERGOING TESTING IN Y.SPOT LAB CEA GRENOBLE

© P.Jayet/CEA 2024

Displaying strata in the snowpack

The Addvisia platform could help achieve a clearer understanding of the physics of avalanches.

Propagation Saw Tests (PST) are designed to evaluate the propensity of a snowpack layer to fracture and potentially lead to an avalanche. PST offer valuable insights into snowpack structural integrity, identifying weak layers that may fail under stress. *"We conducted PSTs utilizing infrared imagers and event-based sensors to capture detailed imagery of the snowpack,"* reports Charles-Elie Goujon (CEA) as a first author of a study published by a team from CEA, Université de Savoie Mont Blanc and the Data Avalanche Association[4]. This innovative approach enabled information beyond the visible spectrum to be examined with a SWIR imager and micro-movements within the snow to be detected using an event-based sensor. SWIR imaging offers a groundbreaking method for analyzing snowpack layers, revealing critical details invisible to the naked eye. *"The methodology introduces new parameters for snowpack and PST analysis. Following these new parameters could improve knowledge of the weak layer and the propagation of rupture,"* underlines Charles-Eli Goujon.



The Addvisia multispectral tool installed outdoors by Christophe Vautey, engineer at CEA Y.Spot and co-director of the Nanoelec/ Technology Dissemination program.

© P.Jayet/CEA 2024

The imaging game

The Gesturama game was presented at the Tech&Fest Grenoble festival on February, 2025, and offers a unique experience in which technology meets creativity.

"The aim of the Gesturama project is to offer the general public access to complex technologies by offering an entertaining, immersive experience," explains Hélène Michel, lecturer-researcher at the Grenoble Management School (GEM), who conceived the project.

GESTURAMA DEMONSTRATOR
© GEM

The collaboration with Nanoelec/ Addvisia is an ideal opportunity to combine our students' game design skills with the technology of the ecosystem. After several iterations, we opted for a captivating concept: an arcade game with gaming mechanics inspired by a cult classic from our childhood, offering fluid and engaging interaction. Over and above the game itself, Gesturama stimulates the curiosity of the participants, who can then explore further by discovering the Addvisia platform, the Lynred photobox and by taking part in a creative session on future uses of imagers," Hélène Michel explains.

Gesturama incorporates the innovative VL53L8 Time of Flight sensors of the FlightSense range from STMicroelectronics, through gesture memorization games produced by a collaboration between GEM, STMicroelectronics and CEA/Y.Spot. The Lynred imagers were also present around the Addvisia platform at Tech&Fest 2025.

For Christophe Vautey, co-director of the technology dissemination program at IRT Nanoelec: *"Addvisia explores the potential of many of the existing imagers, in order to identify new applications. Using gaming as a means of disseminating technology is a challenge enthusiastically tackled by the team, creating the entire Gesturama system in just a few weeks."*
"In combination with an STM32 microcontroller, the VL53L8 Time-of-Flight module from ST's FlightSense® range is a key element in the arcade game," says Jean-Pascal Mangano, Head of collaborative projects at STMicroelectronics. *"It opens the door to new ways of understanding the interactions between the player and the gaming platforms and offers the users a unique, innovative and entertaining experience."*

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4. Goujon, C.-Elie, Duclos, A., Perillat, C., & Pourraz, F. (2024). ISSW 2024, Tromso, Norway

Biathlon tracker

Recording the impact of a bullet on a target.

Following the ideas competition with the "high level sports" class at the GEM, the "Biathlon Tracker" project was selected for exploration with Addvisia. The project concerned the use of the platform's imagers to help biathletes know where the bullet touched the target, so that they could improve their aim.

Addvisia was used during two test sessions on a firing range. The purpose of these tests was to find out how to use the sensors in order to record the impact of the bullet on the target.

The first session identified the correct locations and settings of the imagers in order to pick up the impact of the bullet and observe that the bullet's trajectory to the target was visible. The second session highlighted the superposition of visible and event-based imaging in order to visualize the target and the trajectory and impact of each shot.

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DURING A BIATHLON SESSION

© Image by Ebowalker/Pixabay

Biathlon tracker: a use case selected for an entrepreneurial innovation course

An entrepreneurial innovation course was designed by GEM in collaboration with Nanoelec/Addvisia. It includes a marketing and strategy approach (business model) based on technological use cases. The target audience consists of professionals liable to be involved in an entrepreneurial process, more specifically high-level sportspersons. Pedagogical engineering aims to explore the value creation potential of the technologies to solve their problems.
"What the students produce in a serious gaming context such as this is always interesting," observes Xavier Brenière, Head of the applications laboratory at Lynred. *"This shows the extent to which there are still uses to be explored with our sensors."*

Movement capture and analysis in sport

Addvisia's movement capture and analysis capabilities are showing promise for several uses in the field of sports, notably for greater athlete safety and improved umpiring.

The pertinence of Addvisia's sensors in analyzing rapid movements, was demonstrated for two different but complementary applications, the prevention of concussion and improving umpiring in tennis.

To prevent concussion, the Prophesee event-based sensors demonstrated sufficient time precision to measure accelerations during impacts. This enables the data to be correlated with the events, thus offering a solid base for developing prevention protocols.

For umpiring in tennis, merging data from the event-based and visible sensors made it possible to accurately recreate the trajectory and position of the ball. This paves the way for the creation of an automated line judge, thus improving umpires' decision-making.

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Sustainable development as a driver of innovation

The main goal of the Human Capital and Learning Design program is to provide an agile and proactive response to the skills needs of the consortium's partners, directly related to R&D, technological dissemination and innovation activities.

SYLVIE BLANCO, SENIOR PROFESSOR OF TECHNOLOGY AND INNOVATION MANAGEMENT AT GRENOBLE ECOLE DE MANAGEMENT (GRENOBLE GRADUATE SCHOOL OF BUSINESS), CO-DIRECTOR OF THE NANOELEC/HUMAN CAPITAL & TRAINING DESIGN PROGRAM

© P. Jayet/CEA

PANAGIOTA MORFOULI, PROFESSOR AT GRENOBLE INP-UGA, CO-DIRECTOR OF THE NANOELEC/HUMAN CAPITAL & TRAINING DESIGN PROGRAM

© P. Jayet/CEA

This program lies at the heart of the Nanoelec ecosystem, whose skills requirements stand out in their intensely technological nature, wide diversity of applications and firm commitment to a sustainable impact.

In 2024, 42 modules were designed and/or adapted, including 34 for initial training (level Bac+5 years) and 7 for continuing education. These developments led to effective deployment throughout the year, representing a total of 9,202 participant days. •••

AGENDA

To illustrate the innovative nature of the program and its commitment to sustainable development, a number of actions are highlighted: two tools to raise awareness of the challenges of a responsible digital world, a workshop dedicated to the societal and environmental impacts of interactive screens and the rebound effect, as well as a gamification approach aimed at making technological communication more accessible to the general public. •

CHIF PROGRAM AT A GLANCE

→ **Vision**
Enhancing the competitiveness of the electronics industry requires strong interdisciplinary collaboration, agile teamwork, and the continuous development of dynamic knowledge and skills

→ **Ambition**
Design and pilot an integrated, flexible, and tailored learning ecosystem that reinforces human capital and boosts the innovation capabilities of the Institute and its partners

→ **Mission**
Develop and deliver innovative training content and formats across three key dimensions: core competencies, experiential learning, and learning communities — all geared toward addressing emerging societal and technological challenges

→ **Partners**
Grenoble INP-UGA, Grenoble Ecole de Management (GEM), STMicroelectronics, Schneider Electric

Interactive Screens and the Rebound Effect

Over seventy students from Grenoble INP-UGA and Grenoble École de Management explored the environmental and societal impacts of interactive screens, with a particular focus on the "rebound effect" associated with the widespread adoption of new technologies.

In February 2024, the annual edition of the Chif program's "Sustainable Electronics" workshop brought together experts from CEA, STMicroelectronics, Aledia, Pyxalis and the G-Scop laboratory, and students from Grenoble INP-UGA/Phelma and Grenoble École de Management.

"This year, students worked on the topic of interactive screens and the rebound effect," explains Sylvain Engels, Professor at Grenoble INP-UGA and Digital Team Manager at STMicroelectronics.
"The focus was placed on large-format interactive screens such as whiteboards, information kiosks and control terminals," adds Laura Mazzarella, Nanoelec/Chif pedagogical engineer at Grenoble INP-UGA/Phelma, who co-designed the workshop with Estelle Belin di Stephano, also a pedagogical engineer. *"Interactive screens are now ubiquitous: smartphones, tablets and more. Students were asked to reflect on the environmental and societal impact of these devices, and to analyze how the rebound effect might offset the intended sustainability gains."* •••

The rebound effect refers to the unintended consequences where improvements in energy efficiency lead to increased overall consumption, ultimately reducing or even negating the expected environmental benefits.

"Improving energy efficiency doesn't automatically translate into reduced energy consumption," explained Bruno Gayral, researcher at CEA who introduced the workshop. *"In fact, global energy use has surged in recent decades despite major advances in efficiency. Take LED technology, for instance: while more sustainable and efficient, it has enabled new applications — from hydroponics and indoor farming to architectural lighting and a proliferation of screens — that have ultimately increased overall energy demand."*

During the workshop, students were divided into 13 groups of 5 to 6 participants, with each group assigned to a specific application domain such as education, entertainment or business.
After analyzing literature outlining both the benefits and drawbacks of interactive screens, each group was tasked with designing and presenting solutions aimed at reducing their environmental and societal impacts — while explicitly factoring in the rebound effect. *"What stood out to me was the students' enthusiasm and the relevance of their proposals,"* noted Sylvain Engels. *"The quality of the presentations they delivered - in under 24 hours - was remarkable. One group has even expressed a desire to pursue their concept further, and I fully intend to follow their progress."*
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PROFESSIONALS AND STUDENTS COLLABORATED TO TACKLE THE CHALLENGE OF SUSTAINABLE ELECTRONICS DURING THE 'INTERACTIVE SCREENS AND REBOUND EFFECT' WORKSHOP ORGANIZED BY CHIF IN FEBRUARY 2024

A student group working on the attractiveness of the microelectronics sector in Grenoble INP-UGA/Phelma

© P.Jayet/CEA

The Addvisia platform adapted to a campaign for a commercial brand

From concept to prototype, the Red Bull Clash fictitious experiment shows how gamification, technology and brand can come together to create impactful interactions with the consumers.

The Gesturama pedagogical gamification exercise, developed by Nanoelec/Chif to promote the Nanoelec/Addvisia platform at the Tech&Fest 2025 festival goes beyond just digital design. The students from *Grenoble École de Management* built a complete arcade stand incorporating TOF (Time-of-Flight) sensors from ST-Microelectronics to detect the players' movements in real-time. They cooperated with Didier Chabanol from the IVèS company to understand communication through gestures, as well as markets and trends. They did the coding work with Fanny Aubry from the CEA/Y.Spot design team. The game transforms Red Bull's iconic symbols into an interactive brand experience. It uses gesture recognition technology to create immersive engagement for the customers. It promotes a strong community culture through ritualistic movements.

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Raising awareness for a responsible digital world

Starting from a project designed at the Ense3-G INP school to determine the carbon footprint of digital usages in the school, two awareness-raising tools were created within Nanoelec/Chif.

USING A SERIOUS GAME IN A WORKSHOP TO PROMOTE EFFECTIVE HYBRIDIZATION STRATEGIES AND ENHANCE ENVIRONMENTAL AWARENESS

"The aim is to enable a wider audience to acquire knowledge of the socio-environmental issues of digital applications, encourage them to take a fresh look at their practices and usages, in order to adopt a more responsible approach," explains Loane Danes, pedagogical engineer and "Sustainable Development & Societal responsibility" coordinator at Grenoble INP – Ense³, UGA. This project, which was initially designed to assess the carbon footprint of digital usages at the Ense³ school, was expanded and implemented in two pedagogical tools within Nanoelec/Chif.

The project was presented at the 2024 symposium for sustainable electronics and digital applications in Grenoble[1] and also during a Nanoelec webinar intended for the French electronics community in February 2025[2].
In the "Digital escape" game, the participants take part in an adventure where they discover the lifecycle of a smartphone and the corresponding impacts, while solving puzzles. The "Digital Odyssey" workshop, which lasts about two hours, asks the participants to think about the material nature of the digital world, its impacts at each step along the lifecycle, and its role in the societal and environmental transition[3].

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1. Danes, L., Morfouli, P., Mazzarella, L., Rouge, M., & Le Rasle, C. (December 12, 2024). Digital Escape and the Digital Odyssey: Two tools to raise awareness of the issues of a responsible digital world [Poster]. Symposium for sustainable electronics and digital applications, Grenoble

2. https://irtnanoelec.fr/actualites/webinaire-ingenierie-pedagogique-pour-le-numerique-responsable/

3. The English version is also available for the partners in the European GreenChips project, which include Nanoelec

Hybridizing profiles on the impact of interactive displays

A paper presented at the “Frontiers in Education FIE 2024” conference, in the "innovative practice" category, describes a workshop that emerged from students’ increasing environmental awareness.

The environmental and societal impacts of technology are not sufficiently integrated into students' curricula. In an innovative Nanoelec/Chif workshop, 74 students, with profiles ranging from engineering to business, were brought together with ten experts (including researchers from private companies, managers, and academics). *“This type of activity provides tangible support for the movement towards technological change, as students have the opportunity to engage with experts actively working to drive that change. By exploring applications like interactive displays, which combine the functionalities of PCs, tablets and whiteboards with interactive and collaborative features, we triggered meaningful discussions that we hope will inspire future careers,”* explains Estelle Belin Di Stephano, training engineer at Nanoelec/Chif as a first author of the paper[4].

Emerging pedagogical methods

Hélène Michel, a professor at GEM and sponsor of the Gesturama project within Nanoelec/Chif, explores the contributions of new pedagogical approaches.

How are serious games transforming research?

H.M. One of the most innovative roles of serious games could lie not in the dissemination of messages, but in the creation and collection of new information or knowledge, by using the game in the same way as a research laboratory[5]. By gaming with the students, the lecturer-researcher becomes an agent provocateur who influences the dynamics being studied, revealing behaviors that would otherwise be inaccessible via traditional methods, Serious games are transforming research, encouraging more creative and engaged exploration of the social phenomena.

Design fiction prototypes the future

H.M. Increasing numbers of companies are hiring design fiction scriptwriters and designers. This is an immersive method which uses science-fiction to project potential futures. In our design fiction classes, the students write and record stories about an everyday moment as it could be some time in the future. Thus, on the topic: ”A day in the life of a Grenoble student in 2050”, questions regarding the integration of technologies, in particular those arising out of Nanoelec, the possible future of Alpine ski resorts and all the subjects previously worked on with the ecosystem of partners, are covered in a radio news broadcast of the future.

What do your students do?

H.M. In the same way as scriptwriters, they imagine how technologies and societal trends could change. For example, what would happen if we understood the language of dolphins? If robots went on strike?[6] In the process as developed, the students must embody this future everyday moment via an artifact. They therefore prototype an object of the future in fab lab type locations.

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4. Belin-Di Stephano, E., Morfouli, P., Mazzarella, L., & Le Rasle, C. (October 13, 2024). Workshop on “Interactive Displays: Use, Benefits, Environmental and Social Impacts”. Frontiers in Education FIE 2024, Washington DC, USA.

5. Hélène Michel, Z. S. (May 31, 2024). Serious games as a provocative research method? [Journal]. https://www.openscience.fr; OpenScience : OUI.

6. Michel, H., & Blanco, S. (September 22, 2024). Training students to imagine possible futures through design fiction. The Conversation. http://theconversation.com/avec-le-design-fiction-former-les-etudiants-a-imaginer-les-futurs-230317

Increasingly involved in embedded artificial intelligence

Artificial intelligence (AI) expertise is increasingly important in order to differentiate products developed specifically for applications.

Nanoelec tackles AI from the embedded electronics standpoint: the development and generalized use of embedded AI applications is becoming essential to manage large quantities of data which require local processing at component and system levels. The aim is to make these components able to make decentralized, autonomous and reliable decisions.

Processing must therefore be integrated close to the sensor in order to optimize the data stream and guarantee that the data remain intact and confidential. This offers a good compromise between the data streams from the sensor to the user and the energy footprints of the sensor and central computer processing smaller quantities of data.

The teams involved at Nanoelec are primarily focusing on image sensors and on the security of components and artificial intelligence systems.

Whether for designing new circuits and architectures, taking account of the environmental impacts of the technologies, or developing dedicated components, AI is identified as one of the major challenges for the electronics sector over the coming years and the Nanoelec partners have confirmed their interest in the subject.

SMART IMAGER

Edge AI for smart imager

3D sensor assembly

Imaging is one of the three main fields that use AI. The aim is not only to achieve better image quality, but also to extract relevant data from the image, taking account of the environment, the object, the scene (potentially across a range of lighting conditions), and knowledge of the context.

Research teams working on the Nanoelec/Smart Imager program are focusing on new advanced silicon technology building blocks allowing 3D sensor assembly, on the design of new architectures allowing the implementation of adapted neural networks, and on the development of new design methodologies and tools simultaneously taking account of software and hardware requirements in dedicated EDA tools. In a GdR IASIS talk at the CNRS Conference (May 2024), Thomas Mesquida & al. demonstrated how a GNN (Graph Neural Network) inherently makes a better feature extractor for event-based data than Convolutional Neural Networks (CNNs) or Spiking Neural Networks (SNNs). Graph building constraints drastically reduce its cost while maintaining applicative performance.

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CAD tools and design methodology for Edge AI smart imager

AI engines simulator

CEA and Siemens EDA are developing high-speed simulation tools on circuit abstraction models in order to accelerate their functional verification. The project uses AI engines to detect at which point in the simulation greater precision is required and thus make the transition from a virtual mode to a more precise hardware mode. Later on, this tool will be integrated into a verification tool suite which will provide a much greater and faster level of simulation and verification.

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PHOTONIC SENSORS

Laser on silicon

Mach-zehnder interferometer

With the photonics on silicon platform developed at CEA-Leti, the teams working on the Nanoelec/Photonic Sensors program are involved in a number of European projects to develop neuromorphic architectures dedicated to artificial intelligence applications (learning and inference) for ultra-fast detection of cancer cells (flow cytometry), security applications, image recognition and telecommunications. The circuits studied consist of a pulsed laser associated with a Mach-Zehnder interferometer array controlled by BTO base phase shifters. Developments are expected in lasers integrated on silicon and the use of non-volatile phase shifters based on phase change materials (PCM).

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PULSE

Secure implementation of AI and cryptography

New physical security analysis tools

The teams at Nanoelec/Pulse are looking at secure implementation of artificial intelligence algorithms on embedded systems and more particularly on 32-bit microcontrollers: protection of the integrity and confidentiality of embedded models and security of embedded learning, with characterization of the threat and definition of protection solutions. They are also studying the optimization and hardware acceleration of post-quantum cryptography scheme implementations, along with the creation of new physical security analysis tools.

Security of health devices

AI and intrinsically secure processor

In most connected objects and connected medical devices today on the market, little if any attention is paid to cybersecurity. The teams at Nanoelec/Pulse are studying the hardware and software security of medical devices (MD) and connected health objects (CHO), more specifically by securing the implementation of artificial intelligence models within these objects themselves, improving the concept of the intrinsically secure processor and setting up characterization and comparison (RISC-V) and appropriate security testing (MD) platforms.

Preventing physical attacks at edge AI

Security challenges for federated learning systems

Federated Learning (FL) is a decentralized learning paradigm consisting in training local AI models, usually on edge devices, that are sent to a central server to create a global model. *"The main advantages of FL are to not transmit potentially private local training data to the central server as well as to bring different actors together with a common learning goal,"* underlines Bastien Vuillod (CEA Leti). However, FL also comes with serious security issues regarding both the confidentiality of the data and the integrity of the system, typically with poisoning based threats. In a scientific paper presented at the Ressi Conference[13].

Bastien Vuillod et al. explored the wide and complex attack surface of FL with a large panel of possibilities that an adversary can exploit to break the confidentiality or integrity of these distributed systems. "Since FL systems usually rely on edge devices that can be targeted by physical attacks, we also discuss advanced implementation-based threats," adds Bastien Vuillod.

13. Vuillod, B., Moellic, P.-A., & Dutertre, J.-M. (15 May, 2024). Security Challenges for Federated Learning Systems : A Complex Attack Surface. RESSI. Rendez-Vous de la Recherche et de l'Enseignement de la Sécurité des Systèmes d'Information, Eppe-, Sauvage (France)

International & Europe

In an international context that underscores the challenges of sovereignty, the IRT teams have decided to consolidate an international strategy around a few simple principles:

- Giving priority to reinforcing the positions of the consortium's current members, which already have global reach but which are faced with international competition,
- Continuing support for national startups capable of addressing international markets,
- Accelerating international partnerships, in particular in the fields of materials and production or instrumentation equipment,
- Finally, re-energizing Europe within the new framework programs and the Chip Act.

From the scientific viewpoint, it is worth noting the presence at various major conferences in 2023: IEEE Silicon Photonics, Date for design work, ECTC for 3D integration technology, FIC for cybersecurity, display Week, Mems & Imaging Device Summit.

SMART IMAGER

Infrared sensors for European defense

Night-vision performance

Lynred, a Nanoelec partner, is coordinating the European participants in the Heroic project. The project's goal is to develop the next generation of Read-Out Integrated Circuits (ROIC) in Europe, for IR detectors intended for defense applications. These detectors will then be integrated into high-performance imaging arrays for airborne, land and naval systems. This new generation of detectors in particular requires increased night-vision performance to identify targets or detect events. The Nanoelec/Smart Imager teams involved will develop a surface preparation process for the read-out and/or detection circuit, in order to allow electrical connection of each pixel in the imager sensor matrix to its read-out electronics.

www.heroic-project-edf.eu

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HEROIC EU PROJECT TO DEVELOP THE NEXT GENERATION OF HIGH EFFICIENT READ OUT INTEGRATED CIRCUITS FOR DEFENCE.

© AdobeStock

PHOTONIC SENSORS

Cytometry

Reducing computing time

Nanoelec has been part of the EU Neoteric project aiming to develop a reconfigurable photonic circuit to detect cancer cells in a solution (cytometry) using a machine learning (ML) method. The photonic circuit developed by CEA, within Nanoelec, incorporates new BTO ($BaTiO_3$)-based phase shifters to ensure energy efficiency. This integrated photonics-based solution is expected to reduce computing time compared with the conventional image analysis method. The project ended in April 2024.

neoterich2020.eu

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Neuromorphic computing

Silicon-integrated lasers

The EU Prometheus project aims to manufacture a complete neuromorphic computing chip (set of interferometers using low-consumption BTO-based phase shifters for the synaptic part and pulsed lasers integrated on silicon for the neural part). Nanoelec supports the technological solution based on SOI wafers manufactured by Scintil Photonics, on which BTO technology will be integrated by Lumiphase and III-V technology by CEA-Leti.

prometheus-he.eu

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Secure hardware accelerators

Integrated lasers and non-volatile phase shifters

EUNeuropuls will develop the very first secure hardware accelerators based on novel neuromorphic architectures and PUF-based security layers leveraging the benefits offered by the integration of photonics, PCMs and III-V materials. Through Nanoelec, technological developments are expected in silicon-integrated lasers and the use of non-volatile phase shifters based on PCM material.

neuropuls.eu

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PULSE

A Safe, Human-oriented Industry

Improving working conditions

The European Earashi project (Embodied AI/Robotics Applications for a Safe, Human-oriented Industry) is associated with the Nanoelec/Pulse program through its partners CEA and STMicroelectronics. It supports European startups and SMEs in the adoption of advanced eco-responsible digital technologies (in particular AI, data and robotics), to help workers in their day-to-day activities and improve their working conditions (safety, health and well-being) eventually leading to a boost in productivity.

For the ten projects selected, the requirements are the development of robotic assistance products, tools to facilitate the digitization of manufacturing process management tools and projects designed to improve human well-being and safety in the workplace. All the projects received customized awareness-raising of eco-design, ethics and data protection, cybersecurity, and incorporating the human being into the process, to help with acceptance of and trust in these new technologies.

earashi.eu

A COBOT TO PREVENT MUSCULOSKELETAL DISORDERS

FACING E-WASTE PILE, REDUCE, RELIABILITY, REUSE, REPAIR, REFURBISH, RECYCLE (6R CLAIMS OF THE EECONE EU PROJECT)

PULSE

Reducing the amount of electronic waste

An eco-design tool for electronic systems

EECONE (European ECOsystem for greeN Electronics) is a European project involving 49 partners from more than ten European countries, including 15 from France, among which are STMicroelectronics, CEA, and Grenoble INP-UGA. The common goal is to reduce the quantity of electronic waste Europe-wide. CEA, in collaboration with the other partners of Nanoelec, developed a first mock-up of a tool for the eco-design of electronic systems, notably power electronics.

At the same time, CEA is working on obtaining a database of the environmental impacts of electronic components to be input into the tool. CEA, STMicroelectronics and Grenoble INP-UGA are preparing a map of the involvement of the EECONE partners in the 6R (Reduce, Reliability, Repair, Reuse, Refurbish, Recycle).

Legal interception in cybersecurity

Blocking criminal and terrorist organizations

The POLIIICE project (Powerful Lawful Interception, Investigation, and Intelligence) is a European HORIZON-CL3-2021-FCT-01 project involving 23 partners (>10 nationalities).

The purpose of this three-year project is to study and develop new techniques and tools for legal interception, to provide local authorities with up-to-date resources to deal with technological developments (5G&Beyond, post-quantum cryptography, etc.) which could be exploited by criminal and terrorist organizations. CEA is developing directly exploitable fault injection techniques to study flaws in cryptography algorithms, notably in post-quantum cryptography.

Autonomous vehicle

Six scenarios based on road accident studies

Through Inria, Nanoelec is involved in the French PRISSMA research project which aims to propose a platform overcoming the technological hurdles to the deployment of secure AI systems, and integrating all the elements needed for the performance of autonomous vehicle approval activities and validation in its environment for a given use case. Although the simulation of critical scenarios is essential, it cannot yet fully replace real testing, which nonetheless remains time-consuming and resource intensive.

The teams at Inria proposed an improved methodology using augmented reality, providing an intermediate test method which allows complete, real-world testing at reduced cost and with improved realism. To demonstrate this methodology, tests were run in a controlled environment using six critical scenarios selected from road accident studies.

Reuse of electronic components

Memory data deletion

The European Repex project is focusing on the recycling of electronic devices by deleting data from their memories using X-rays. The purpose is to develop an industrial method for wiping data that is faster and more reliable than today's software or physical destruction solutions, while enabling electronic equipment to be reused. The main advantage of the X-ray wiping method lies in its ability to delete once and for all the data stored in the flash memories that can be found in numerous electronic objects (telephones, SSDs, USB memory sticks, SD cards, etc.).

However, there are many technical challenges. For mobile phones, the diversity of the components complicates optimization of the irradiation process. The aim is to find the right compromise between complete deletion and preservation of the other components so that they can be reused. In 2024, CEA started a life cycle assessment (LCA) of the X-ray source equipment.

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Detection of cross-border cyber-threats

Pooling alerts between security operations centers

The European SAFE4SOC project brings together ten European partners around information sharing concerning the detection of cyber-threats between cross-border security operations centers (SOC). An alert pooling format is being studied to identify the information that can be shared between SOCs, in particular incident information.

The eARGOS solution developed by CEA under the Nanoelec/Pulse program is being proposed in the project. This solution relies on an AI-based intruder detection system and hardware data close to the electronic components. One of the project's challenges lies in the exchange of heterogeneous information between the SOCs of different countries.

safe4soc.eu

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INSIDE A PC: MOTHERBOARD, CPU SOCKET AND RAM MEMORY

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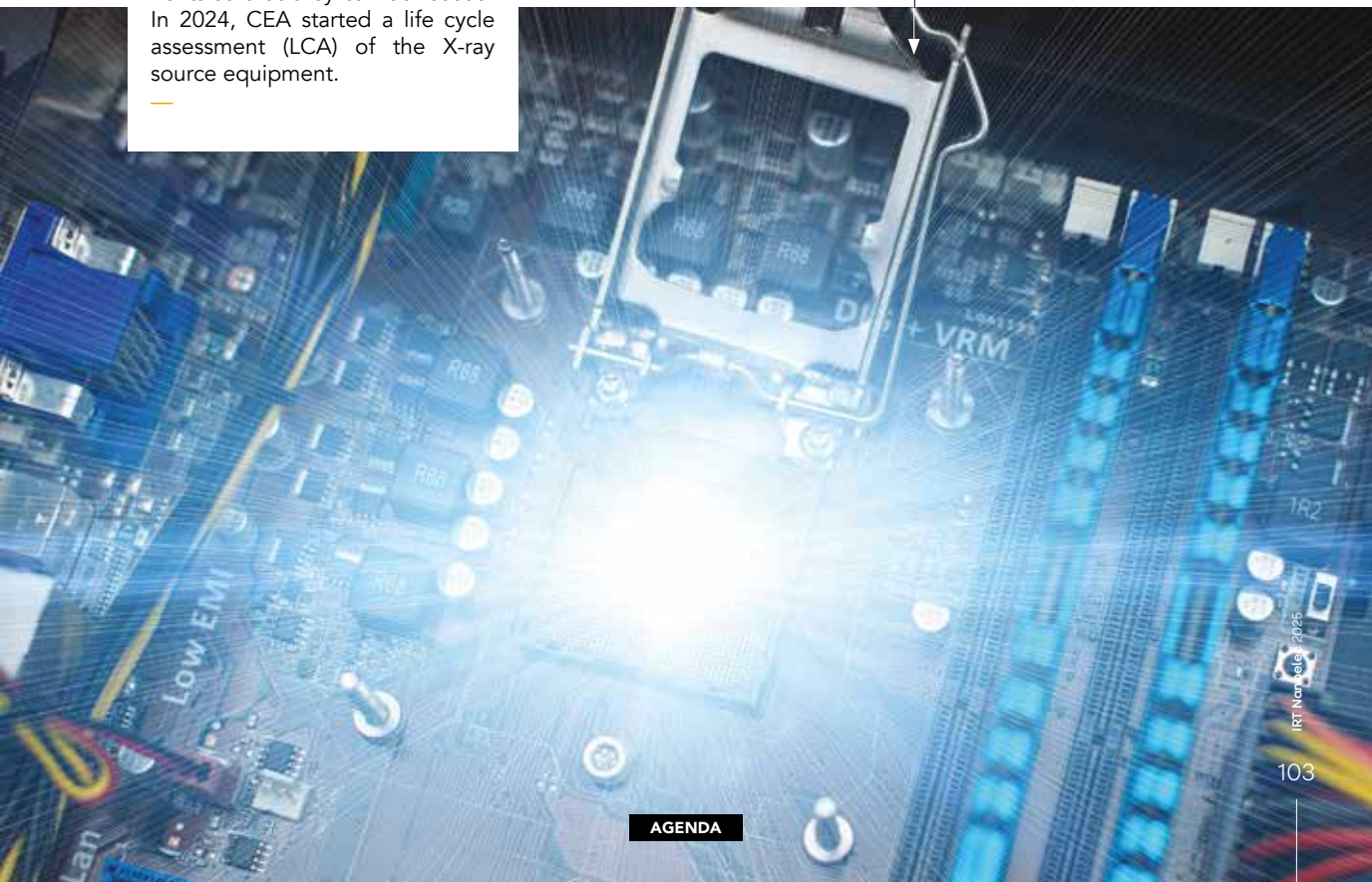

CHARACTERISATION

Nanomechanical materials characterization in industry

New methodologies

NanoMECommons is an H2020 collaborative project focusing on the development of new characterization methodologies tailored to industrial needs in the nanomechanical field. .

nanomecommons.net

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Exploring radiation effects for industry and research

A distributed research infrastructure

Radnext (for RADiation facility Network for the EXploration of effects for indusTry and research) is an H2020 collaborative project running a distributed research infrastructure in Europe, open to the industrial and university irradiation community.

radnext.web.cern.ch

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Nano Foundries and Fine Analysis

Colocation of nanofabs and high-level analytical instrumentation

Nano Foundries and Fine Analysis (NFFA) is an H2020 collaborative project which proposes launching the first distributed research infrastructure within the EU, offering access to high-level instrumentation to support activities in the nanosciences and nanotechnologies. The idea is to colocate nanofabs and high-level analytical instrumentation. Within the NFFA consortium, IRT Nanoelec proposes access to the BM05 beamline, via the ESRF, in coordination with CEA-PFNC.

nffa.eu

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ENGINEERS OF THE NANOELEC;/PAC-G ARE WAINTING FOR YOU AT ILL TENIS IRRADITION PALTEFORME, INTHE FRMAE OF NANOELEC/CARAC PROGRAM

© A.Havret/CEA

TRAINERS TO SHAPE A COMPETIVE AND SOVEREIGN SUSTAINABLE ELECTRONICS BUSINESS AT EU LEVEL

© Utopik/CEA

HUMAN CAPITAL & TRAINING DESIGN

Training Design for Green Electronics

Expand the dissemination

The Nanoelec/Chif program is committed to transforming teaching methodologies by introducing more dynamic content, particularly with a focus on sustainable development. It emphasizes experiential learning and broad access to resources, providing a common platform for a diverse range of learners. Additionally, the Chif program is closely linked to the EU GreenChips-EDU project through Grenoble INP-UGA.

This initiative connects the Nanoelec/Chif program to EU priorities, offering an opportunity to expand the dissemination of the Chif content.

STUDENTS AND PROFESSIONALS WORKING TOGETHER ON BUSINESS IDEAS TO REDUCE THE REBOUND EFFECT OF DISPLAYS

© Grenoble INP-UGA

Training design for Greener Chips

Student empowerment and engagement

In Europe, the EU Chips Act aims for a 20% share of global semiconductor production by 2030. However, there is a significant shortage of skilled workers, The GreenChips-EDU project seeks to address this gap by increasing the number of students pursuing electronics and empowering them to contribute to a green and circular economy. This initiative connects the Nanoelec/Chif program to EU priorities, offering an opportunity to expand the dissemination of the Chif content.

Transformational issues of organizations & businesses

Managers to design advanced digital

The aim of the EU Digi-Me project is to nurture a European community of leaders capable of designing, initiating and implementing innovations based on advanced digital technologies (AI, generative AI, augmented intelligence, digital twin, blockchain, data analytics, and IoT). The project connects the Nanoelec/Chif program to EU strategic and transformational issues facing businesses and it provides an opportunity to increase dissemination of the contents of Chif.

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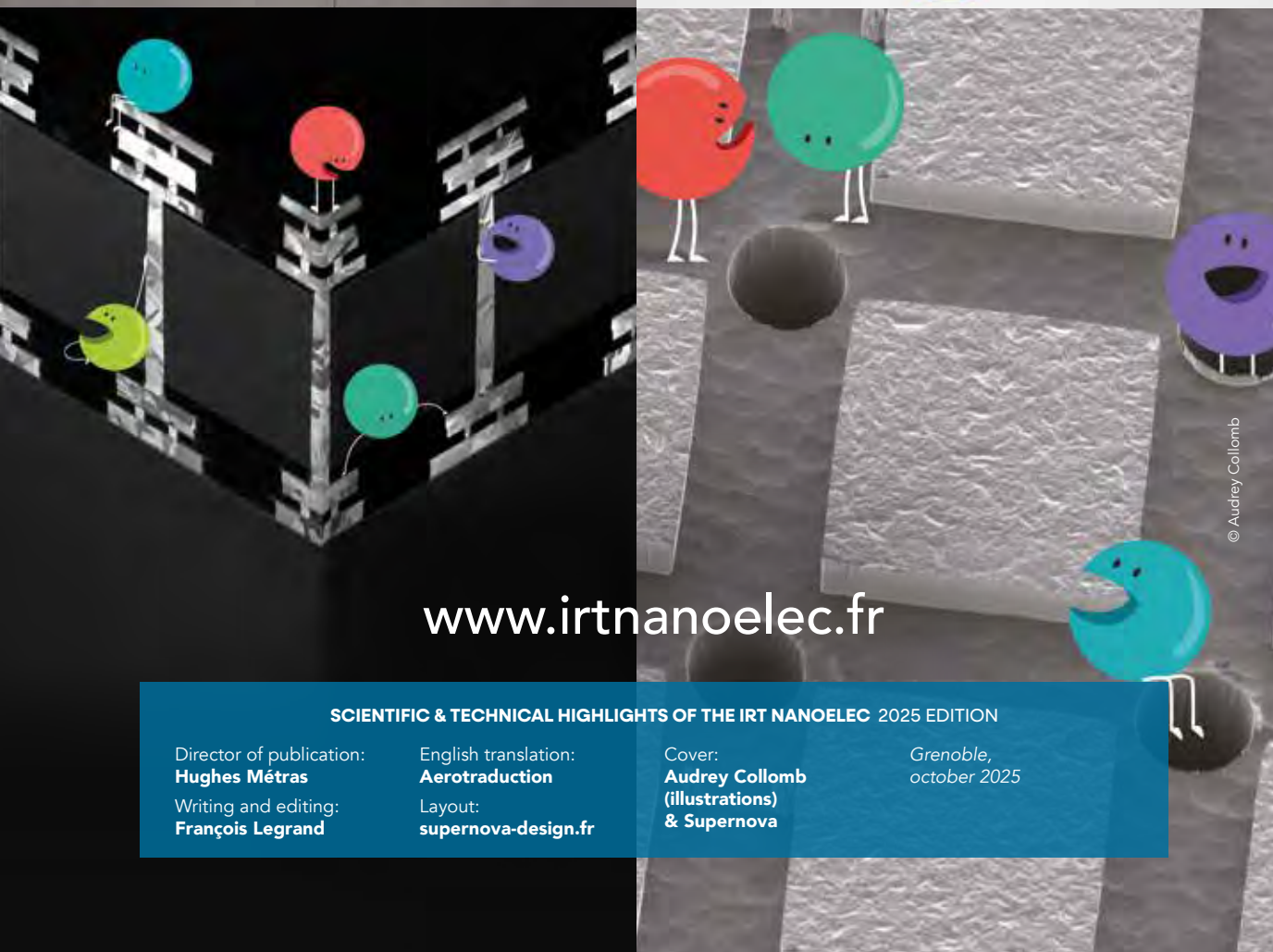

www.irtnanoelec.fr

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