SCIENTIFIC & TECHNICAL HIGHLIGHTS

2022 EDITION

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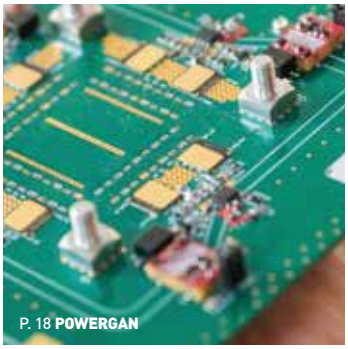

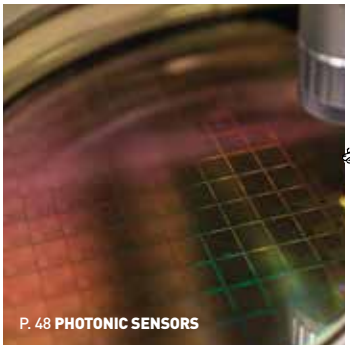

DIGITAL TRUST

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HUMAN CAPITAL & TRAINING DESIGN

ARTIFICIAL INTELLIGENCE

SUSTAINABLE DEVELOPMENT

EXPLORING THE FUTURE OF ELECTRONICS

IRT Nanoelec runs multi-partner programs to make the electronics sector more competitive, and greener to contribute to the sustainable development of society.

The Nanoelec technological research institute is a consortium of private and public sector players, hold by CEA. Our mission is to help companies create value and enable their products to stand out on the digital transition stage. Nanoelec contributes to the competitiveness of the electronics sector, especially in France. It is based in Grenoble, a world-class hub for research, innovation and production in this field.

Our R&D programs are built jointly by representatives from the academic and industrial worlds.

"Working together to carry out responsible research and development programs to help businesses create value."

They deal with the design and development of new processes, systems and components in the following fields:
> photons & imaging: photonic sensors, new-generation displays and smart image sensors,
> digital trust: cybersecurity for connected objects, and characterization of components and systems by means of large instruments.

The Nanoelec IRT also runs training engineering and technological dissemination programs for SMEs with the support of the Auvergne Rhone-Alpes region. We implement open innovation techniques as well as more conventional technological development methods.

Given the pervasive nature of digital technologies, Nanoelec is in contact with actors from all sectors ranging from goods to services, industry, infrastructures, and consumer products, not forgetting transportation, environment and health. Nanoelec is a member of FIT, the hub gathering the technological research institutes (IRT) and energy transition institutes (ITE) set up by the French Government and financed by the Investments for the Future program (PIA). The network of institutes was created to pool academic and industrial players to run collaborative R&D and innovation projects aimed at boosting the competitiveness of the French economy. ◆

Anticipating future human and technological needs

Microelectronics innovation

- Carry out world-class collaborative R&D in tree domains to enable innovative components and embedded systems: image & photons, energy conversion and digital trust
- Develop and transfer these technologies to create the electronic circuits of the future
- Give industry players access to development, prototyping and advanced characterization resources

Technology dissemination

- Help businesses in the field of information and communication technologies meet the challenges of IoT through digital trust and security
- Provide expertise to help SMEs from various industrial sectors build new products and services with innovative components and embedded software
- Promote cooperation between SMEs, mid-caps and large companies
- Focus on collaborative innovation to unveil new applications comprising environmental and social impact assessments

Development of human capital

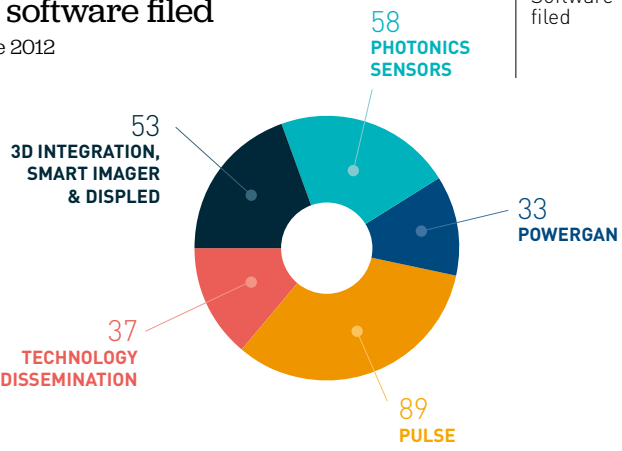
- Attract young people to jobs in electronics that contribute to sustainable development
- Work with all partners on parity and professional equality
- Design training courses to meet current needs
- Anticipate future skills requirements in the sector: sustainability, cross-skills, communities for social and sustainable innovation

KEY FIGURES OF THE INSTITUTE

DECEMBER 2021

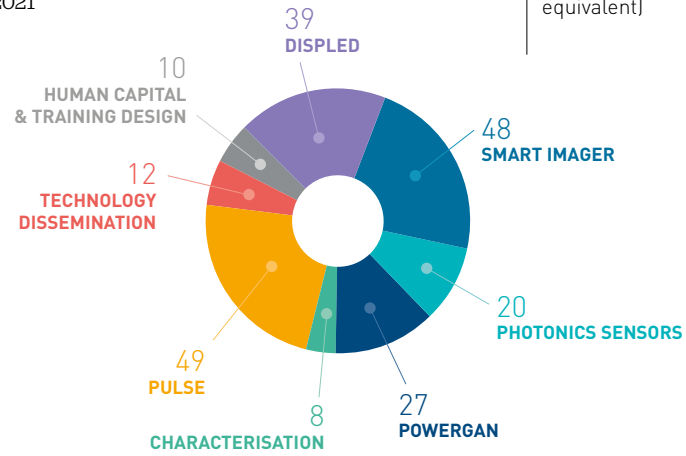
224 patents &
46 software filed
since 2012

Patents & Software filed



213 Full Time jobs
37% in private companies
in 2021

Human resources at the institute (in full-time equivalent)



A consortium of **public & private** members*

€54M average annual budget

295 associated partners including 218 SMEs
since 2012

544 scientific or technical publications & communications
since 2015

** 22 partners as of Dec. 2021*

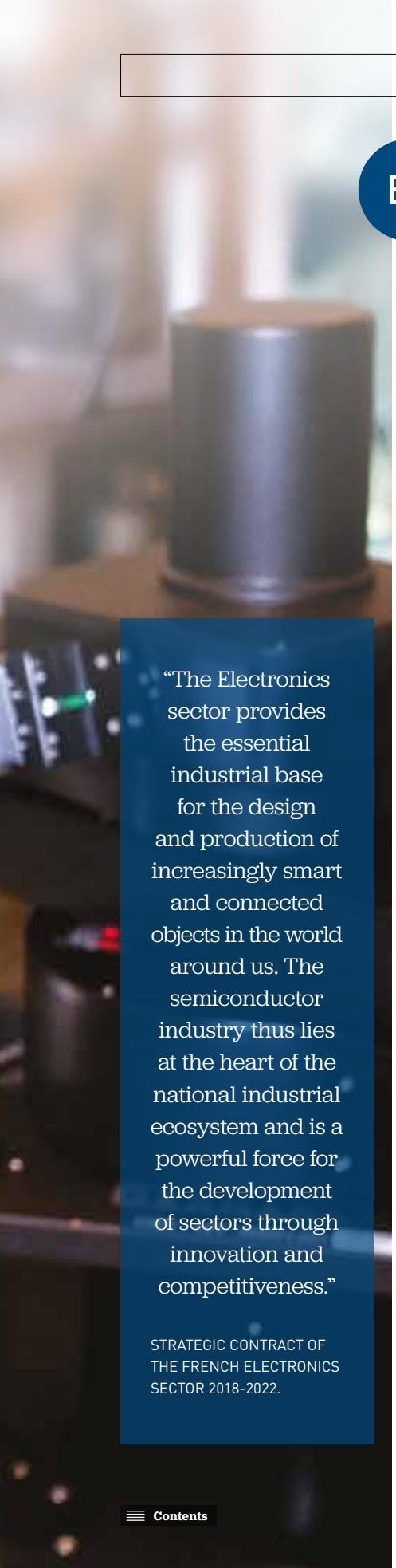
"Anticipating future human and technical needs in electronics"

Analysis zone, clean rooms at CEA-Leti
© Aubert/CEA

SEMICONDUCTOR RECOGNIZED AS A STRATEGIC SECTOR

"The IRT renewed its convention with the Public Authorities last year as well as its consortium agreement with twenty or so partners."

EVGroup Gemini equipment.
EVG is a Nanoelec partner.



"The Electronics sector provides the essential industrial base for the design and production of increasingly smart and connected objects in the world around us. The semiconductor industry thus lies at the heart of the national industrial ecosystem and is a powerful force for the development of sectors through innovation and competitiveness."

STRATEGIC CONTRACT OF THE FRENCH ELECTRONICS SECTOR 2018-2022.

BY

HUGHES METRAS,
DIRECTOR OF THE IRT NANOELEC TECHNOLOGICAL RESEARCH INSTITUTE

© P.Jayet/CEA

2020 and 2021 revealed the importance of electronics in the development of society. This was confirmed with a number of announcements concerning significant developments of industrial capacity, in particular in the Grenoble area, on the STMicroelectronics, Soitec and Aledia sites. In a context that was already tense owing to the Covid epidemic and now made worse by the geopolitical crisis at the gates of Europe, there is no doubt that competitiveness and sovereignty issues will be priorities. By virtue of its mission, the Nanoelec institute will continue to contribute to the dynamism of the electronics sector in France and Europe.

In 2021, Nanoelec launched the first phase of projects implementing the roadmaps set out for the period running from January 2021 to June 2025. This launch was accompanied by the extension of the contractual framework. The amendment to the consortium agreement was signed in the summer and all agreements with each partner were renewed before the end of the year. As a result, IRT Nanoelec benefits from a steady contractual framework for the coming years.
The programs are led by a dedicated team of program directors, who immediately grasped the challenges for the consortium and built a multi-partner dynamic framework within each program. Two new partners joined the IRT in 2021: Diabeloop - a start-up specializing in out-patient treatment of diabetes - participates to the Pulse program to work on security for artificial intelligence, a technology at the heart of the system it is developing, while Iroc Technologies - a company specializing in electronic circuit testing - joined the Characterization program.

In response to the Government's recommendations, we are carrying out four initiatives in line with the UN's sustainable development goals: we evaluated eco-innovation diagnostic methods to bring guidance to SMEs for the Easytech projects; in partnership with Aledia, we initiated the development of an eco-design tool in R&D phase for the Displed program; within the CHIF program, with the support of STMicroelecronics, we amplified our involvement in designing educational modules addressing environmental and societal challenges in the electronics industry. We also activated the Nanoelec ecosystem, to raise awareness of professional parity and equality issues.

Finally, the impact of Easytech projects was assessed thanks to the participation of 60 companies that have been supported by Nanoelec over the past 10 years. ◆

Three questions for Sébastien Dauvé, the new Nanoelec President

On July 1st 2021, Sébastien Dauvé was appointed as CEO of CEA-Leti. He took over from Emmanuel Sabonnadière, who was named head of the silicon carbide program at Soitec. Sébastien Dauvé is now President of IRT Nanoelec steering committee.

© Christian Morel/CEA

SÉBASTIEN DAUVÉ,
DIRECTOR OF CEA-LETI AND PRESIDENT OF THE STEERING COMMITTEE OF NANOELEC

IN 2021, NANOELEC RENEWED ITS CONTRACT WITH THE FRENCH GOVERNMENT. WHAT DO YOU BELIEVE ARE NANOELEC'S STRENGTHS AS AN INSTITUTE THAT DRIVES COMPETITIVENESS IN THE ELECTRONICS INDUSTRY?

More than ever, the microelectronics industry is crucial for European and French sovereignty. Nanoelec is an invaluable asset in such a context. The institute is home to internationally renowned industrial firms that are willing to work together as one, thereby strengthening their research and industrialization capabilities. Nanoelec's industrial entities work at different levels along the value chain, share common roadmaps and employ academics who strive for scientific excellence. For example, IRT Nanoelec has developed 3D technologies that are essential for the future of electronics, enabling devices that address both advanced scaling and heterogeneous integration road maps. Nanoelec benefits from a robust technological know-how, world-class equipment manufacturers specialized in chip-to-wafer or wafer-to-wafer assembly, architecture specialists and finally component manufacturers addressing a diversity of markets. Furthermore, thanks to our SystemLab initiative, we will be able to combine our assets and understand emerging markets for our industrial players.

IPCC (GIEC) SCIENTISTS HAVE ISSUED NEW WARNINGS REGARDING CLIMATE CHANGE. WHAT CAN THE ELECTRONIC INDUSTRY DO TO PRESERVE THE ENVIRONMENT?

At CEA-Leti and at Nanoelec, it is no longer possible to ignore the issue. This is a major concern for industrial firms and research teams. We must strive for a more sustainable industry and promote "frugal" electronics. This term encompasses numerous areas of innovation that, I hope, will help reduce our greenhouse gas emissions and our dependence on rare earth minerals. I also believe that this could generate a competitive edge. In addition, as a body backed by the Government, IRT Nanoelec's actions are part of a transition towards sustainability.

WHAT DO YOU CONSIDER TO BE THE SIGNIFICANT MILESTONES OF 2021?

Unlike purely bilateral collaborations, Nanoelec addresses collective issues and works with a group of industry players sharing interests at each step of a given value chain. Its goal is to prepare the ground for the emergence of new technologies that are useful and relevant to multiple stakeholders in the society and the industry.

In 2021, the commitments made by the partners confirmed their willingness to continue their common adventure within the IRT, by building roadmaps and projects in application areas of excellence for the Grenoble ecosystem (imaging and photons, digital trust, energy conversion).

The technical results are outstanding, with the validation of key milestones within the PowerGaN program, the first significant technological results on the Smart Imager and Displed programs, notably with an initial demonstration of the Smart Pixel concept. Nanoelec's capacity for innovation is confirmed by the significant number of patents and the diversity of publications accepted in leading conferences such as ISSCC and IEDM.

The original System Lab initiative has entered full deployment, with implementation of a multi-sensor image platform designed to explore a variety of use cases. This platform could act as the technical framework for proposed collaborations with the IRT and ITE network.

The institute's responsiveness and flexibility help industry players be increasingly competitive in the electronics industry. ◆

Highlights


© F. Legrand/CEA

• January 2021 •

BLOCKCHAIN AND DIGITAL IDENTIFICATION

A public comprehensive talk by Christine Hennebert (CEA-Leti) associated with the Nanoelec/Pulse program.


© P. Jayet/CEA

• February 2021 •

SUSTAINABLE ELECTRONICS

57 students from Grenoble-INP and GEM took part in a "Sustainable Electronics" workshop organized as part of the Nanoelec/Human Capital and Training Engineering (Chif) program, with an original serious game "My IOT" created by Nanoelec and Need for IOT (Idex UGA).


© pixabay.com

• March 2021 •

PARTNERS CONFIDENCE RENEWED

Industrial and academic partners of Nanoelec finalize the consortium agreement.

• March 2021 •

OPEN HARDWARE

Nanoelec strongly supports the Risc-V week attracting around 400 scientists from 33 countries.

© CEA

• March 2021 •

WOMAN ENGINEER

Severine Cheramy (Product line manager at Aledia) receives the "Engineer of the year 2021" award from the 3DinCites professional review dedicated to the international 3D architecture community.


A. Alix/CEA

AACSB
Business Education.
Connected.

• April 2021 •

DIGITAL TRAINING TRANSITION

Grenoble Ecole de Management (GEM) "Back to school 2020 challenge", designed with Nanoelec, is praised for its positive societal impact by AACSB within the framework of the annual challenge "Innovations that inspire".

Highlights

© P. Jayet/CEA

• May 2021 •

DISPLAY EXPERTISE

The Fellow Award of the Society For Information Display goes to François Templier, director of the Nanoelec/Displed program.

• May 2021 •

WHITE PAPER

A 100-page report on blockchain for personal identity privacy is published by the French Interior Ministry, Thales and Nanoelec, with CEA.

• May 2021 •

SMEs

Nanoelec/Technology dissemination program takes part in Minalogic Business Meetings 21.

• June 2021 •

IOT SECURITY

Digifed Generic Experiment Community on cybersecurity is kicked-off with sixteen French and European SMEs interested in strengthening the security of their embedded applications for the Internet of Things (IoT).

• July 2021 •

SERIOUS GAME FOR SUSTAINABLE ELECTRONICS

Grenoble-Ecole de management presented a professional webinar on "My IOT" a learning./training tool produced by the UGA Idex "Need for IOT" and Nanoelec.

• July 2021 •

REALITY OF SUSTAINABLE ELECTRONICS

A public webinar and round table "Micro-électronique responsable : quelles réalités ?" with Grenoble INP and GEM within Nanoelec CHIF program.

• June 2021 •

GENDER MATTERS

Nanoelec and Giant Campus organize a special public event on June 23th, the International Women in Engineering Day.

• **October 2021** •

SCIENCE FESTIVAL

10/7-8

Short public webinars for science popularization on “A green smartphone” and “Digital trust”, with Giant Campus, in the frame of the national Fête de la science program.

10/12

CEA/Y.Spot presented a professional webinar “Use cases for innovating” (by Céline Verchère, formerly at Nanoelec/Pulse program).

10/21

Professional webinar “Limatech: a startup for batteries”.

• **September 2021** •

NEW COMERS AT NANOELEC

The startup Diabeloop joins Nanoelec consortium on securisation of embeded AI for health application on diabetes.

The SME Iroc Technologies joins Nanoelec consortium to take part in the setting up of the Center for expertise in radiations effects on electronics components and devices.

• **November 2021** •

SIDO FAIR

System Lab platform was presented for the very first time in a professional trade fair in Paris (Sido, Paris).

Highlights

• November 2021 •

GIANT HIGH LEVEL FORUM

Keynote & booth with three startups from Nanoelec: Cocoon Care, ISKN/AMI et Kentyou.

• November 2021 •

CYBER HACKING

11/10-14

The 2021 edition of CSAW, the largest international academic cybersecurity competition, was held from November 10 to 14, 2021. The European edition was organized by Grenoble-INP / Esisar and the LCIS laboratory, with the support of Valence Romans Agglo and IRT Nanoelec. It brought together 104 finalist students representing 35 European universities from 10 different countries.

11/18

At the Festival Transfo festival/French Tech In the Alps, Nanoelec produced a round Table “Sustainable development as a new trend for innovation?”

• November 2021 •

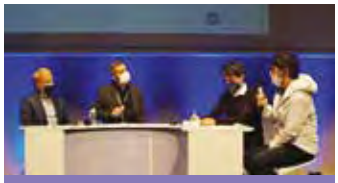
SILVER ECONOMY

Nanoelec was partner of the local authorities for a one-day professional seminar on Silver Economy.

• November 2021 •

HIGH PERFORMANCE IMAGING

Dedicated to imaging techniques, the 8th edition of Carac has been held November 30, 2021.
The attendees had the opportunity to take part in a set of practice workshops focused on selected high performance techniques(tomography, chemical mapping, high-resolution topography and morphology...).



• November 2021 •

GENERALY ASSEMBLY

Nanoelec 2021 general assembly focused on issues shared between R&D and society,
by gathering on thematic round tables experts from human sciences with our scientists.

• January 2022 •

SUSTAINABLE ELECTRONICS FOR SMART BUILDINGS

A immersive 2-days wokshop gathering students from business school and engeneering with industrial experts organized by Nanoelec/ Human capital & training design program.

• February 2022 •

EQUALITY & PARITY

Nanoelec became member of two association: Parité Science in Grenoble and Women in Engineering.

• March 2022 •

EDUCATION & TRAINING

Webinar for overview presentation of the training offer of Captronic, a core partner of Nanoelec.

CAP'TRONIC

Highlights

• March 2022 •

WOMEN AT ENGENEERING

For the 10 years of the institute, launch of the contest "Nanoelec award 2022 for women in technological research", at the occasion of the International day for Women Rights.

• March 2022 •

DESIGN AND ARCHITECTURE

At the international DATE conference, Nanoelec broadcast online a one-day event consisted of a plenary keynote, guest speakers, and regular presentations from CEA, Qualcomm, Georgia Tech, Stanford University, ETHZ (Switzerland), Fraunhofer Institute, University of Seville, Prophesee, STMicroelectronics, NTU (Singapore), Boston Univ., Univ. of Manchester, Stony Brook Univ., Notre Dame Univ, META Group (Facebook), Siemens EDA, Intel.

• April 2022 •

SYSTEM LAB FOR SMART BUILDING

A session for SMEs, ETIs and innovative startups in the Auvergne Rhône-Alpes region: presentation of System Lab, an open platform for exploring new scenarios for using multispectral optical sensors.


© P. Jayet/CEA

• May 2022 •

EFFECTS OF RADIATIONS

Grad[Next], workshop on radiation facilities nd testing of semiconductor devices & system for industry is organized by Nanoelec, Cern, ILL, ESRF, Iroc Technology, CNRS/LPSC, Radsag & Radecs.

• May 2022 •

OPEN HARDWARE

Annual Risc-V week in Paris, with Nanoelec.

• May 2022 •

A FRENCH AMBITION FOR NEXT GENERATIONS OF DISPLAYS

Nanoelec/Dispeld program presented in a public conference by CEA and Aledia experts.

• June 2022 •

PARITY FOR SCIENCE

Exhibition “Science size XX elles” from Parité Science is presented at Nanoelec and CEA-Leti.

© Vincent Moncorgé Photothèque CNRS Association Femmes & Sciences

• May 2022 •

POWERGAN

National symposium for the conclusion of the Nanoelec/ powergan dedicated to the electrical power conversion with GaN Material, by Nanoelec, ITE Vedecom & IRT Saint Exupéry.

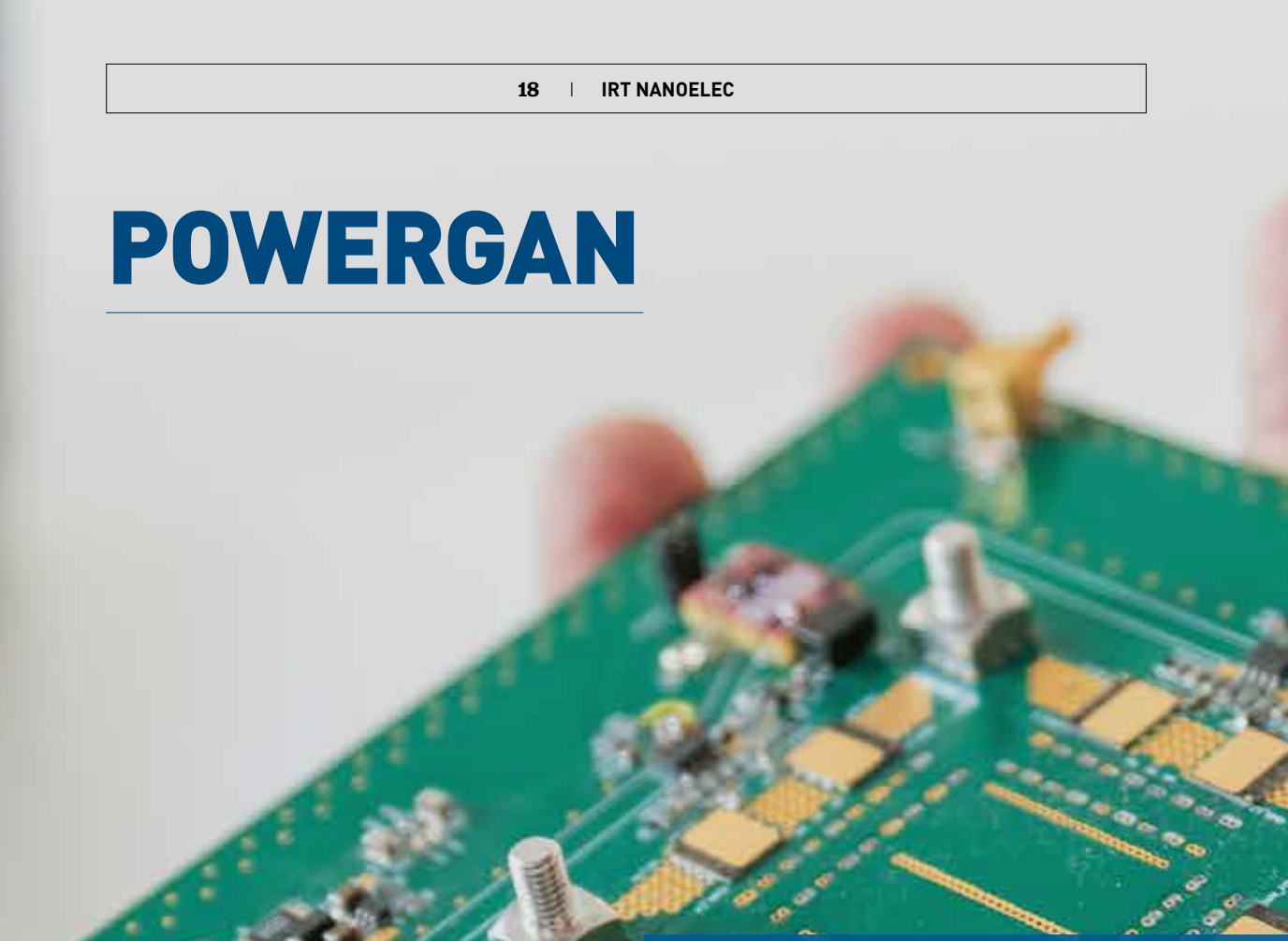
• June 2022 •

NANOELEC AWARDS FOR WOMEN IN TECHNOLOGICAL RESEARCH

Pitch of the 14 candidates for “Nanoelec Award 2022 for women in technological research”, with Giant Campus and GEM, at the occasion of the International Day for Women in Engineering.

© P.Michallon/CEA Femmes & Sciences

POWERGAN



Powergan program at a glance

VISION
Support and accelerate the development of a new generation of power components to address digital and energy transition challenges

AMBITION
Contribute to the structuring of the national GaN value chain with a research strategy based on disruptive GaN/Si power devices using 200mm technology and GaN enabled power converter co-design tools and techniques

MISSION
Prepare 650V transistor technology transfer to STMicroelectronics and establish proof of concept for a PowerGan Digital Twin

PARTNERS
CEA
Grenoble-INP
Siemens EDA
Schneider Electric
STMicroelectronics

BY

RAPHAEL SALOT,
DIRECTOR OF THE NANOELEC/POWERGAN PROGRAM AND KEY ACCOUNT MANAGER AT CEA-LETI

© P. Jayet/CEA

From smartphones to kitchen appliances and e-vehicles, electric current and voltage must both be processed and controlled with the help of a converter to supply the optimal energy required by each specific device.
Power conversion, however, leads to energy loss. Gallium nitride (GaN) and other wide-bandgap materials can substantially reduce this loss. Until recently, these technologies were too costly to use in power conversion applications. But driven by the aeronautics and automotive industries in their quest for highly compact and efficient power converters at low cost, R&D centers are now pioneering new GaN techniques.

The aim of the Nanoelec/PowerGaN program has been to strengthen and structure a national industrial and academic ecosystem to help stakeholders from French and European industry gain a foothold in a variety of sectors, ranging from personal electronic equipment to electrification of private and mass transport. Teams brought together through the program have contributed to the development of GaN-on-silicon (GaN/Si) technologies in order to overcome the technical and economic limitations of existing power-component technologies available for the 100-650V segment. The program ran from 2017 to 2021 and enabled the development of a disruptive technology using 200 mm wafers compatible with mass production. This technology is at the heart of the GaN/Si pilot line that STMicroelectronics is implementing in its factory in Tours, France. We improved the performance and reliability of a first generation of 650V components and prepared for the next generations. In order to further drive the miniaturization of systems, we also worked on architectures of disruptive converters. We developed tools and methods to co-design component and system architectures and to accelerate technological adoption, especially for harsh environments such as automotive applications.

GaN power devices may be just around the corner. However, this achievement requires a greater R&D effort. Each architecture has its own potential, depending on the application targeted. Academic and industrial teams brought together within Nanoelec have been exploring various architectures in order to address the great need for efficiency at low cost, and, perhaps more importantly, the need for greener power electronics.

To conclude the program, we assessed the widely shared interest in GaN material for power conversion: we brought together close to 200 experts from both industry and academia at a symposium in Paris in March 2022. The main scientific contributions of the program were discussed at round tables and via keynotes from Renault, STMicroelectronics and Yole Development. The event was organized with our colleagues from IRT Saint Exupéry and ITE Vedecom. ◆

POWERGAN

The community comes together

To conclude the Nanoelec/PowerGaN program, close to 200 experts from both industry and academia got together at a symposium in Paris in March 2022 (and on-line) organized with IRT Saint Exupéry and ITE Vedecom.

The main scientific contributions of the program were discussed at round tables and via keynotes from Renault, STMicroelectronics and Yole Development. The event also featured important contributions from Vitesco Technologies, Airbus Defence and Space, Schneider Electric, Safran, Elvia, Siemens EDA, G2ELab (Grenoble-INP, CNRS, Université Grenoble-Alpes) and CNRS-Laas.

On this occasion, Jean-Philippe Mercier, HEV System & e-motor Expert Leader at Renault Group, explained what end-users like Renault Group or equipment manufacturers may expect from GaN components: to develop and increase standardization of components and their packaging, to increase customer value and facilitate outstanding characteristics exploitation, to enhance current and voltage capability (up to 1200 V). For Filippo Di Giovanni, Strategic Marketing, Innovation and Key Programs Manager at STMicroelectronics, *"Wide-bandgap sem conductors meet the requirements of the decarbonized economy and those of the energy transition to systematically improve conversion efficiency."* Recalling that STMicroelectronics is pursuing a global strategy on wide-bandgap products, in particular to consolidate its presence on the electric car market thanks to SiC components (MOSFETs), he underlines that his group supplements this approach with a complete roadmap for GaN and participation in collaborative projects. *"The GaN industry can now draw on an ecosystem of industrial skills and advanced research"*, he concludes. ◆

"Wide-bandgap semiconductors meet the requirements of the decarbonized economy and those of the energy transition to systematically improve conversion efficiency."

POWERGAN

A 100W AC/DC converter

A new generation of components has been designed. It incorporates a new control method which relies on local detection of the operating quadrant and needs no ultra-fast critical measurement. Simulation results with detailed modelling of the circuits offer very good efficiency prospects.

The action taken aimed to overcome the obstacles to the 100W USB Power Delivery application. It requires that a 100W AC-DC power converter be integrated into the authorized volume of a wall power outlet, while meeting the standards for isolation and radiated and conducted harmonic pollution generated by the system on the grid.

In 2019, a first generation of 100W AC-DC converters using Dual Active Bridge architecture was designed and built around high-speed analog electronics with impedance matching stages. *"Its inherent advantages are to do away with the multiple conversion stages which limit the efficiency and miniaturization of the converter"*, reports Leo Sterna, research engineer at CEA-Leti.

Tests on a demonstrator show that the ZVS (zero volt switching) driver circuit was significantly improved by comparison with the previous work. The proposed solution allows operation at 1 MHz with considerable dynamic ranges. An experimental implementation on a converter cell validated the solution with efficiency levels obtained (losses for 100 W) of 98%.

"Efficiency performance at 1 MHz is good but nonetheless insufficient for the final application", notes Leo Sterna. *"That's why we studied a new control approach for a second-generation demonstrator which does not create any control complexity for the user. This control method is based on local detection of the operating quadrant and requires no ultra-fast critical measurement."* It can be implemented with low-cost analog and digital circuits and has the advantage of offering extensive integration (possible IC). *"Then, we validated the working of the proposed control by a SPICE simulation with detailed modelling of the circuits. The simulation results indicate extremely good efficiency prospects"*, Leo Sterna adds. ◆

"Efficiency performance at 1 MHz is good but nonetheless insufficient for the final application"

POWERGAN

Measurement of heat flux in the component

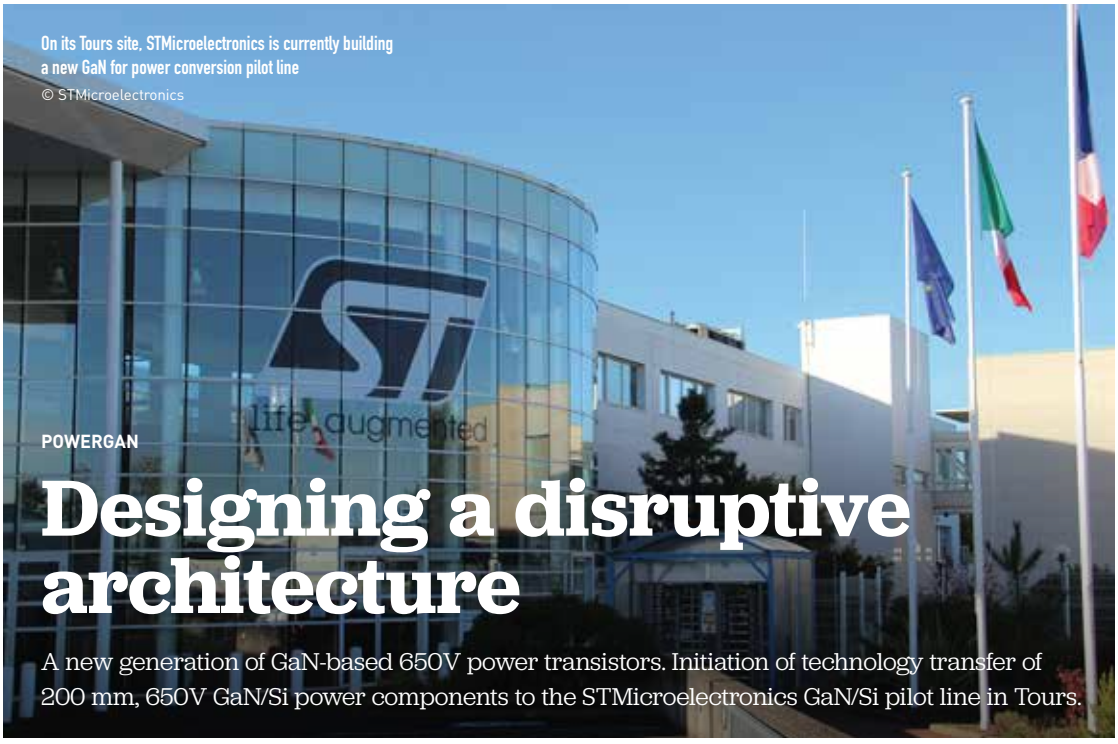
Proofs of concept for functions that can be integrated onto a chip with a view to developing new components capable of contributing to large-scale adoption of GaN technology by the market. CEA researchers developed a heat flux sensor that prevents degradation of the component.

When using a power transistor, its operating state must be known, more particularly its temperature, so that it can be limited, to avoid degrading the characteristics. Operation at too high a temperature leads to an increase in heat losses which can result in reduced performance or even a shortened component lifetime. Managing the thermal parameter generally entails using a temperature sensor which is usually added to the transistor package or, more recently, integrated directly on the same chip.

"The approach being studied at Nanoelec/PowerGaN is not based on the use of temperature sensors, but rather on heat flux sensors", underlines René Escoffier, leader of the study at CEA-Leti. The principle of these sensors is not to measure a single temperature, but two temperatures at different distances on the heating part. This sensor (called a thermoelectric sensor) is based on the Seebeck effect, which can generate a voltage in a circuit made up of two electrically connected materials that conduct differently, for which the connections are kept at different temperatures. This original solution enables a flux sensor to be integrated, using only the basic building blocks of HEMT transistor manufacturing, with no extra processes being added.

"The approach being studied at Nanoelec/PowerGaN is not based on the use of temperature sensors, but rather on heat flux sensors."

"We produced three sensor geometries in order to study the impact of their shape and position as compared with a central heating element, here consisting of a 10A rating HEMT transistor", Escoffier reports. *"The results show very good sensitivity of the sensors to the heat flux. The sensors' response is between a few millivolts and several tens of millivolts for a power of only 2 Watts (in the heating element). We also noticed that the sensitivity of these sensors increases as the ambient temperature rises. This is an extremely interesting property for the high-temperature operation of wide-bandgap power components (such as GaN transistors)."* ◆



On its Tours site, STMicroelectronics is currently building a new GaN for power conversion pilot line
© STMicroelectronics

POWERGAN

Designing a disruptive architecture

A new generation of GaN-based 650V power transistors. Initiation of technology transfer of 200 mm, 650V GaN/Si power components to the STMicroelectronics GaN/Si pilot line in Tours.

The Nanoelec/PowerGaN program focuses on the development of a radically innovative architecture for an enhanced GaN transistor with insulated gate (known as Recessed Gate MIS). This technology notably enables the transistors to function in "Normally off" (Noff) mode, with low current leakage from the gate, and lesser degradation of the Ron (conduction resistance leading to performance losses) at higher temperature than the competing solutions. It is thus the ideal response to the needs of the designers, but requires numerous technological obstacles to be overcome, in particular in terms of its gate (stability of electrical characteristics, reliability).

In addition to the technological developments needed to optimize the various blocks and validate a complete manufacturing process, different characterization and analysis methods have been implemented in order to model the working of the transistors and test a number of architecture variants.

The performance model must be linked to the geometrical and physical parameters of the component (in particular electron gas resistance, contact resistance, mobility in the channel, etc.). *"We characterized various geometries, in order to extract the associated overall Ron (conduction resistance leading to performance losses), to evaluate the impact on the threshold voltage and to decorrelate the various contributions"*, says Romain Gwoziecki (CEA-Leti), who led the study with colleagues at STMicroelectronics. *"The impact of the geometries on the blocking voltage withstand capability was also evaluated, notably in order to define the accessible dimension limits. The main architecture-related compromise is that of Ron / BV (Breakdown Voltage), both of which drop as the gate/drain length (Lgd) is shortened"*, he adds.

> "The impact of the geometries on the blocking voltage withstand capability was also evaluated."

The second key parameter identified was the length of the channel, which in principle has no impact on the voltage withstand capability, but a significant one on the Ron.

Finally, these measurements were able to define a performance model for the Ron which acted as the basis for the generation of a new test vehicle designed for improved performance.

"This work paves the way for technology transfer with a view to industrial implementation on our French site in Tours," concludes Stéphane Martinez, Director of the STMicroelectronics Tour site. ◆

POWERGAN

Reducing electromagnetic interference

On a PCB demonstrator, with packaged chips, a team from G2ELAb (Univ. Grenoble-Alpes, CNRS, Grenoble-INP) established, validated and constructed the principle of a "sandwich" type 3D layout for lateral GaN components. A concept with shielding by the continuous bus between the semiconductors' floating point and the reference potential (heatsinks) was used and confirmed a reduction in electromagnetic interference. Digital simulation was then used.

Frequencies ranging from 100 Hz to 2 kHz traditionally refer to the notion of active filtering of harmonics. This entails measuring the network harmonics and reinjecting them in phase opposition onto the line to eliminate them. GaN HEMT components offer the possibility of fast switching at several MHz with acceptable efficiency. They enable the concept to be widely used to reduce disturbances in the frequency ranges usually covered by passive filtering. *"It is thus possible to envision compensating conducted emissions in the frequency band ranging from 10 kHz to several hundred kHz. We set ourselves a target of about 500 kHz at the beginning of this study, to be confirmed subsequently. As a result we hope to significantly reduce the passive filtering effort and therefore the volume of components needed"*, explains Jean-Luc Schanen for the G2ELAb (Univ. Grenoble-Alpes, CNRS; Grenoble-INP) who, within Nanoelec, directed a study for a disruptive concept to reduce electromagnetic interference on GaN components for power conversion. *However, rapid switching at frequencies this high and with semiconductors such as GaN demands particular precautions to control the disturbances emitted beyond the quench frequency (from a few MHz to several tens of MHz), failing which, the filtering gain on the 10kHz-500kHz part would be cancelled out by that needed for the high frequency part."*

Jean-Luc Schanen and his team validated the principle of a "sandwich" type 3D layout for the lateral GaN components and constructed a PCB demonstrator, with packaged chips.

> Jean-Luc Schanen and his team validated the principle of a "sandwich" type 3D layout for the lateral GaN components.

"Using simulations performed with tools in the Siemens EDA suite, we carried out a detailed analysis of the experimental results obtained on a reference board (without shielding) and on a board with a shielding layer limiting the common mode, Schanen reports. *The different origins of the electromagnetic disturbances were thus brought to light: obviously considerable impact by the power traces, but also a non-negligible impact from the semiconductor package, on which the face connecting to the heatsink is connected to the GaN component source, as is the driver of the "Top" component."* The gradual application of shielding has produced interesting results regarding the respective contributions of the 3 common mode origins and highlighted significant gains by shielding the 3 contributors. The methodology is thus perfectly well-known and has been validated, first of all through simulation and then physically. ◆

At G2ELab, Pawel Derkacz, PhD student (UGA and Gdansk University, Poland) developed an electromagnetic interference measurement bench for Nanoelec/PowerGaN power boards

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POWERGAN

Digital twin for GaN

A homogeneous design flow using Siemens EDA software tools was validated by means of different power boards which made it possible for each one to focus on specific elements: compact model, electromagnetic interference, embedded PCB, complex board.

Gallium Nitride (GaN) type Wide Bandgap (WBG) components have been emerging on the power market in recent years, for high frequency applications (>>100 kHz) in order to increase the power density of converters. But they are also finding their place in lower frequency applications (<100 kHz) for high-efficiency converters. These two fields of application make maximum use of the performance of GaN components, notably low on-state resistance and switching performance that is today unparalleled.

The integration of GaN type WBG components demands particular attention, notably discrete component integration on PCB. The high transition speeds of these components expand the frequency ranges which had not yet been explored with slower components using classic Silicon (Si) technology. The parasitic elements induced by the PCB, which are not an issue with Si technologies, become problematical for operation of GaN components. Their integration has to be optimized, notably minimization of the switching loop inductances, optimization of the placement of the decoupling capacitors, the hot point-cold point capacitive couplings, etc.

In 2020, Siemens EDA (ex. Mentor Graphics) joined the Nanoelec/PowerGaN program. *"We brought to the program the capacity to build a Digital Twin of GaN power converters, enabling system and technology co-optimization, testing of accuracy against measurements and use throughout its full lifecycle, as well as preparing for a response to the acceleration of the market"*, underlines Jean-Marc Talbot, Senior Director Solutions & Strategic Partnerships at Siemens EDA.

On the one hand, a DUT1 "design under test 1" integrates CEA-Leti 650V/30A components on a simple half-bridge in different formats; TO247-3L-based packaging and a design based on bare die components with glob top. The designs were imported into HyperLynx Siemens EDA in order to extract the parasitic elements from the PCB. Using the equivalent PCB models generated, the circuit diagram can be constructed with Xpedition Designer in order to associate the PCB models with their connections to the passive and active components.

"Once the diagram is complete, frequency, static and time-domain analysis can be carried out to stu-

One of the scientific and technological challenges of the Nanoelec/PowerGan program centered on the modelling of power components (via the 650V transistor compact model study). The digital twin concept consists in replicating a physical system in a digital model. This type of approach was developed by Nanoelec for GaN power components and it will allow co-optimization of the system and the technology and drive them to the performance limits.
© P. Jayet/CEA

dy the behavior of the circuit, including the parasitic PCB and components, explains Charley Lanneluc (CEA-Leti) who worked in close connection with teams from G2ELab (Grenoble-INP, CNRS, Université Grenoble-Alpes). *All the results, whether PCB parasitic elements and time-domain waveforms were compared with the experimental results and showed a good degree of coherence."*

On the other hand, a DUT2 integrates off-the-shelf 650V/30A GaN components from the GaNSystem company into a classic half-bridge with capacitive mid-point. This DUT2 was integrated on a bench standardized for electromagnetic compatibility (EMC) tests, notably to measure the conducted common mode noise level generated by the GaN components. *"As with the DUT1, we integrated this design into HyperLynx to extract the PCB parasitic elements, as well as into Xpedition Designer, to create the schematic around the PCB, but also around the EMC bench (RSIL, probes, common mode inductances, etc.). We then meticulously characterized each component to take account of these imperfections, so that simulation of the discrete elements would be as realistic as possible. The theoretical common mode noise obtained from simulation is consistent with the simulation results, notably with regard to the amplitudes and the transition frequencies"*, adds Charley Lanneluc.

> "Once the diagram is complete, frequency, static and time-domain analysis can be carried out to study the behavior of the circuit, including the parasitic PCB and components."

The quality of the digital model results, in particular with the Siemens EDA suite, is encouraging. *"There are still some differences between the laboratory demonstrators and their digital twins, although the trends, the amplitudes, the frequencies, etc., are in line with the experimental results on the two DUTs in question"*, concludes Jean-Marc Talbot. ◆

POWERGAN

Our customers are increasingly attentive to the hidden cost of power losses

For Miao-Xin Wang, Director of the Schneider Electric power conversion research center in Grenoble, GaN and SiC will lead to gains in power density and energy efficiency.

© Wang

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MIAO-XIN WANG, DIRECTOR OF THE SCHNEIDER ELECTRIC POWER CONVERSION RESEARCH CENTER.

WHAT DID SCHNEIDER ELECTRIC GAIN FROM ITS PARTICIPATION IN THE POWERGAN PROGRAM?

For us, this program was an opportunity to develop methods and evaluate modelling and co-simulation tools for converters containing GaN components. The approach enabled us to conduct an initial evaluation of the converter circuit before fabrication. We also identified and consolidated the fact that the availability of bidirectional GaN transistors, developed within Nanoelec, will lead to a significant gain for various topologies and applications in terms of efficiency and power density.

HOW WOULD YOU DESCRIBE THE POWER CONVERSION MARKETS ON WHICH YOU ARE ACTIVE?

We have sales of more than 3 billion euros with our power converters, out of the group's total sales of 29 billion euros. It is clear that introducing technologies enabling us to progress could lead to impressive market figures. Most of our equipment covers the IT farm power supply markets (UPS, data centers) and variable speed drives.

Thanks to GaN power conversion technologies, Schneider Electric is aiming to develop high-speed chargers for the IoT, for example to enable you to charge your mobile phones more rapidly.
© Schneider Electric

ON THESE MARKETS, WHAT CHALLENGES DO YOU THINK COULD BE MET USING NEW MATERIALS SUCH AS SIC OR GAN?

First of all, there are always savings to be made in terms of systems energy efficiency. This is important in the energy transition context, because our customers are increasingly attentive to the hidden cost of power losses.

We will also make gains on the cost and dimensions of converters. Within Nanoelec, Schneider Electric and CEA thus carried out a number of studies on GaN converters for USB-C type wall outlet charger applications: we demonstrated that GaN technology can reduce the size and up to 70% of the weight of USB adapters for smartphones and divide the charge time by a factor of 3. This demonstration will now have to be converted into a product, by proposing USB wall outlets for sale to private individuals and professionals.

> "Within Nanoelec, Schneider Electric and CEA thus carried out a number of studies on GaN converters for USB-C type wall outlet charger applications."

YOU ALSO STRESS THE IMPORTANCE OF DIGITAL TWINS, COVERED IN POWERGAN WITH SIEMENS EDA. WHY?

I'm convinced that integrating the methods developed by Nanoelec/Powergan, for modelling and co-simulation of converters containing GaN components, into the design phase will reduce the development cost and time for Schneider Electric conversion products, such as uninterruptible power supplies and variable speed drives.

IN YOUR OPINION, WHAT APPLICATIONS WILL STRUCTURE GAN POWER INNOVATIONS?

Today, we know that the development of new components will be driven to a large extent by automotive needs. We will be paying close attention to this, while remaining efficient and focused on stationary applications. ◆

- KEY PUBLICATIONS -

European Solid-State Device Research Conference (ESSDERC)

At the 21' European Solid-State Device Research Conference (ESSDERC) in Grenoble, two studies developed within Nanoelec were presented by teams from CEA, Université Grenoble-Alpes. The first one is an analysis of parasitic capacitance in a short channel MIS-HEMTS GaN component. *"Gate-to-channel coupling capacitance behavior on GaN-HEMT with recessed MIS-Gate was analyzed combining experimental data and 2D-simulations"*, says Romeo Kom Kammeugne (CEA-Leti) as the first author. The second study presents a reliable method for low field temperature dependent mobility extraction at the Al2O3/GaN interface.

ROM KOM KAMMEUGNE ET AL
PARASITIC CAPACITANCE ANALYSIS IN SHORT CHANNEL GAN MIS-HEMTS

BLÉDION RRUSTEMI & AL
RELIABLE METHOD FOR LOW FIELD TEMPERATURE DEPENDENT MOBILITY EXTRACTION AT AL203/GAN INTERFACE

Essderc/Esscirc, online | September 2021

Assessing the interfaces in heterostructures built with GaN

In a study conducted by a team from CEA-Leti and IMEP-LAHC (CNRS/Grenoble INP/UGA/Université SAVOIE Mont-Blanc), the gate-to-channel capacitance and the drain current behaviors were used to investigate interface charges in SiN/AlxGa1–xN/GaN heterostructures. *"This work brings clarity regarding the properties of the SiN/AlGaN interface. The models used can guide the optimization of HEMTs ON-state resistance as they allow easy parameter extraction from simple current and capacitance measurements"*, explains Bledion Rrustemi (PhD student at CEA-Leti) as first author of the related paper published in the Journal of Applied Physics.

BLEDION RRUSTEMI & AL.
INVESTIGATION ON INTERFACE CHARGES IN SIN/ALXGA1–XN/GAN HETEROSTRUCTURES BY ANALYZING THE GATE-TO-CHANNEL CAPACITANCE AND THE DRAIN CURRENT BEHAVIORS

Journal of Applied Physics | 2021

The impact of GaN surface treatment conditions on device performance

Al2O3/GaN interface properties have been studied using X-ray photoelectron spectroscopy (XPS). The results were published in ACS Applied Electronic Materials by a team from CEA-Leti, within Nanoelec. Different wet treatments, NH4OH, HCl, HF, and H2O2/H2SO4, were applied on etched and as-epi GaN samples prior to atomic layer deposition (ALD) of thin Al2O3. Higher Ga oxidation is observed for etched samples by comparison with as-epi samples, along with a shift of the Ga 3d peak position towards higher energies, probably related to GaN band-bending changes due to varying charge densities at the Al2O3/GaN interface.

LAURA VAUCHE & AL.
STUDY OF AN AL2O3/GAN INTERFACE FOR NORMALLY OFF MOS-CHANNEL HIGH-ELECTRON-MOBILITY TRANSISTORS USING XPS CHARACTERIZATION: *THE IMPACT OF WET SURFACE TREATMENT ON THRESHOLD VOLTAGE VTH*

ACS Applied Electronic Materials | February 2021

Underlying physical mechanisms in GaN-HEMT technology

Bias temperature instability (BTI) may severely affect transistor lifetime as well as the dynamic performance of a GaN component for power conversion. Researchers from CEA-Leti, STMicroelectronics, University of Padua (Italy) and IMEP-LAHC (CNRS/Grenoble INP/UGA/Université Savoie Mont-Blanc) investigated the underlying physical mechanisms leading to BTI degradations in GaN-based transistors. BTI instabilities are thoroughly explored under various gate voltage stresses on GaN-on-Si.

ABYGAËLE VIEY & AL.
INFLUENCE OF CARBON ON PBTI DEGRADATION IN GAN-ON-SI E-MODE MOSC-HEMT

IEEE Transactions on Electron Devices | April 2021

- KEY PUBLICATIONS -

Characterization of degradation mechanisms and electrical reliability study on GaN-on-Si power transistors

Electric vehicles and energy storage batteries have driven very significant growth in the market for medium power devices. Future generations of devices will need to support voltages in the 650V range and operate at high frequencies (>1 MHz). GaN-on-Si devices are currently considered the best candidates to meet these specifications. CEA-Leti is developing its own GaN-on-Si prototyping line, from the silicon wafer to the final power module. In this context, the devices developed at Leti and featuring a disruptive architecture based on a MOS gate have demonstrated excellent static and dynamic performance. However, the temporal degradation under stress as well as the failure mechanisms of the devices need to be further understood. The purpose of this thesis is to study the threshold voltage VTH instabilities of GaN-based transistors on silicon through advanced electrical characterization techniques initially dedicated to CMOS technologies. A part of the research work focused on identifying the defects causing VTH drifts, as well as on understanding the underlying physical mechanisms involved in these instabilities. Moreover, particular attention has been paid to the physical modeling of the observed phenomena. Finally, the influence of the gate architecture on the VTH variations was also investigated through the implementation of an innovative experimental setup. Although this work has contributed to the development of GaN-on-Si transistors at CEA-Leti, a clearer understanding of VTH instabilities is still required.

THESIS DEFENDED BY
ABYGAËL VIEY
at Université Grenoble-Alpes | November 2021

SMART IMAGER

From image sensors to embedded vision in Europe

Mastering smart imagers industrial process flow would be a competitive advantage for Nanoelec's industrial partners.

© Pixabay

Smart Imager program at a glance

VISION
The transition from imagers to vision sensors generates new market opportunities

AMBITION
To provide key hardware and software building blocks, to validate them through demonstrations ranging from test vehicles and proofs of concept to the prototyping of a smart multi-layer imager

MISSION
Stacking/3D technologies, embedded AI and data management, New architectures

PARTNERS
CEA
Lynred
Prophesee
Siemens EDA
STMicroelectronics
Grenoble-INP

BY

ERIC OLLIER,
PROJECT MANAGER AT CEA-LETI AND DIRECTOR OF NANOELEC/SMART IMAGERS PROGRAM

© P. Jayet/CEA

Launched in 2021, the Nanoelec/Smart Imager program is committed to providing relevant and real-time environment analysis by vision.

Our goal is to develop the technologies needed for the next generation of imagers. We will thus be able to move from generating images to exploiting the information they contain, even at the level of the sensor itself, in order to capture a scene, understand the situation and intervene. For the industry, this transition is a real disruption as well as a paradigm shift, with the problems of computing and memory becoming priorities, in addition to actual generation of the image. This revolution entails implementation of artificial intelligence within the actual image sensor. This is why we are working on both the components and the software. Apart from the fact of opening up new application fields, this new generation of smart imagers will offer obvious advantages in terms of data security, protection of privacy, low latency and low energy consumption.

The goal of the consortium is to develop 3D stacking technologies in order to implement artificial intelligence functions on the sensor itself.

Analysis of state-of-the-art 3D imagers confirms the technological choices made by the IRT's partners for image sensors. The integration possibilities are numerous and depend on the initial know-how of the actors and the final target market, but direct hybrid bonding is now the basis of the most advanced integrations, owing to its ability to achieve small interconnection pitches, and its versatility in allowing both wafer-to-wafer and chip-to-wafer integration, depending on requirements. This technology would also appear to be transferrable to 3-layer assembly, which is today the identified core of our work and for which there are many utilization prospects. To achieve this complex assembly, an additional crucial technology is being developed in the program: High-density TSV (Through Silicon Via) to ensure electrical continuity through the intermediate silicon substrate.

Finally, although initially developed for visible imagers, 3D technologies would also appear to be highly promising for other types of sensors, in particular infrared imagers and event-based sensors which are also considered in the program.

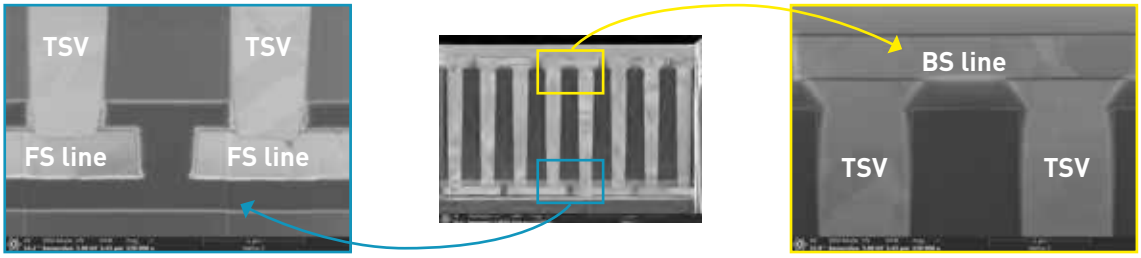
This technological work is also enriched by the development of simulation and design tools to allow the design of these complex 3D objects with a complete design stream, as well as in-depth examination of the most relevant architectures. ◆

SMART IMAGER

Development of the HD-TSV building block for smart imagers

Electrical interconnections

View of the high-density TSV (Through Silicon Via) produced in 2021 under the Nanoelec/Smart Imager program. TSV is a basic technological building block for 3D integration essential to the 3-layer stacking targeted by the program. It ensures electrical continuity through the intermediate silicon substrate. The electrical characterizations and reliability tests performed in 2021 gave good results. The process was optimized in terms of geometry control, alignment on the other levels and compatibility with the 3-layer stack (compatibility with hybrid bonding). In addition, a new equipment was identified and evaluated to enable high-precision thinning of the silicon layer through which the TSV are made, paving the way for thin HD TSV (5 then 3µm). ◆



© CEA

3D stacking

Demonstration of the 3-layer test vehicle has been started and is under way in the CEA clean rooms. It is based on the 3LHB masks set designed beforehand for IRT's 3D program. The aim is to demonstrate electrical continuity in a stack of 3 wafers 300 mm in diameter, thus validating the integration based on 2 hybrid bondings and 1 stage of TSV-HD. The first level of hybrid bonding went well and integration continued with the fabrication of the TSV and preparation of the second hybrid bonding. This manufacturing is a means of identifying and dealing with all the technological challenges posed by a stack of this complexity, as and when they occur.

300mm wafer integrating the two key technological bricks for 3D architecture: hybrid bonding and high density TSV

P. Jayet © CEA

AI software & architecture

"In 2021, we selected two AI applications (Motion Segmentation for the visible segment, and Motion Detection for infrared segment), and we proposed different AI architectures based on Mobilenet topology and trained these neural network architectures on different available data sets" explains Pascal Vivet (CEA-List), Deputy Director of the Smart Imager program. Our teams also explore a disruptive architecture for executing these neural networks within the Smart Imager.

The Retine technology, developed by CEA-List and CEA-Leti, acts as the basis for the study and optimization of a fine-grain SIMD distributed cluster type imager architecture, for different technological targets and pixel sizes. "The first explorations show that the architecture is viable for the visible spectrum using FD28 technology for small pixels (1 µm range), and for the infrared spectrum using C40 technology for larger pixels (10µm range)", states Pascal Vivet, indicating that in 2022, *"the architecture need to be further refined and compared with more standard solutions."* ◆

The Retine technology, developed by CEA-List and CEA-Leti, constitutes one of the basis for the study and optimization of an architecture for the future Nanoelec/Smart imager.

© CEA/Morel

SMART IMAGER

3D design flow

For the needs of the Smart Imager/Nanoelec program, the teams from CEA and Siemens EDA developed several circuit design methodologies and associated Process Design Kit (PDK) in 2021, specifically for 3D architectures. Jean-Marc Talbot tells us more (Siemens EDA).

CONCERNING 3D, WHAT POINTS ARE OF PARTICULAR INTEREST TO YOU?

Several aspects of 3D-IC design & verification methodologies and Siemens EDA tools usage, applied to Smart Imagers are addressed by this program. Thermal analysis for 2.5D/3D design has been a collaboration topic between Siemens EDA and CEA for years and have helped mature the SAHARA product, and new flows have been added in 2021, notably IR drop and electromigration analysis with mPower software, analog and mixed-signal with the new generation platform Symphony and more.

IN SMART IMAGER, YOU ARE TAKING PART IN IMPLEMENTING A COMPLETE 3D DESIGN FLOW. WHAT IS YOUR POSITION ON THIS?

We are developing the corresponding tools to cover the entire design flow, from the high level (architecture) down to the low, technological level, in order to be able to design highly complex systems and real applications demonstrators.

More specifically a methodology allowing fast exploration of AI accelerator hardware engines has been validated. It is based on the coupling of two tools : a high level tool for AI modelling and learning (N2D2 tool from CEA) and high level synthesis (Catapult from Siemens EDA). In addition digital implementation methodology for 2.5D/3D using Aprisa platform has been initiated in 2021 for further joint work with CEA in 2022.

HOW DOES THE MULTI-PARTNER ENVIRONMENT AT NANOELEC ENABLES YOU TO REINFORCE YOUR OFFERING WITH REGARD TO DESIGN TOOLS?

In 2021 we made significant progress on design & verification methodologies for the design of the future 3D imager at Nanoelec covering all aspects of the design. The collaboration with CEA and other partners is based on the deployment of commercial tools for this category of applications as well as research and maturation of new tools

In addition to the existing tools already developed in the previous 3D program (such as CALIBRE 3DSTACK for the Inter-Die DRC (Design Rule Check) and LVS (Layout Versus Schematic), Siemens EDA supplies the IRT Nanoelec partners with a comprehensive set of design and verification tools so that they can address the challenges linked to imaging and photons. ◆

SMART IMAGER

Lam Research

The project associating the American company Lam Research with Nanoelec aims to make progress on wafer edge issues by using a plasma-enhanced chemical vapor deposition solution, a deposit with the specificity of being located on the periphery of the wafers.

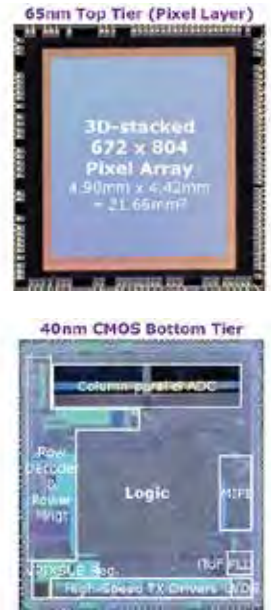
In particular, we intend to develop a silicon oxide deposition technology at the edge of a 300 mm wafer to simplify the management of contamination present at the periphery of the wafer," explains Moty Keovisai (Lam Research), the leader of the study. *"It is now possible to manage the contamination at the edge of the wafer while remaining compatible with further bonding for the construction of innovative 3D architectures."* ◆

SMART IMAGER

The very first 0.5 megapixel 3-dimensional image sensor on the market

STMicroelectronics is currently developing a whole range of new image sensors with unprecedented performance thanks to the 3D integration developed within Nanoelec.

The 3D architecture technologies are industrialized by STMicroelectronics in its four major imager application markets: automotive, industry, personal electronics and computers & peripherals. The international group is now proposing a whole range of products based on these technologies developed within Nanoelec. In 2022, the group launched the VD55H1, a low-noise, low-power indirect time of flight (iToF) sensor array of 672 x 804 pixels (0.54 Mpix). *"This imager is manufactured using advanced backside illuminated stacked slice technology, based precisely on developments made within Nanoelec. The VD55H1 comprises an image sensor "bonded" onto a 40 nm CMOS circuit"*, says Eric Mazaleyrat, Technology Scouting and Innovation Director at STMicroelectronics. *"By comparison with comparable devices on the market: we offer moderate energy consumption, a low noise level and reduced chip size. The VD55H1 currently offers the best cost/resolution compromise on the market with a pixel size of 4.6 µm."*



The VD55H1 is a low-noise, low-power, 672 x 804 pixel (0.54 Mpix), indirect Time-of-Flight (iToF) sensor die manufactured on advanced backside-illuminated, stacked wafer technology developed with Nanoelec
© STMicroelectronics

These products provide smartphones and mass market electronic devices with advanced 3D vision and depth measurement capacity. This type of sensor can be used to map surfaces in three dimensions with a resolution of more than half a million points, by measuring the distance of each point from the sensor. Objects can be detected up to a distance of five meters. They are suitable for both augmented reality and virtual reality applications, such as mapping rooms indoors, video games and 3D avatars. In smartphones, they improve photographic performance notably by offering the following functionalities: the "Bokeh" effect (background blur), automatic selection of the camera and video segmentation. Security via facial recognition is also made more robust thanks to the higher resolution and greater precision of 3D images, which improves applications such as unlocking the telephone, payments via smartphone and indeed secure transactions or access control in general. In the field of robotics, they can be used to map high-resolution 3D scenes at varying distances, along with new and even more powerful functionalities.

"We are also manufacturing Global Shutter type image sensors[1], based on BSI (backside illumination technology) using 3D building blocks developed within IRT Nanoelec", adds Eric Mazaleyrat. *"This innovation comes after several years of development within IRT Nanoelec which were marked by a certain number of outputs, including the Harmony demonstrator in 2018."* In 2021, STMicroelectronics began to produce and distribute these products to major customers. *"They are very success in robotic and automotive type applications"*, adds Eric Mazaleyrat, before stating that *"the teams at STMicroelectronics are currently working on the design of other new products, most of which use wafer stack technology."* ◆

[1] The Global Shutter is an automatic shutter mode used in CMOS photographic sensors, enabling all the pixels of the image sensor array to be read at once, generating an instantaneous image. This is as opposed to a Rolling Shutter sensor which illuminates each line of the pixel array in turn.

SMART IMAGER

DATE 2022

3D technologies are becoming increasingly pervasive in digital architectures, as a strong enabler for heterogeneous integration.

Pascal Vivet, Scientific Director at CEA-List & Deputy Director for the Nanoelec/Smart Imager program organized a workshop on 3D heterogeneous integration at DATE'22, with his scientific committee attracting scientific personalities from Qualcomm, Fraunhoffer Institute, Georgia Tech, Stanford University and CEA.

Due to the large amount of data required and the associated memory capacity, Machine Learning and AI accelerators could benefit from 3D integration not only for High Performance Computing (HPC), but also for the edge and embedded HPC. *"3D integration and associated architectures are opening up a broad spectrum of system solutions, from chiplet-based partitioning for High Performance Computing to various sensors such as fully integrated image sensors embedding AI features, but also with the tight 3D coupling of computing & memory enabling an efficient In-Memory-Computing paradigm"*, explains Pascal Vivet (CEA-List), Deputy Director of the Nanoelec/Smart Imager Program who organized a dedicated workshop at the DATE conference 2022. DATE is the annual reference event for electronic system Design Automation & Test in Europe.

"In the 3D Integration Workshop, we discuss Heterogeneous 3D Architectures and Sensors", adds Pascal Vivet. *"We brought together 50 experts from the academic and industrial worlds who were interested in this exciting and rapidly evolving field, in order to update each other on the latest state-of-the-art, exchange ideas, and discuss future challenges."*

This one-day event consisted of a plenary keynote, guest speakers, and regular presentations from CEA, Qualcomm, Georgia Tech, Stanford University, ETHZ (Switzerland), Fraunhofer Institute, University of Seville, Prophesee, STMicroelectronics, NTU (Singapore), Boston Univ., Univ. of Manchester, Stony Brook Univ., Notre Dame Univ, META Group (Facebook), Siemens EDA, Intel.

DATE'2022 3D Integration: The Heterogeneous 3D Architectures and Sensors workshop was technically co-sponsored by IRT Nanoelec. ◆

- KEY PUBLICATIONS -

New trends in chiplet integration

In two communications in 2021, scientists from CEA Leti and CEA List, associated with colleagues from LIP6, Paris, STMicroelectronics, Siemens EDA, reported on their experience with chiplet integration on an active silicon interposer. They described the improvements underway on direct hybrid bonding for ultra-dense die-to-die interconnects and die-to-wafer bonding for heterogeneous 3D integration (II/V or CMOS). They also presented their circuit prototype: called IntAct, it integrates six chiplets using FDSOI 28-nm technology, which are 3D-stacked onto this active interposer in a 65-nm process, offering a total of 96 computing cores.

PERCEVAL COUDRAIN ET AL.
CHIPLET INTEGRATION ON ACTIVE SILICON INTERPOSER
Applied Power Electronics Conference, June 2021

PASCAL VIVET ET AL.
INTACT: A 96-CORE PROCESSOR WITH SIX CHIPLETS 3D-STACKED ON AN ACTIVE INTERPOSER WITH DISTRIBUTED INTERCONNECTS AND INTEGRATED POWER MANAGEMENT
IEEE Journal of Solid-state Circuits | January 2021

Hybrid Bonding-Based Interconnects

Researchers from CEA, STMicroelectronics and the University of Bordeaux reviewed the most significant qualification and reliability achievements obtained over the last 6 years by the scientific & industrial R&D communities for hybrid bonding-based interconnects (HB) also named Cu-Cu or Cu/SiO2 bonding. Their study concludes that *"once the manufacturing issues (surface preparation, alignment, etc.) have been resolved, this technology is robust and reliable at pitches > 1 µm as it reacts more or less like a conventional back-end of line (BEoL) interconnect."*

STÉPHANE MOREAU ET AL.
ECS J. SOLID STATE SCI. TECHNOL. 11 024001

- KEY PUBLICATIONS -

Towards 5µm interconnection pitch with Die-to-Wafer direct hybrid bonding

The die-to-wafer direct hybrid bonding process is foreseen as a key enabler of heterogeneous 3D integration. Hybrid bonding technologies were first developed on W2W assembly reaching 3D interconnection pitches of 1µm. Recently, CEA-Leti, under Nanoelec, demonstrated the feasibility of DTW direct hybrid bonding at 10µm with a specific die bonder (NEO HB) developed by SET Corporation. A joint research effort from CEA and SET was reported at the 21'Electronic Components and Technology Conference. The paper presents the latest improvements to DTW hybrid bonding process flow and die bonder alignment capability. The main results showed an alignment capability improved to <1µm which enables bonding of die with <5µm interconnection pitch. Multi-interconnection pitch bondings on a wafer were achieved with Cu pitches varying from 5µm to 10µm. A clear gain in bonding and electrical yields is reported and is extremely encouraging for industrialization of this technology.

EMILIE BOURJOT ET AL.
2021 IEEE 71ST ELECTRONIC COMPONENTS AND TECHNOLOGY CONFERENCE (ECTC) - ONLINE

What technologies and architectures for 3D Smart Imagers

At the SEMI international conference, in September 21, Pascal Vivet (CEA-List) Deputy Director of the Nanoelec/Smart Imager program reported on advanced 3D technologies and architectures for 3D Smart Imagers. *"Sensors are becoming increasingly pervasive in our environment"*, he said before stating that *"smart Vision systems will bring disruptive imaging detection & recognition features, with tight integration of computing within the sensor itself."*
He emphasized the need for disruptive technologies and architectures, especially *"a smart Vision system will associate fully distributed pixel & computing architecture, multiscale, region-of-interest, wake-up, high throughput acquisition, embedded energy-efficient neural network and heterogeneous & fine grain 3D technologies."*

PASCAL VIVET
ADVANCED 3D TECHNOLOGIES AND ARCHITECTURES FOR 3D SMART IMAGERS
Guest speaker at 3D & Systems Semi Conference | September 2021

3D: The El Dorado of Heterogeneous Integration

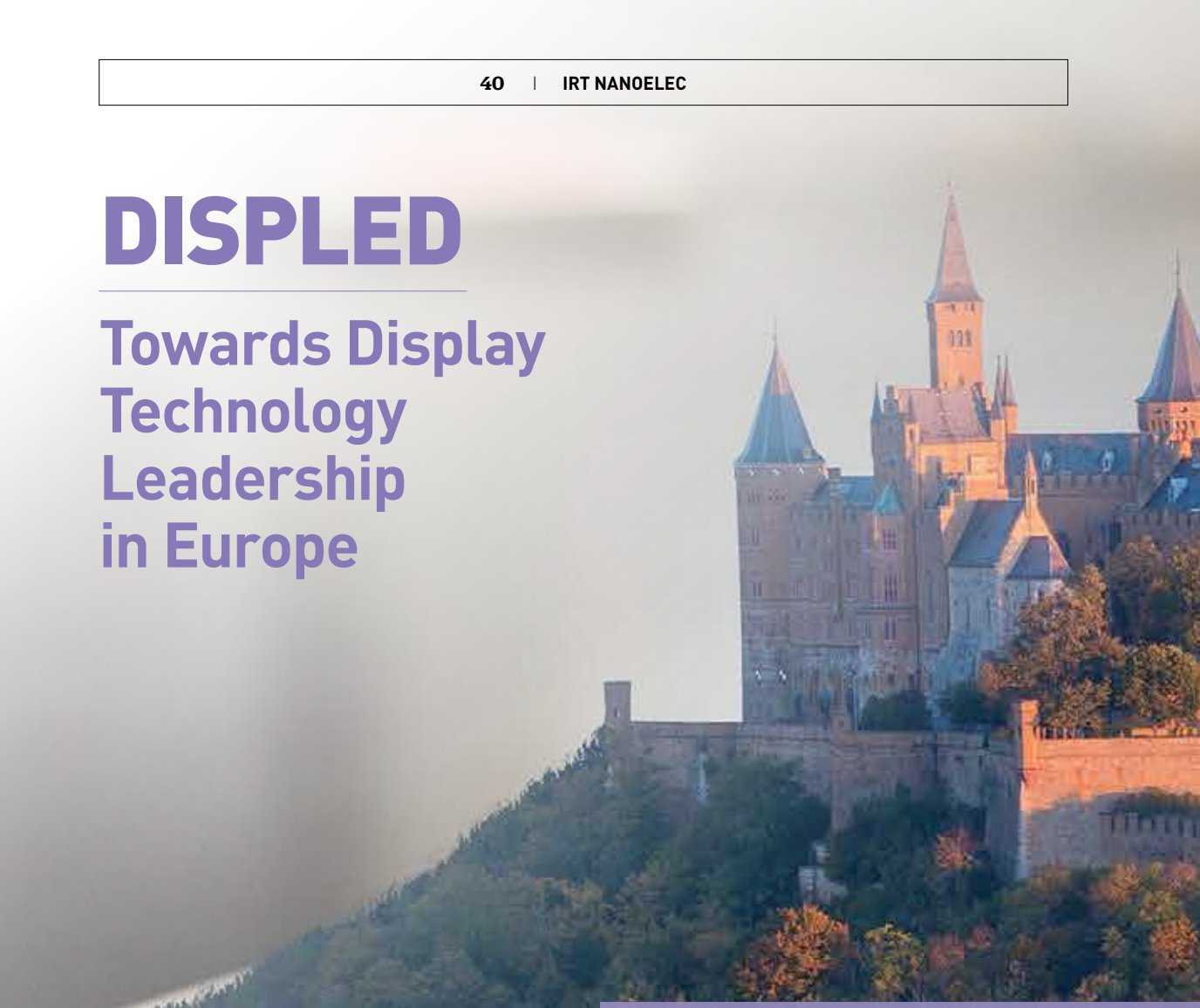
From the cloud to edge computing, the quest for ever-greater power efficiency remains the top priority for researchers. Vertical 3D integration technology enables chips to be stacked in a device to help achieve denser interconnects, which translates into greater power optimization and improved signal propagation within the component. Séverine Cheramy, Former Director of the Nanoelec/3D Integration program and now product line Manager at Aledia, a core partner of Nanoelec, produced two papers reporting the recent demonstrations in hybrid bonding made at CEA-Leti, under Nanoelec. "Following this achievement in the HPC domain, similar architectures are envisioned for quantum computing to vastly improve performance and speed. A team of scientists from CEA-Leti, CEA-List, and the Néel Institute (CNRS) designed the first prototype interposer in 2020", she says in a 3D Incities paper. In addition, in the Chip Scale Review, she co-signed an important overview of Intel and CEA-Leti collaboration (with support from Nanoelec ?). "With Intel's support and the expected collaboration with different players in the supply chain, particularly equipment suppliers, the technology may be a must-have for low-cost, high-performance heterogeneous integration for the future", she concluded.

SÉVERINE CHERAMY ET AL.
3D: THE EL DORADO OF HETEROGENEOUS INTEGRATION
3Dincities web site | February 2021

SÉVERINE CHERAMY (ALEDIA), EMILE BOURJOT (CEA-LETI) & JOHANNA SWAN (INTEL)
HETEROGENEOUS 3D INTEGRATION FOR HIGH-PERFORMANCE COMPUTING
Chip Scale Review | March-April 2021

DISPLED

Towards Display Technology Leadership in Europe



Displed program at a glance

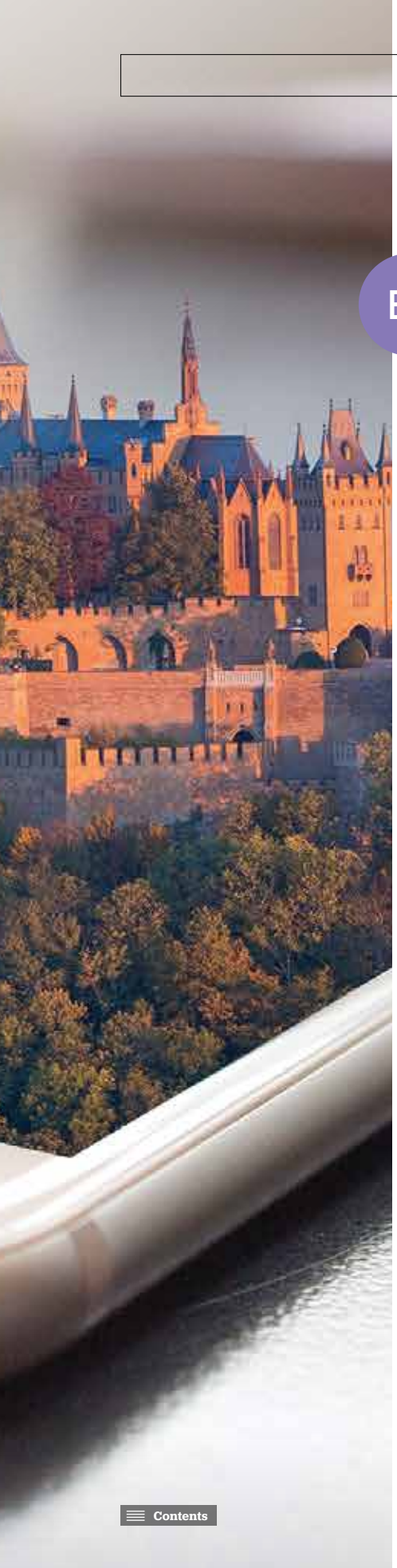
VISION
A unique opportunity for a French & European ecosystem on large display technologies for immersive applications

AMBITION
To design and demonstrate key microLED technologies for high-end, immersive/interactive displays

MISSION
To develop process flows for microLED, Smart-pixel fabrication and mass transfer onto the display

PARTNERS
Aledia
CEA
EVGroup
SET

The Nanoelec/Displed program prepares real breakthroughs in the display industry value chain as well as new image functionalization.
© Pixabay



BY

FRANÇOIS TEMPLIER,
STRATEGIC MARKETING MANAGER FOR DISPLAYS AT CEA AND DIRECTOR OF THE NANOELEC/DISPLED PROGRAM

© P.Jayet/CEA

The aim of the Displed program, launched in 2021, is to bring display production back to France. By bringing around the same table actors situated at various levels along the value chain, we should be able to accelerate our roadmap in support of the industry. We intend to develop a radically new high-performance microLED type display, based on the "Smart Pixel" concept, for which we will be expanding the scope of applications and reinforcing the mass production processes. We will be paving the way for ultra-high resolution video wall technologies, very large flat displays for TVs or interactive meetings, flexible displays or even displays capable of reproducing a 3D immersion in a virtual or remote universe.

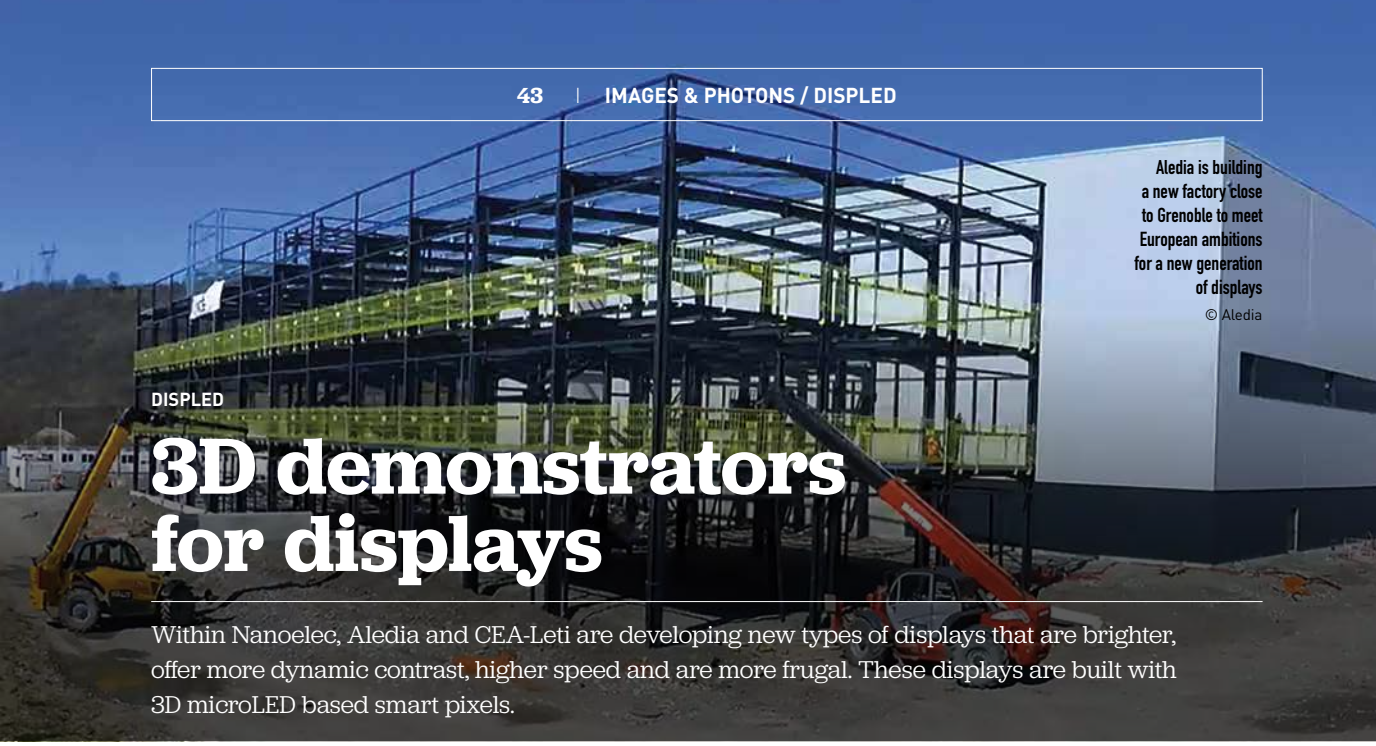
The aim of IRT Nanoelec's Displed program is to demonstrate the industrial scale feasibility of the Smart Pixel concept. This concept consists in hybrid bonding of a layer of microLEDs on a CMOS wafer in order to create a pixel, which can be locally controlled. This pixel can then be placed on any substrate functionalized simply by rows and columns of metal contacts, without requiring the TFTs arrays which can only be manufactured in the Asian "mega-fabs". The stakes of this technology are to enable a relocation of the display industry in France.

The project is based on creating a value chain with a focus on specific steps: assembly of microLED wafers and CMOS wafers, technologies for mass transfer of smart pixel components on a substrate. The technical hurdles relate to the technical and economic viability of the concept: transfer of very small chips on a very large scale and at very high speed. The project is built around five main work packages: wafer assembly using 200 mm technology, scaling to 300 mm technologies and development of packaging and mass transfer solutions for Smart Pixels. Finally, the work will undergo a demonstration phase, and a final activity focuses on the exploration of flexible, immersive, solutions for very high-end displays. ◆

AT CEA-LETI, SILICON DIES HAVE BEEN ASSEMBLED ON WAFER BY A CU-CU HYBRID BONDING PROCESS WITH THE NEO HB EQUIPMENT FROM SET CORPORATION, A CORE PARTNER OF NANOELEC.

NEO HB enables the integration of electronic chips with extremely precise alignment. Design and fabrication of a first generation vacuum-based microtool for mass transfer, also tested on an upgraded version of the FC300 tool was achieved in 2021, through the Nanoelec/Displed program.
SET developed its latest equipment in collaboration with IRT Nanoelec. *"Our prototype of the NEO HB is being used in the clean rooms at CEA-Leti,* explains Pascal Metzger, CEO of SET. *"In June 21, we launched a partnership in the field of die-to-wafer hybrid bonding with SUSS MicroTec for the development of a fully-automated, configurable and high-yield tool for the integration of 3D dies, based on SET's NEO-HB."*
With several hundred machines installed in clean rooms around the world, the company from Haute-Savoie, created in 1975, has been a cooperative since 2012, following the buy-out by its employees. ◆

Last November, SET took part in Semicon Europe in Munich, Germany, the first Semicon event organized since the beginning of the health crisis.
© SET



Aledia is building a new factory close to Grenoble to meet European ambitions for a new generation of displays
© Aledia

DISPLED

3D demonstrators for displays

Within Nanoelec, Aledia and CEA-Leti are developing new types of displays that are brighter, offer more dynamic contrast, higher speed and are more frugal. These displays are built with 3D microLED based smart pixels.

"*These developments employ all the know-how of the Nanoelec/3D program for match-up, plate-to-plate assembly and interconnection of a light emitting module (LEM) pixelated wafer with a CMOS wafer. The aim is collective interconnection of hundreds of millions of 3D LEDs with CMOS components, with the LEMs providing brightness in three colors (red-green-blue in a single pixel) while the CMOS wafers house the pixel control function"*, says Philippe Gilet, CTO & Co-founder of Aledia.

> "In 2021, we obtained successful bonding with good alignment and verified electrical contact for 2D microLEDs with CMOS wafer"

"In 2021, we obtained successful bonding with good alignment and verified electrical contact for 2D microLEDs with CMOS wafer", underlines Muriel Dupont, Aledia referent for the Nanoelec/Displed program. *"During the year, we also demonstrated the fundamentals of the smart pixel display concept through our operating prototype."*

The program evaluates various technological building blocks by means of demonstrators. In 2020, proofs of concept were specified and designed with a specific attention paid to interconnections between the various layers of 3D pixels. *"The challenge is to achieve assemblies of plates rather than of individual pixels"*, points out Séverine Chéramy, Product Line Manager at Aledia. *"And we are aiming for production in accordance with microelectronics standards (200 or 300 mm on silicon) whereas most of today's practices use more specific substrates with small surface areas. Standardized production will enable us to significantly bring down costs."* ◆

On September 3rd, 2021, Agnès Pannier-Runacher, French Minister of Industry, inaugurated the Display Valley in Champagnier near Grenoble, on the site where Aledia is building its next production fab, to be finished by 2023 and expected to hire up to 500 staff. The process to be set up at the Aledia Champagnier factory will integrate the smart pixel technology developed by CEA and Aledia within Nanoelec.
© Aledia/Jayet

DISPLED

Collective Die-to-wafer bonding

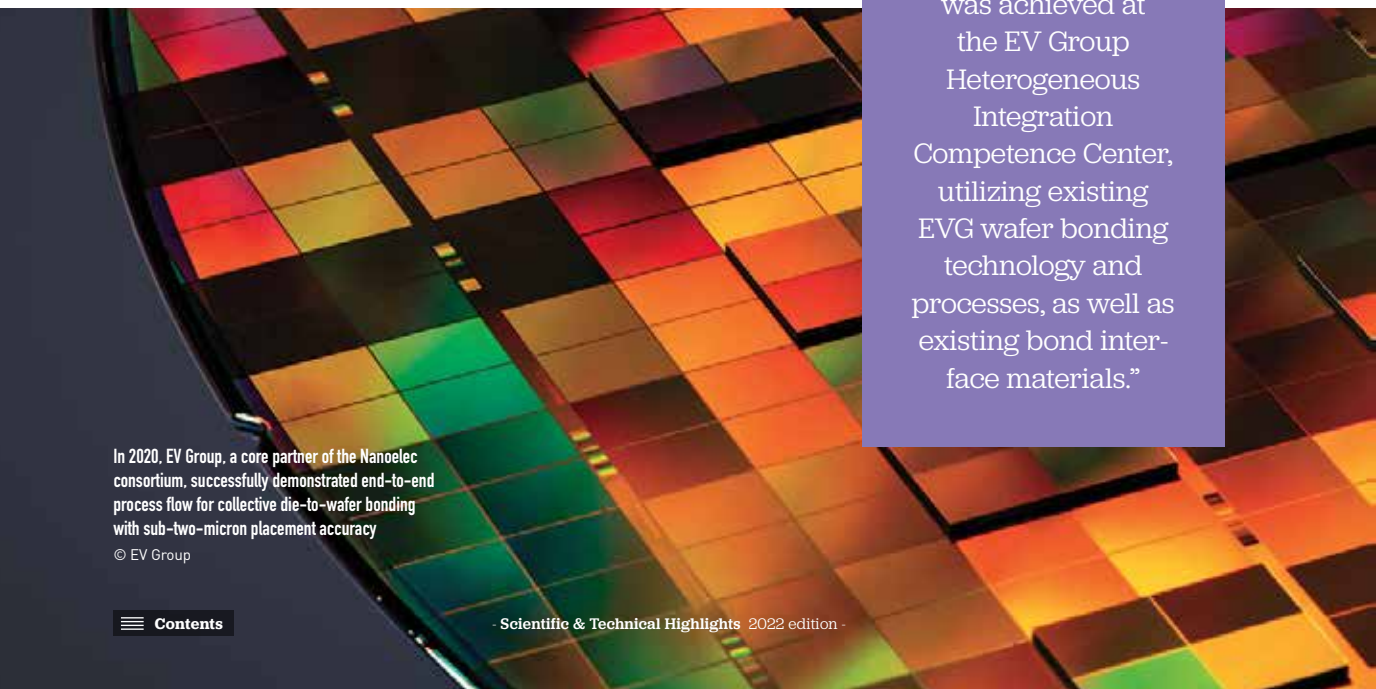
In 2021, EVG unveiled the EVG®40 NT2 automated metrology system, which provides overlay and critical dimension (CD) measurements for wafer-to-wafer (W2W), die-to-wafer (D2W) and die-to-die (D2D) bonding as well as maskless lithography applications.

"Designed for high-volume production with feedback loops for real-time process correction and optimization, the EVG40 NT2 helps device manufacturers, foundries and packaging houses to accelerate the introduction of new 3D/heterogeneous integration products as well as to improve yields and avoid scrapping of highly valuable wafers", explains Markus Wimplinger, Corporate Technology Development & IP Director at EV Group, a core partner of the Nanoelec consortium.

A few months earlier, with substrates provided by Nanoelec and CEA-Leti, EVG successfully demonstrated end-to-end process flow for collective die-to-wafer bonding with sub-two-micron placement accuracy, *"The demonstration was achieved at the EV Group Heterogeneous Integration Competence Center, utilizing existing EVG wafer bonding technology and processes, as well as existing bond interface materials"*, underlines Markus Wimplinger. *"EVG does not have the capability to prepare adequate test material in-house for such applications. For this reason, the partnership with CEA-Leti within IRT Nanoelec is very important, as it connects EVG with world-leading capabilities from the other partners in this consortium. Moreover, this collaboration gives EVG access to the required materials and technologies and also enables us to perform leading-edge research and development."*

This breakthrough represents an important milestone in accelerating the deployment of heterogeneous integration in next-generation 2.5D and 3D semiconductor packaging. Such technologies are required for cutting-edge applications such as artificial intelligence, autonomous driving, augmented/virtual reality and 5G, all of which require the development of high-bandwidth, high-performance and low-power devices without increasing production costs. ◆

"The demonstration was achieved at the EV Group Heterogeneous Integration Competence Center, utilizing existing EVG wafer bonding technology and processes, as well as existing bond interface materials."



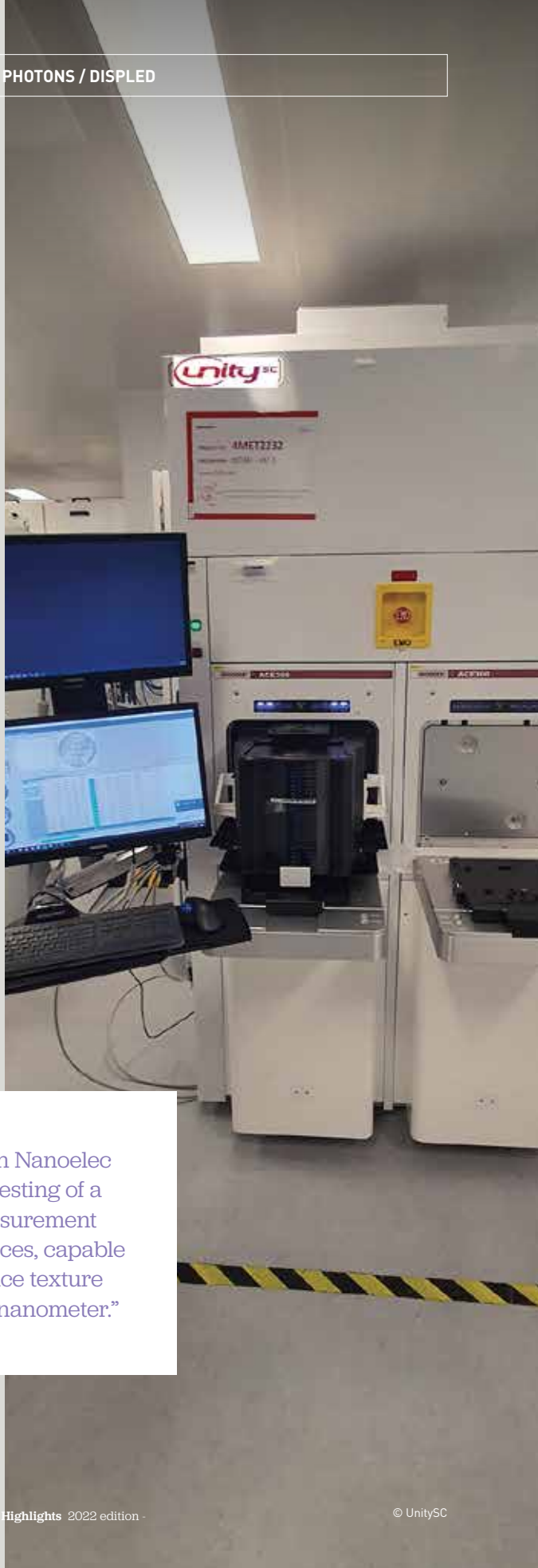
In 2020, EV Group, a core partner of the Nanoelec consortium, successfully demonstrated end-to-end process flow for collective die-to-wafer bonding with sub-two-micron placement accuracy

DISPLED

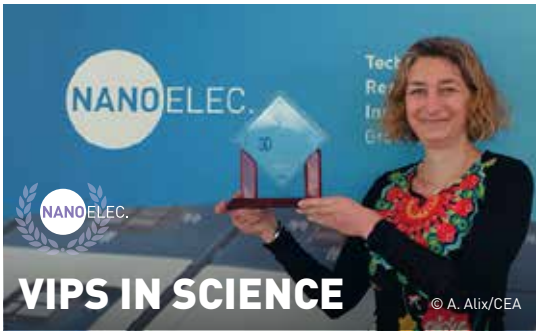
Surface topography before bonding

UnitySC, a subsidiary of the Fogale nanotech group, is a manufacturer specializing in characterization and inspection equipment for the semiconductor industry.

This global company is based in Montbonnot. *"We are associated with Nanoelec for development and testing of a nanotopography measurement technique on large surfaces, capable of detecting chip surface texture variations down to one nanometer"*, says Carlos Beitia, VP Strategic Alliance at UnitySC. This type of characterization is crucial in the case of 3D applications using direct bonding integration technologies, such as assemblies for imagers and displays. ◆



"We are associated with Nanoelec for development and testing of a nanotopography measurement technique on large surfaces, capable of detecting chip surface texture variations down to one nanometer."



SEVERINE CHERAMY (PRODUCT LINE MANAGER AT ALEDIA) RECEIVED THE **"ENGINEER OF THE YEAR 2021"** AWARD FROM THE 3DINCITES PROFESSIONAL REVIEW DEDICATED TO THE INTERNATIONAL 3D ARCHITECTURE COMMUNITY.

Until February 21, Séverine was senior business developer at CEA and director of the former Nanoelec/3D integration program.

DISPLAY INDUSTRY RECOGNIZES FRANÇOIS TEMPLIER

FRANÇOIS TEMPLIER, A CEA-LETI EXPERT IN ADVANCED DISPLAYS AND DIRECTOR OF THE NANOELEC/DISPLED PROGRAM, WAS NAMED **A FELLOW OF THE SOCIETY FOR INFORMATION DISPLAY AT DISPLAY WEEK 2021**, THE INDUSTRY'S FLAGSHIP EVENT.

The honor recognizes Templier's "many contributions to the science and technology of thin-film transistors, flexible displays, OLED microdisplays, and GaN micro-LED displays." François Templier has had a significant impact in the field with his research on GaN micro-LED displays. *"This honor acknowledges my long-standing commitment to display research and development, and micro-LED displays in particular. However, it is also a testament to the contributions of the process technicians and engineers and PhD students I have worked with over the years"* said François Templier. *"It is gratifying to see our achievements recognized by my peers."*

- KEY PUBLICATIONS -

Award: 3D interconnects compatible with foundry manufacturing lines

The study on '3D interconnection using copper direct hybrid bonding for GaN on silicon wafer' presented by a CEA-Leti team under Nanoelec received the 'Best Paper' award at the IEEE International 3D System Integration Conference (3DIC, November 21).

"We have developed a complete process flow for 3D interconnection which is targeted to be compatible with foundry production lines, including an innovative CMP process specifically developed for the new Cu/SiO2 hybrid interface with GaN devices", explains Christophe Dubarry as first author of the paper.
"The process described in the paper is performed on the back side of a CMOS wafer, after hybrid bonding on the wafer front side. The integration process maintained good metal integrity along the entire 3D link despite the heterogeneous conductive materials. And our electrical test vehicle has shown excellent morphological and electrical performance (resistance and leakage) with connection dimensions ranging from 3x3µm² to 5x5µm² in size, which confirms the scalability of these 3D contacts", he comments.

A 3D functional interconnections process flow for GaN applications is under development with Cu/SiO2. Applications like 6G or displays could use these interconnections between a GaN device and logic devices on silicon.

CHRISTOPHE DUBARRY & AL.
3D INTERCONNECTION USING COPPER DIRECT HYBRID BONDING FOR GAN ON SILICON WAFER
IEEE International 3D System Integration Conference (3DIC) | Raleigh, USA | November 2021

- KEY PUBLICATIONS -

Die-to-Wafer Bonding Steps into the Spotlight on a Heterogeneous Integration Stage

The semiconductor industry is currently undergoing the most radical change in its history. Many new applications such as artificial intelligence (AI), augmented/virtual reality and autonomous driving require enormous computing power with processors optimized specifically for each application. At the same time, development cycles are becoming shorter, costs for new chip designs are rising exponentially, and yields in many cases are declining. All of these aspects can only be tackled if the principles of the entire semiconductor manufacturing process are changed.

While 2D transistor scaling is still important, the rising costs and complexity associated with scaling have driven the semiconductor industry to turn to 3D integration and heterogeneous integration – the manufacturing, assembly and packaging of multiple different components or dies with different feature sizes and materials onto a single device or package – in order to increase performance on new device generations supporting these new applications. This migration to advanced packaging as a leading driver of innovation began with the transition from monolithic systems to die-level systems, such as newly released smartphone application processors, which combine individual components such as the processor, memory and AI/neural components using advanced packaging. This transformation will only accelerate in the coming years with the further miniaturization of these components from dies to chiplets, thus enabling much more precise and individual mapping of customer and application requirements.

THOMAS UHRMANN
DIE-TO-WAFER BONDING STEPS INTO THE SPOTLIGHT ON A HETEROGENEOUS INTEGRATION STAGE
White paper, www.EVGroup.com | April 2021

Towards 5μm Interconnection Pitch with Die-to-Wafer Direct Hybrid Bonding

The die-to-wafer direct hybrid bonding process is foreseen as a key enabler of heterogeneous 3D integration. Hybrid bonding technologies were first developed on W2W assembly reaching a 3D interconnection pitch of 1µm. CEA-Leti demonstrated the feasibility of DTW direct hybrid bonding at 10µm with a specific die bonder (NEO HB) developed by SET Corporation. In July 21, at the Electronic Components and Technology Conference, they presented the latest improvements to DTW hybrid bonding process flow and die bonder alignment capability. The main results showed an alignment capability improvement to <1µm which allows die bonding with <5µm interconnection pitch. Finally, multi-interconnection pitch bondings on a wafer were achieved with Cu pitches varying from 5µm to 10µm.

EMILIE BOURJOT & AL.
TOWARDS 5µM INTERCONNECTION PITCH WITH DIE-TO-WAFER DIRECT HYBRID BONDING
IEEE 71st Electronic Components and Technology Conference | June 1-July 4, 2021, Online

PHOTONIC SENSORS

Photonic sensors program at a glance

VISION
New sensor opportunities based on large-scale 300mm silicon photonic technologies

AMBITION
Enrich our photonic prototyping and industrial platforms with key building blocks enabling new sensors to address Medtech, Environment, Consumers goods, Mobility (Lidars) and Computing

MISSION
Miniaturize sensors/ Diversify the fields of applications/Manage the integration of thousands of functions on the same chip/Increase technology readiness level using CAD tools and enrich our device library including performance corners, fabrication process flow

PARTNERS
Almae
CEA
CNRS
Siemens EDA
STMicroelectronics

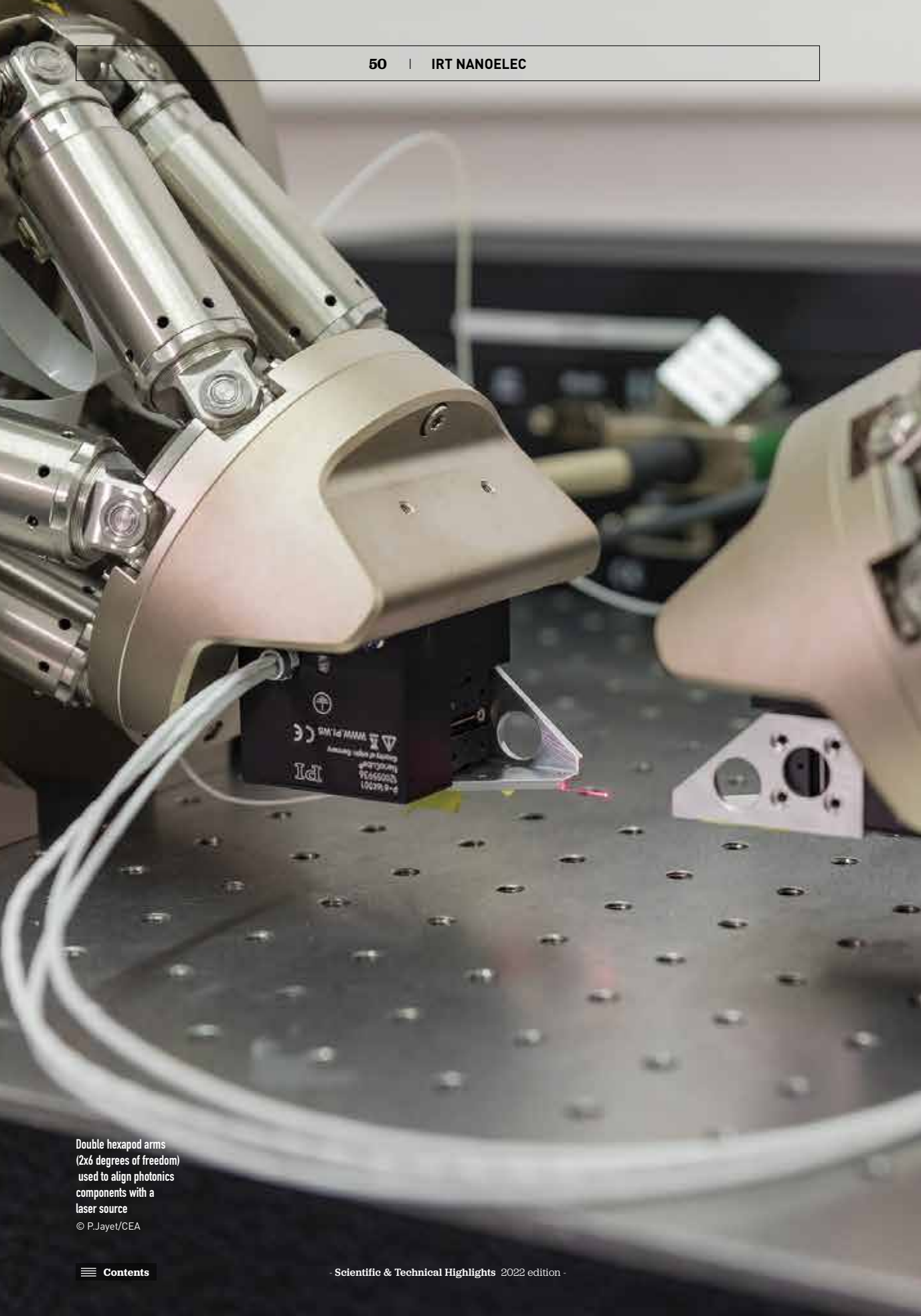
BY

STÉPHANIE GAUGIRAN
HEAD OF THE NEW PHOTONIC APPLICATION SECTOR AT CEA-LETI AND DIRECTOR OF THE NANOELEC/PHOTONIC SENSORS PROGRAM

© UtopikPhoto/CEA

The global market for optical sensors is already worth more than 20 billion dollars, with a target annual growth rate in excess of 10% for the coming decade. These sensors are of interest for numerous applications requiring sensitivity, selectivity, versatility and high acquisition rate. By developing this type of sensors on a silicon platform for integrated photonics, we aim to propose new generations of components with improved compactness, light weight and low consumption while bringing down production costs. The main technological challenges for these sensors are measurement precision and stability, miniaturization, data processing and transfer, as well as compatibility with mass production constraints.
The unique properties and the performance of integrated photonics are essential in being able to meet these requirements. Optical beams can be used in sensors for a wide variety of tasks: scanning a scene, measuring or converting a signal, processing and transferring data. Furthermore, our technology can be used to integrate thousands of miniaturized photonic functions in a single microelectronic chip. The partners of the Nanoelec/Photonic Sensors program are looking at applications such as Lidars, inertial sensors (gyroscope) and biochemical sensors for health and environment applications.

In 2021, we demonstrated OPA circuits for Lidars at 1550 nm and 905 nm, validating the manufacturing processes including characterization methods. The program delivered new design environments based on the Tanner tool from Siemens EDA suited to the 300mm photonics technology from STMicroelectronics and CEA-Leti. ◆



Double hexapod arms (2x6 degrees of freedom) used to align photonics components with a laser source
© P.Jayet/CEA

PHOTONIC SENSORS

Widespread Use of Lidar Systems Based on Integrated Optical Phased Arrays (OPAs)

Taking a critical step towards developing Lidar systems for widespread commercial applications, teams at Nanoelec have developed generic algorithms to calibrate high-channel-count optical phased arrays (OPAs), as well as an advanced measurement setup enabling wafer-scale OPA characterization.

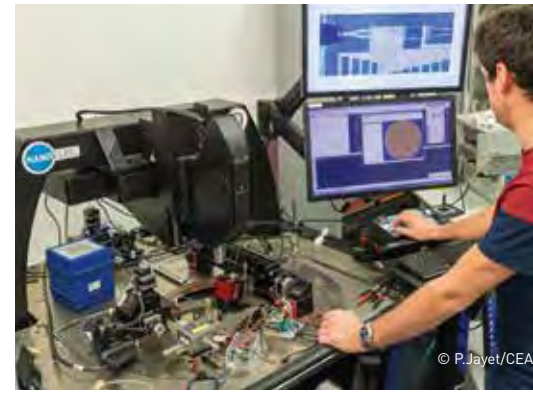
OPAs are an emerging technology made of arrays of closely spaced (around 1 µm) optical antennas which radiate coherent light in a broad angular range. The interference pattern produced can be changed by adjusting the relative phase of the light emitted by each antenna. For example, if the phase gradient between the antennas is linear, a directional beam is formed. By changing the slope of the linear gradient, the direction of the beam can be controlled, which enables solid-state beam steering.

"The development of a high-performance OPA would pave the way for inexpensive Lidar systems for autonomous vehicles, holographic displays, biomedical imaging and many other applications."

"The development of a high-performance OPA would pave the way for inexpensive Lidar systems for autonomous vehicles, holographic displays, biomedical imaging and many other applications", says Sylvain Guerber, the lead author of a paper from CEA-Leti and STMicroelectronics at the 21'Photonics West International Conference.

"This can improve performance in scanning speed, power efficiency and resolution compared to the heavy, power-hungry and expensive mechanical beam-steering systems used in current lidars. An additional feature of OPA-based lidar systems is that they have no moving parts, as solid-state beam steering is achieved simply by phase-tuning the antennas, which significantly reduces the size and cost of these systems", he adds.

Lidar, which stands for Light Detection And Ranging, has emerged as a key enabling technology for tomorrow's sensing and vision systems. In addition to automotive and medical uses, they could enable autonomous mobility for drones and robots, as well as industrial automation. Commercial Lidar systems must meet stringent requirements, especially for automotive applications. In particular, a high-power, low-divergence beam is needed to accurately resolve a scene. For example, resolving a 10-cm object at 100 m requires an OPA operating at a wavelength of 1 µm with a circuit consisting of at least 1,000 antennas, each spaced 1 µm apart. Therefore, the development of high-channel-count OPAs is necessary for a commercial OPA-based Lidar system. ◆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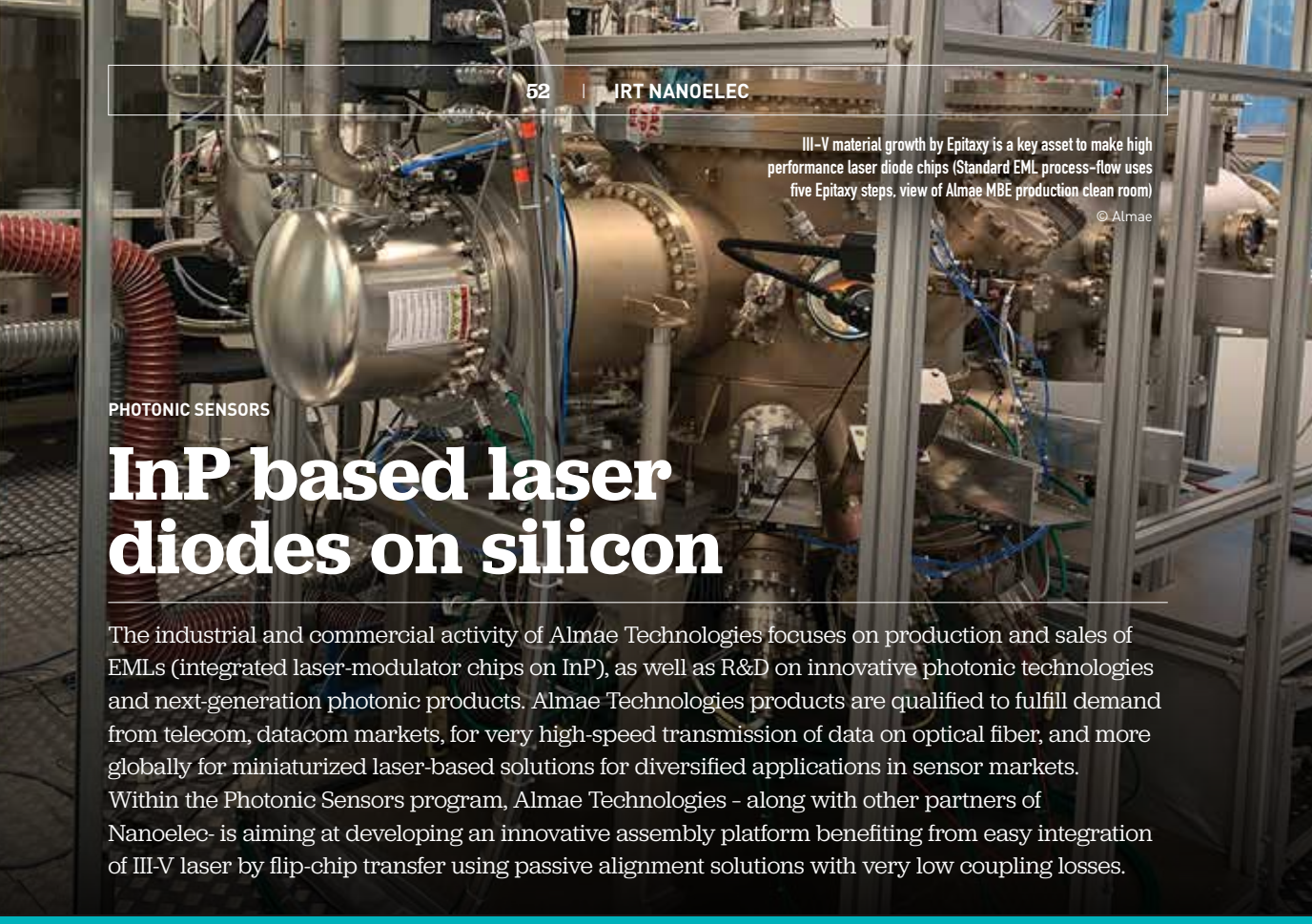

III-V material growth by Epitaxy is a key asset to make high performance laser diode chips (Standard EML process-flow uses five Epitaxy steps. view of Almae MBE production clean room)
© Almae

PHOTONIC SENSORS

InP based laser diodes on silicon

The industrial and commercial activity of Almae Technologies focuses on production and sales of EMLs (integrated laser-modulator chips on InP), as well as R&D on innovative photonic technologies and next-generation photonic products. Almae Technologies products are qualified to fulfill demand from telecom, datacom markets, for very high-speed transmission of data on optical fiber, and more globally for miniaturized laser-based solutions for diversified applications in sensor markets.
Within the Photonic Sensors program, Almae Technologies - along with other partners of Nanoelec- is aiming at developing an innovative assembly platform benefiting from easy integration of III-V laser by flip-chip transfer using passive alignment solutions with very low coupling losses.

“

A REVIEW OFTHE ISSUES WITH
JEAN-LOUIS GENTNER
FROM ALMAE TECHNOLOGIES

THE LASER CHIP IS A CORE ELEMENT OF THE SUBSYSTEMS INTEGRATED FOR THE PHOTONIC SENSORS. WHAT IS AT STAKE?
With its photonic sensors program, Nanoelec is looking to prepare for the mass production of sensor applications in a wide variety of fields: lidar, environment, health, etc. Optical beams can thus be used in sensors for widely differing tasks: scan a scene, measure or convert a signal, process and transfer data. These applications require specific performances for the laser sources themselves: spectral purity, wavelength, adapted operating temperature range (requiring a particular design of the laser gain structure as well as a specific adaptation to the integration platform to obtain the required performances).

WHAT ARE YOUR TARGET APPLICATION MARKETS?
The market for photonic chips on silicon could well exceed $1 billion within a few years. Growth will remain driven by datacom applications for the short term. However, the emergence of new applications in consumer markets for which growth will even be greater is anticipated, with initial penetration of mass-market products, like machine vision, including lidars for autonomous vehicle, or sensors for environment monitoring and “connected health”. However, we are well aware that these sectors will be highly competitive, requiring a multi-level strategy if we are to achieve a position on those markets and prepare for industrial operation. We are facing a real technological breakthrough to move from professional applications to consumer applications and meet the challenge of high volume and low unit cost of for integrated photonic sensor chips.

WHAT IS YOUR POSITION IN NANOELEC'S PHOTONICS PROGRAM?
Almae Technologies designs and builds InP-based high power, ultra-fast, integrated photonic chips essential for new generation telecom and datacom infrastructures and more broadly for all connectivity solutions. We contribute to the program in the area of semiconductor material design of the InP family for integrated laser fabrication and in key design elements of the integration platform to optimize its performance. In the future, we are particularly

interested in participating to the emergence of an industrial integrated photonics ecosystem. We will contribute to the choice of the most suitable technical platform and will invest in III-V material growth and wafer processing capacity increase in order to capture emerging mass markets and diversify our offer with disruptive technical solutions in phase with market mega trends. The ability of program partners to produce fast loop demonstrators is one of the key factors to keep pace with these mega trends and attract interest of major market players.

WHAT ARE YOUR PROSPECTS FOR THESE TECHNOLOGIES DEVELOPED WITH THE NANOELEC PARTNERS?

The market trends are powerful in favor of Photonic Integration. However, they come with challenges : first, we should establish a highly automated PIC sub-system manufacturing platform to benefit from innovation in chip packaging, regain market leadership leadership and provide easy access to European start-ups; we also need to accelerate the emergence of next generation wafer level manufacturing platforms by leveraging our leadership in Silicon Photonics circuits manufacturing with our leading edge position in III-V material technologies, for performance and scaling. These challenges will have to be addressed in close collaboration and Nanoelec is a perfect organization to achieve this if we can broaden partnership and accelerate developments by focusing efforts of all partners. Nanoelec is also a perfect place to prepare next industrial deployment steps, which will likely involve new major industrial initiatives. Short-term objective is to put our mature and field proven InP laser technology at play to demonstrate applications in a fast turnaround hybrid integration platform, this for various Lidar and sensor applications. Longer term, we are aiming to develop a second-generation laser technology based on InP on Si capable of meeting the demand for far greater volume at lower cost. Time being of the essence in keeping technical leadership, this longer-term objective is already part of the program, major building blocks having been demonstrated already, and will be the subject of new initiatives in the near term. ◆

> "The market for photonic chips on silicon could well exceed $1 billion within a few years."

Silicon photonics switch layout based on CEA-Leti / Siemens EDA PDK
© CEA-Siemens EDA

PHOTONIC SENSORS

Process Design Kit

An integrated Process Design Kit (PDK) has been included in the Tanner design flow from Siemens EDA and is now opened up to Nanoelec partners.

Eleonore Hardy is Business developer in Silicon Photonics at CEA-Leti and Deputy Director of the Photonic Sensors program at Nanoelec.
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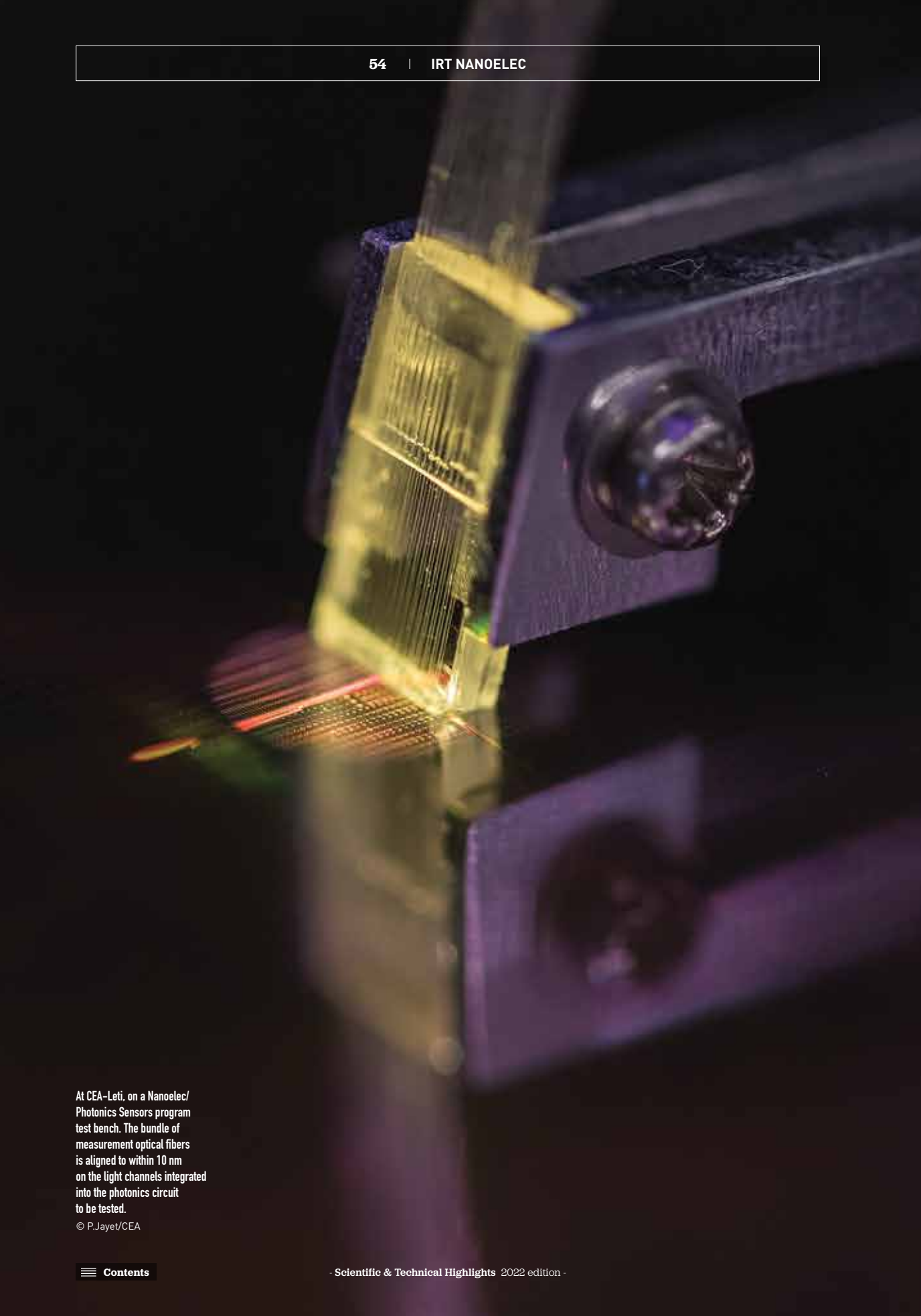
With its photonic sensors program, Nanoelec is looking to prepare for the mass production of sensor applications in a wide variety of fields: lidar, environment, health, etc. Optical beams can thus be used in sensors for widely differing tasks: scan a scene, measure or convert a signal, process and transfer data. These applications require specific performances for the laser sources themselves: spectral purity, wavelength, adapted operating temperature range (requiring a particular design of the laser gain structure as well as a specific adaptation to the integration platform to obtain the required performances).

In 2021, within the multi-partner Nanoelec consortium, we therefore took part in defining a demonstrator for a new gas sensor in the NIR-SWIR near-medium infrared spectral band, as well as the first manufacturing tests for a III-V/Si hybrid laser using 300nm thick silicon. ◆



At CEA-Leti, on a Nanoelec/ Photonics Sensors program test bench. The bundle of measurement optical fibers is aligned to within 10 nm on the light channels integrated into the photonics circuit to be tested.

- KEY PUBLICATIONS -

Award: Cheap and low-power optical communication systems

Quentin Wilmart (CEA-Leti, contributor to the Nanoelec/ Photonic Sensors program) received the Young Research Award at 2021 International Conference on Solid State Devices & Materials (SSDM). Quentin unveiled the very first integration of a hybrid III-V laser on the backside of a Si/SiN wafer. *"To de-bottleneck data centers, it is beneficial to replace conventional electronic communication with optics, because it's cheaper, faster, and perhaps more importantly, low-power"*, underlines Wilmart, whose work pioneers mass-market silicon photonics-based transceivers.

"Our work has been conducted within the Nanoelec framework and a CEA-Leti contribution to the H2020 Cosmicc project (2015-2019). With the aim of building cheap, low-power optical communication systems, the project focused on developing silicon microchips embedding photonic integrated circuits, which can send or receive high data volumes at very high speed conveyed by light in optical fibers."

Award : Ni2P Contact technology for 300 mm Si Photonics

Research teams from STMicroelectronics and CEA-Leti, working together within Nanoelec, received the Best Contributed Presentation Award at the 20th International Workshop on Junction Technology (IWJT) #IWJT2021 conference. The development of a contact technology module is one of the building blocks for maturing a 300mm Si photonics platform. The team developed Ni 2 P thin films on a 300mm platform, in order to assess their potential use as contact layers for Si photonics devices. Ni 2 P layers, obtained by magnetron sputtering of a Ni 2 P target, were implemented and integrated on III-V-based structures to extract the contact resistivity on n-InP and p-InGaAs. Due to its high thermal stability and low contact resistivity, Ni 2 P metallization exhibited the best results among the Ni-based metallizations studied for contacting n-InP layers.

FLORE BOYER & AL.
CONTACT TECHNOLOGY FOR 300MM SI PHOTONICS PLATFORM
20th International Workshop on Junction Technology (IWJT) | Japan, June 2021

Electro-refractive modulators to reduce energy needs

Silicon photonic modulators are a key component for electro-optic transmitters in data centers. Electro-refractive modulators relying on free carrier plasma dispersion in a Mach-Zehnder interferometer have become the most popular solution. Accumulation-based capacitive modulators are an efficient approach, which can reduce modulation power consumption. Preparing his PhD thesis with the support of Nanoelec core partners (CEA-Leti, CNRS & STMicroelectronics), Ismael Charlet studied the behavior of capacitive modulators with polycrystalline silicon to form the capacitance. *"The modulators are made within the standard fabrication flow with only a few add-ons. We demonstrated that furnace annealing conditions and excimer laser annealing conditions during polycrystalline silicon formation enhance the modulator bandwidths"*, he says. The results were reported at the 21'Photonics West International Conference.

ISMAEL CHARLET & AL. (CEA-LETI & CNRS & STMICROELECTRONICS, UNIV. GRENOBLE-ALPES, UNIV. PARIS-SACLAY)
SI CAPACITIVE MODULATOR INTEGRATION IN A 300MM SILICON PHOTONICS PLATFORM USING DIFFERENT ANNEALING CONDITIONS
SPIE Opto & Photonics West, USA | January 2021

- KEY PUBLICATIONS -

Silicon photonics for terabit/s communication in data centers and exascale computers

Silicon Photonics Technology using a submicron SOI platform, which commercially emerged at the beginning of the century, has now gained market shares in the field of fiber optic interconnects, from Inter- to Intra-Data Center communications. With growing demand in terms of aggregated bandwidth, scalability, transceiver form factor, and cost, Silicon Photonics is expected to play a growing role, especially with the foreseeable need to co-package photonic transceivers with next generation Ethernet switches. This new paradigm will be possible only with an evolution of existing Silicon Photonics manufacturing platforms, in order to solve the challenges of 3D packaging, laser integration, reflow-compatible optical connectors and high efficiency, low footprint modulators. Achieving these challenges may pave the way to Terabit scale communications in Data Centers and High Performance Computing Systems (HPC).

STÉPHANE BERNABÉ ET AL.
SILICON PHOTONICS FOR TERABIT/S COMMUNICATION IN DATA CENTERS AND EXASCALE COMPUTERS
Solid-State Electronics Review | May 2021

Platinum redistribution in the Ni0.9Pt0.1/InP system

Ni-based contacts are envisioned for integrating III-V device contacts on a 300 mm platform. In this regard, the Pt redistribution in the Ni0.9Pt0.1/InP system, and the impact of Pt-alloying of Ni thin films on InP over solid-state reaction and layer morphology have been investigated. Results have shown that at low temperature (< 300°C), the presence of Pt partially slows down the diffusion of Ni towards the InP substrate, which as a result delays the growth of an intermixing amorphous Ni-In-P layer. In addition, the presence of Pt in the system has delayed the consumption of the Ni0.9Pt0.1 layer. At higher temperatures (> 300°C), the thermal energy brought to the system overcomes the Pt-induced partially slowed down Ni diffusion, and the observed phase formation sequence indicates that the Ni-based crystallized phases (NiP, NiP and NiInP) are identified regardless of the presence of Pt, which is not incorporated into the formed Ni-based phases (NiP, NiP and NiInP). Instead, the latter is rejected from the forming interface, which allows it to participate to the formation of the stable PtIn crystallized phase.

FLORE BOYER & AL.
PLATINUM REDISTRIBUTION IN THE NI0.9PT0.1/INP SYSTEM: IMPACT ON SOLID-STATE REACTION AND LAYER MORPHOLOGY
Materials Science in Semiconductor Processing | June 2021

A Lidar on a 300 mm platform

Today, Silicon photonics technology provides solutions for data processing and is benefiting from the 300mm CMOS industrial manufacturing infrastructure that enable low cost and reliable technologies. Aas the data market is booming, the need for sensors in mobile and automotive markets is also expanding. Indeed, the development of 3D scan sensors for short-range and long-range applications may serve the consumer market (e.g. mobile for more accurate sensors) or automotive market for driver assistance.

905nm OPA are an opportunity to propose solid-state beam steering for LIDAR applications with the major advantage of being compatible with high-performance Si-based SPAD detectors for reception, that are commercially available at low cost. Unlike more classical 1550nm Si-based technology OPAs, the required technology platform should integrate several Si & SiN building blocks for this purpose.

While some demonstrations of OPA for 905nm LiDAR were made in 2019 with a 200mm SiN platform, research teams from STMicroelectronics and CEA-Leti, working together within Nanoelec, produced the very first demonstration on a 300mm wafer industrial platform with all components previously dedicated to the SWIR domain.

STEPHANE MONFRAY & AL.
OPTICAL PHASED ARRAY FOR 905NM LIDAR APPLICATIONS INTEGRATED ON 300MM SI-PHOTONIC PLATFORM
Optical Fiber Communication Conference, San Diego (US) | March 2022

- KEY PUBLICATIONS -

3D integration for new architectures of photonic modules on silicon

The rise of new technologies such as high-performance computing or artificial intelligence require high bandwidth links between the computer nodes and storage. Optical links, with greater performance and power efficiency than electrical links, are an interesting solution for addressing these needs.
Preparing his thesis at STMicroelectronics within Nanoelec, Pierre Tissier investigated possibilities to interface the optical links and electronic computing elements, and to bring the optical link as close as possible to the computing element, using a tridimensional architecture based on a photonic interposer.
"The co integration of silicon photonics with 3D interconnections needed for the photonic interposer is therefore mandatory to ensure adequate performance", he explains. This co-integration presents challenges, from both the microscopic and macroscopic points of view. More particularly, the presence of metallic interconnections can modify the optical properties of photonic devices nearby. *"I have been working on the evaluation of this disturbance, to present optimal design rules to ensure correct optical performance. The challenges identified for the production of the silicon photonic interposer have been addressed, and design rules have been established for future architectures based on such a circuit"*, he adds.

Thesis defended by Pierre Tissier at Université de Grenoble-Alpes | October 2021

Advanced electro-refractive devices in silicon photonic integrated circuits for next generation applications

Global Internet traffic increases year by year, which is proving to be an issue for data centers. Silicon photonics is a strong solution for addressing such constraints. Modulation within silicon is based on the free plasma dispersion effect. Basically, it relies on the integration of a PN junction within an optical waveguide Nevertheless, this approach exhibits relatively low efficiency. This happens to be an issue with regard to the global maximization of the optical modulation amplitude. In his PhD work prepared at CEA-Leti within Nanoelec, Ismaël Charlet investigated two solutions to improve modulator efficiency: *"On one hand, I focus on a capacitive structure based on a semi-conductor/insulator/semi-conductor junction. On the other hand, strained-SiGe grown on silicon exhibits higher electro-optical coefficients,"* he says.
To do so, a few additional steps were performed with the foundries of STMicroelectronics and the CEA-Leti. Ismael also performed numerical simulations to assess best achievable performance with these 2 solutions.

Thesis defended by Ismaël Charlet at Université Paris Saclay | July 2021

PULSE

© Morel/CEA

Pulse program at a glance

VISION
Due to the rise in cybercrime, the cybersecurity of the Internet of Things (IoT) is a major challenge for digital trust. Strengthening and hardening critical embedded, increasingly interconnected and smarter systems is now vital.

AMBITION
New smart and intrinsically secure nanocomponents to reinforce systems resistance against future cyberattacks
+ Improved security of smart embedded systems throughout their lifecycle (including AI algorithms)
+ Safer deployment environments through digital ID, data sovereignty and secure interactions between smart systems

MISSION
To develop and test new security features for components and systems in three fields of application: Industry 4.0, Homecare and Robotics

PARTNERS
CEA
Diabeloop
Grenoble-INP
Inria
Schneider Electric
STMicroelectronics
UGA

BY

VINCENT CACHARD
NANOELEC/ DIRECTOR OF THE PULSE PROGRAM AND MANAGER OF THE HARDWARE SECURITY RESEARCH DEPARTMENT AT CEA-LETI

© P. Jayet/CEA

With the advent of the Internet of Things (IoT), new services based on heterogeneous connected devices and data management are multiplying. At the same time, the dramatic increase in the number of cyber-attacks is raising awareness among the public and institutions regarding the risks associated with a too rapid and poorly controlled digital transition.

New hardware and software vulnerabilities are being identified and revealed to the general public in a time where medical devices, automobiles, industrial and urban equipment are becoming increasingly connected and autonomous. These vulnerabilities and the attacks that exploit them are undermining the trust of the users in connected services and goods. Consequently, the impact generated by this phenomenon is not only on the image of the companies, but also on society's economy and citizen's privacy. They even sometimes compromise the legal and social liability of the public or private players who have inadequately protected their products.

In the same time, when designing digital products, cybersecurity is often seen as a constraint which should not weigh too heavily on the primary function (health care, mobility, manufacturing, etc.), whether in terms of cost, performance, or ergonomics.

The challenge of the Nanoelec/ Pulse program is thus to identify how electronics technologies can help providing an appropriate answer to this new paradigm.
It aims at developing new technologies that will allow the emergence of connected products and services capable of increasing operating security, protecting confidentiality, authenticity and integrity of digital data, guaranteeing protection of privacy, while simplifying the deployment of cybersecurity strategies. Our work focuses on three application fields: the cybersecurity of industrial systems, that of healthcare products and the security of autonomous systems and self-driving vehicles.
In its own way, the Pulse program aims to help meet the vital needs of institutions, solutions suppliers and users to live in a trusted digital world. ◆

PULSE

Home & health cybersecurity

Reliable Connected Medical Devices

Diabeloop develops automated insulin delivery solutions enabling diabetics to regulate their blood sugar levels. The company was founded in 2015 and has developed the first closed loop connected medical device mimicking the functions of the pancreas. By joining Nanoelec, Diabeloop aims to improve the security of its medical devices and is exploring new security strategies. A discussion with Erik Huneker, co-founder and CEO of Diabeloop.

© Diabeloop

“

ERIK HUNEKER,
CEO OF
DIABELOOP

YOU HAVE ENTERED INTO A CONSORTIUM WITH NANOELEC FOR A PROGRAM OF WORK ON CYBERSECURITY. WHAT IS AT STAKE HERE?

Developing technology in the health sector helps optimize the treatment of the patients and the ability of the healthcare personnel to treat them, but it can also lead to an increase in cyberattacks attempts and the risk of health data leaks. The cybersecurity of medical devices is therefore today a major concern for the manufacturers and healthcare and certification organizations, with the primary issues being to protect individuals as well as the integrity and confidentiality of their personal health data.

HOW ARE DATA PROCESSED IN THE DIABELOOP DEVICES?

Our first medical device consists of a continuous glucose measurement sensor and a terminal containing our self-learning algorithm which determines the insulin dose that the insulin pump needs to deliver. The data are transmitted to a display platform for the person equipped with our system and they can then choose to share access with their health care team and/or those close to them. It is the development of these reinforced data transfer mechanisms that will make sharing as flexible as possible, when and where the person so wishes.

WHAT IS YOUR PREFERRED APPROACH AT NANOELEC?

For our artificial intelligence systems, we must adress issues of operation (resistance to physical and logical attacks), authenticity (proof of integrity) and confidentiality (resistance to reverse engineering). We must also protect them against the new types of attacks made possible by quantum computers, if this technology ever becomes a reality. The technical solutions proposed by Nanoelec and its partners in the Pulse program are in line with this strategy.

More broadly, we seek to strengthen a generic framework for the cybersecurity of connected medical devices and for the standardization of security architectures in the healthcare and IoT sectors. ◆

The DBLG1 from the French manufacturer Diabeloop
© Diabeloop

Home & health cybersecurity

Accurate occupancy data to assist smart building management

A brand new product of Schneider electric might be a game changer in the journey to net-zero carbon buildings.
It has been introduced in April 2022, and brings high-performance people-counting features, developed through an innovative partnership led in the framework of #Nanoelec by @STMicroelectronics, @Schneider Electric and @Lynred.

On April 2022, Schneider Electric presented SpaceLogic™ Insight-Sensor, an advanced six-in-one ceiling mounted room/zone sensor for people counting, occupancy, light, sound, temperature, and humidity sensing. Unlike traditional ventilation control that relies on schedules or CO2 levels, the Sensor, which uses anonymous people-counting technology, responds to precise changes in room occupancy in real-time for optimal fresh air supply. Coupled with a full Building Operation System, it enables fast response time with no additional design, configuration or commissioning costs.
While monitoring occupancy in large spaces with multiple entrances and exits is a significant challenge in any closed environment, this advanced sensor provides significant value to hotels, offices, retail and real estate businesses, while making easier and more efficient the setup and implementation of the features by the system integrators.

Three core partners of Nanoelec –Schneider Electric, STMicroelectronics, and Lynred –, with scientific and technological inputs of CEA, Inria and UGA demonstrated a strong collaboration leveraging combined expertise and delivering this high-performance people-counting sensor. It gathers a strong mix of hardware and software options with the appropriate cybersecurity, reliability, and energy specifications. At the same time, Pulse/Nanoelec provided the technological platform to setup and test different configurations representative of the application context and to gather data exploring a range of suitable innovative solutions.
Integrating this work, Schneider Electric introduced in 2022 its Insight-Sensor. Consistently with the number of people in a room, the sensor informs the Building Operation System, which dynamically adjusts room ventilation, reacting quickly before conditions become uncomfortable. Conversely, the Sensor ensures that energy use for HVAC or lighting is reduced when rooms are at low or zero occupancy.

Principals of the anonymous people-counting technology
© Schneider Electric

Since 2015, the Nanoelec/Pulse program partners have been working on attendance monitoring in public areas using digital devices. Following this success and market introduction of the SpaceLogic™ Insight-Sensor, the collaboration is pursued within the program and would keep on delivering innovative and worldclass efficient products for building operation, leveraging the unique know-how gathered and shared between industry and research leaders within the framework of the IRT Nanoelec, combining electronics, AI, cybersecurity, and smart integration. ◆

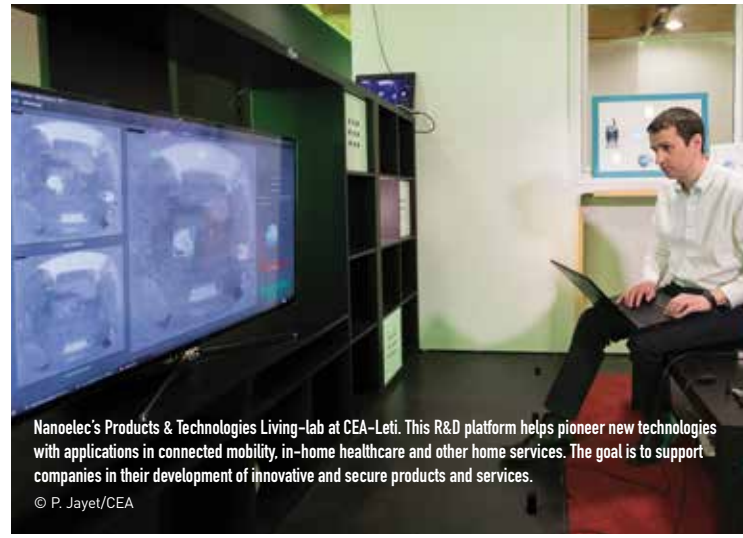
Demonstrator for monitoring occupancy in smart building
© Schneider Electric

Home & health cybersecurity

Data to preserve the autonomy of seniors

In 2021, teams from Université Grenoble-Alpes and the startup Cocoon Care, used the Product & Technology Living Lab (PTL) installed at CEA by Nanoelec to evaluate the technical performance of a fall detection solution to enable seniors to remain safely at home.

"We worked with healthy volunteers in realistic but controlled and standardized conditions" explains Laurent Adde, one of the founders of Cocoon Care. *"We are aiming to integrate the Wiser solution from Schneider Electric, a connected home automation and building management system. The results of this study are more than encouraging in terms of both sensitivity and specificity and were compared with the previous versions of the device and commercially available detectors to position this solution as a high-performance sensor."* ◆



Nanoelec's Products & Technologies Living-lab at CEA-Leti. This R&D platform helps pioneer new technologies with applications in connected mobility, in-home healthcare and other home services. The goal is to support companies in their development of innovative and secure products and services.
© P. Jayet/CEA

Christophe Villemazet, Head of laboratory for secure embedded systems at CEA-Leti and Deputy Director of the Nanoelec/Pulse Program is mounting a bed presence detection device on the "testbed" placed in an instrumented replica of a nursing home room at the Nanoelec/PTL.
© P. Jayet/CEA

Cocoon Care fall detection solution
© Cocon Care

Home & health cybersecurity

Reliable data transfer

"SecWay is a secure data gateway developed for medical applications, currently being transferred to become a reference solution in our product range", says Thierry Fensch, Director Innovation and Collaboration at STMicroelectronics Grenoble.

A first prototype of SecWay was finalized in 2021 within Nanoelec and a package design is currently underway with the teams at CEA/Y.Spot.

"SecWay is based on the STM32MP1 microprocessor adds Thierry Fensch. It is currently undergoing validation and is being made available for several European projects (GateKeeper, DigiFed, etc.) and industrial partners."

The prototype was produced using a security by design approach, relying on a system architecture based on secure electronic components (TrustZone, TPM). It incorporates software security building blocks to guarantee end-to-end security.

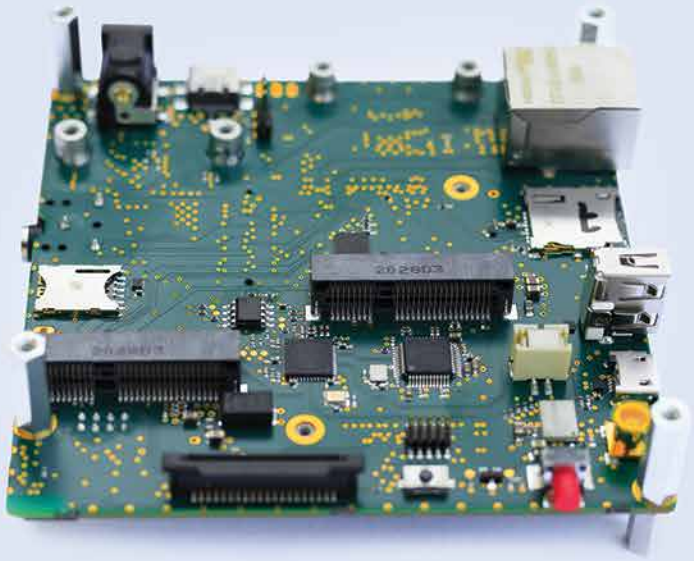
"We will be able to propose this application demonstrator to our partners and customers, in order to facilitate their R&D developments by giving access to our technologies within the framework of a complex system with embedded security", explains Thierry Fench. *"This new gateway also represents societal progress in the security of connected medical systems: it contributes to the monitoring of patients and homes and gives greater autonomy to elderly and fragile persons."* ◆

Packaging of SecWay protoype has been designed by CEA/Y.Spot

© P. Jayet/CEA

SecWay is a secure data gateway developed for medical applications

© P. Jayet/CEA



PULSE

Cybersecurity of industrial systems

In the event of an AI attack on embedded systems

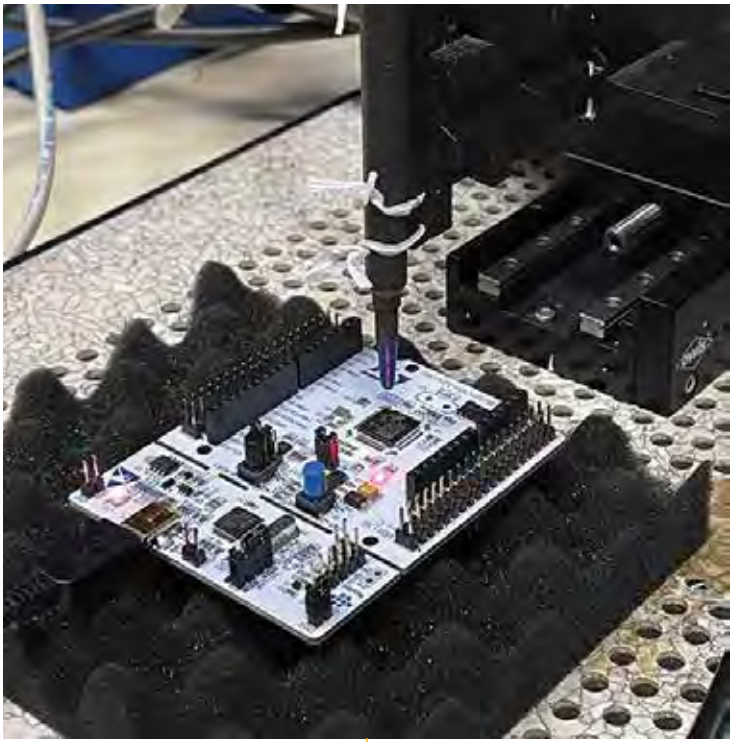
Utilization of Machine Learning algorithms, especially Deep Neural Network (DNN) models, is becoming a widely accepted standard in many areas, more particularly in IoT-based systems.

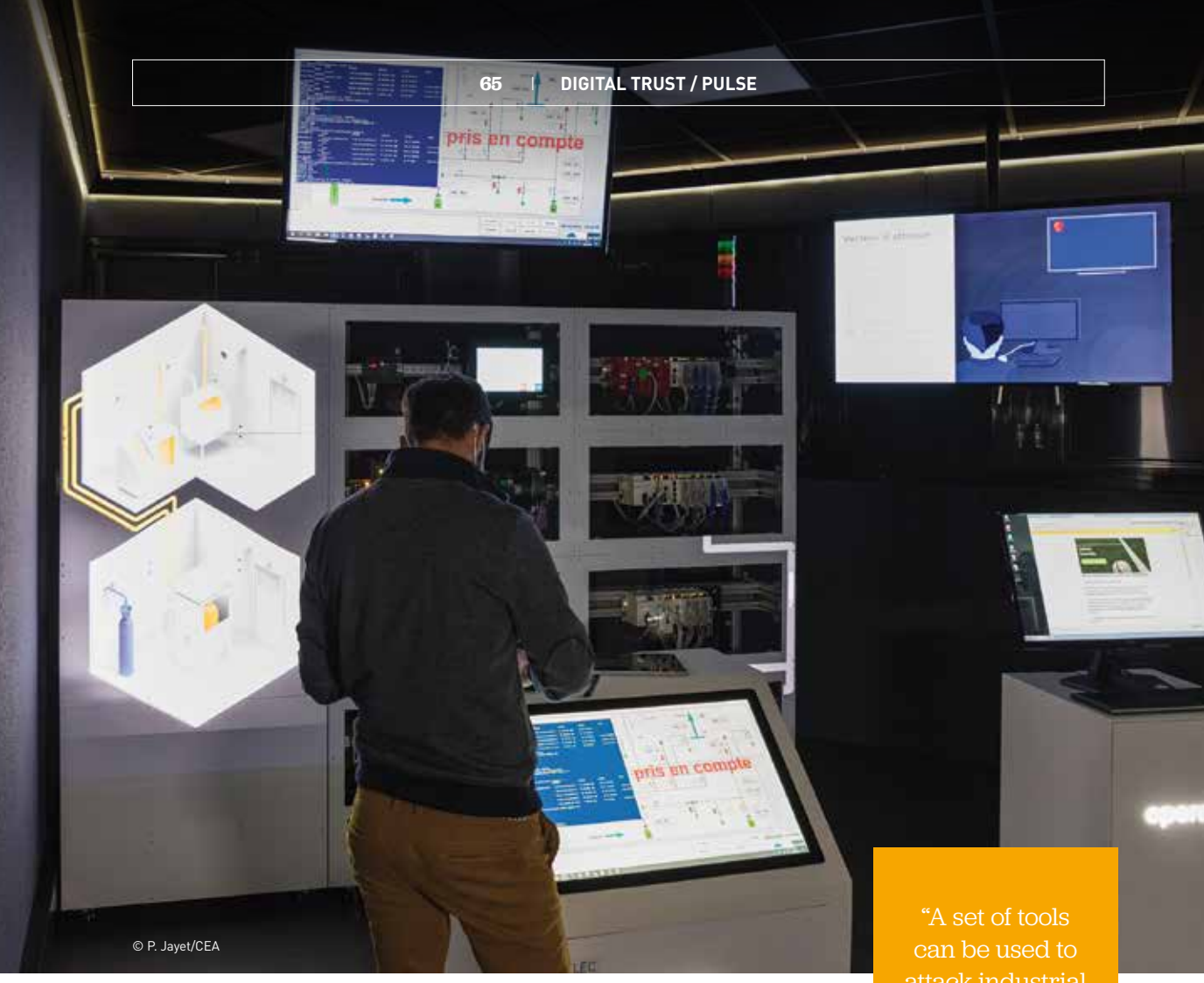
DNN models are achieving impressive performance in several sensitive fields such as medical diagnosis, smart transport or security threat detection, and represent a valuable piece of Intellectual Property. Over the past few years, a major trend has been the large-scale deployment of models in a wide variety of devices. However, this migration to embedded systems is slowing down because of the broad spectrum of attacks threatening the integrity, confidentiality and availability of embedded models. A research team from Mines St Etienne and CEA, supported by Nanoelec, produced a review of the state-of-art, covering the landscape of attacks targeting the confidentiality of embedded DNN models that may have a major impact on critical IoT systems, with particular focus on model extraction and data leakage. *"We highlight the fact that Side-Channel Analysis (SCA) is a relatively unexplored bias by which a model's confidentiality can be compromised. Input data, the architecture or parameters of a model can be extracted from power or electromagnetic observations, testifying to a real need from a security point of view"*, underlines Raphael Joud (CEA) who presented the study at the IEEE 7th World Forum on Internet of Things in July 21 in New Orleans, USA.

The risk of attacks is a growing concern for the security and artificial intelligence community, even if the majority of the works are limited to simulation efforts or do not take into consideration the characteristics of embedded models (e.g. low bit width parameters). *"Lessons could be learned from theoretical adversarial machine learning to better predict future advanced threats and design appropriate defense schemes"*, adds Mathieu Dumont (CEA) also involved in the review. ◆

TWO STUDIES PRESENTED BY RAPHAEL JOUD & AL. AND MATHIEU DUMONT & AL.
IEEE 7th World Forum on Internet of Things, 2021, July 14 New Orleans, Louisiana, USA.

Classic setup for electromagnetic emanations recording (target under test here is a Cortex M4 32-bit Microcontroller)
© CEA





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Cybersecurity of industrial systems

Hardware-in-the-loop platform for cybersecurity

"A new scenario around the Tennessee Eastman chemical process is under integration on the WonderICS platform and new attack scenarios are being carried out", explains Pierre-Henri Thevenon, cybersecurity engineer at CEA who coordinated the design of WonderICS.

The 'Tennessee Eastman' chemical process is a well-known physical process that simulates many typical characteristics of real-life complex industrial systems and processes.

The WonderICS platform - installed within Nanoelec at CEA at the end of 2020 - consists of a hardware-software co-simulation environment designed to alert the public and professionals to the cybersecurity threat to industrial control systems and experiment with innovative security solutions. The platform integrates simulators to emulate physical processes for different use cases such as hazardous gas management or hydroelectric power plants.

"A set of tools can be used to attack industrial control systems in different ways (phishing mails, corrupted USB key, hardware Trojan, etc.)." (...)

"A set of tools can be used to attack industrial control systems in different ways (phishing mails, corrupted USB key, hardware Trojan, etc.). Fortunately, we also demonstrate organizational and technical solutions that would have prevented this type of attack", comments Pierre-Henri Thevenon. ◆

PULSE

Safety of industrial robots

Safe and autonomous smart hoisting

Schneider Electric is looking to improve the control/command loops for its overhead cranes, for better compensation of cable slack and to obtain more precise positioning of the mass to be transported.

From a bridge crane to smart hoisting
© iStock/jordacheir

The system operates under in industrial conditions, therefore with considerable uncertainty, noise, disturbances and risks to the safety of people and property.

"We produced a digital cable model with 20 degrees of freedom, of the rigid multibody system type with or without axial deformation, along with a toolbox capable of performing sub-optimal calculation of the open loop and closed loop control gains. This enabled us to conduct preliminary comparison work between these numerous feedback algorithms", explains Bernard Brogliato, Director of research at Inria and manager of the project.

> "We produced a digital cable model with 20 degrees of freedom, of the rigid multibody system type with or without axial deformation" (...)

Once the theoretical models are established and proven, and the commands tested by digital simulation, a second phase should be able to study the integration of specific measurement sensors from STMicroelectronics (based on inertial units) to provide real-time data and improve the control/command loops.

"An overhead crane is an apparently common object and often seen as far from the cutting edge of innovation as it is such a common sight in industrial halls. Yet our problem is an acute one, because the trolley+cable system is one that it is significantly under-actuated: one, two, or three control inputs even though the cable has a large number of degrees of freedom, owing to its considerable flexibility. It is well-known in the automation world that commanding under-actuated mechanical systems is generally a difficult problem", explains Bernard Brogliato.

The goal of the project is to produce a safe and secure mobile robot demonstrator. ◆

The HistoTrust solution aims to be resilient, robust to software attacks and provide a high level of protection against side-channel attacks and fault injections.
©CEA

Safety of industrial robots

Digital Identity

Device- or user-centric system architectures allow everyone to manage their personal or confidential data.


©CEA

But how does one create the trust required to enable the stakeholders of a given ecosystem to work together, each protecting their own interests and their business? Developed by CEA-Leti under Nanoelec, the HistoTrust demonstrator was built in 2021. It introduces a solution to this problem: a system architecture separating the data belonging to each stakeholder and the cryptographic proofs (attestations) of their history shared in an Ethereum ledger. The designed solution aims to be resilient, robust to software attacks and provide a high level of protection against side-channel attacks and fault injections. Furthermore, the real-time constraints of an embedded industrial application are respected and integration of security measures does not affect performance during operation. ◆

©CEA

Safety of industrial robots

Implementing post-quantum cryptography

Post-Quantum Cryptography (PQC) is a field of technological research aiming to guarantee the security of information potentially threatened by attacks controlled by a quantum computer.

Within Nanoelec, researchers from CEA, UGA and STMicroelectronics have achieved a first level of optimization for implementation of a standardized post-quantum algorithm which has been acclaimed by the community (NIST competition). *"By comparison with the state-of-the-art in the public scientific literature, we are 40% to 60% more efficient in terms of computing time and with a memory footprint reduced by 70%"*, explains Antoine Loiseau (CEA-Leti) who is heading this work along with the STMicroelectronics, Diabeloop and Schneider Electric companies.

"Nanoelec enables us to anticipate the problem of the future deployment of PQC in our products, through dynamic exchanges and collaboration, notably with the academic partners UGA and CEA", states Bernard Kasser, Company Fellow & SRA Security R&D roadmap Director at STMicroelectronics.

"Nanoelec enables us to anticipate the problem of the future deployment of PQC in our products, through dynamic exchanges and collaboration" (...)

Antoine Loiseau also presented the results of the developments carried out within this framework, notably the performances obtained thanks to the optimization of the PQC implementation and a completely new side channel attack, at the 6th edition of the European Cyber Week (ECW2021), in November 2021. ◆

Safety of industrial robots

How can a blockchain help protect the digital identity of a person or company?

The French Ministry of the Interior and IRT Nanoelec with CEA and Thales publish a joint White Paper investigating the future prospects for Blockchain technology, notably with respect to Digital Identity management.*

Digital identity lies at the heart of trust in the digital economy: while it is essential in ensuring secure transactions, we know that the possession of users' personal data is also one of the bases of the economic model of the web giants. For its part, the State is permanently looking to adapt its identity ecosystems to the challenges of privacy protection, compliance with new anti-fraud regulations, as well as the prevention of theft and impersonation.

The concept of Self Sovereign Identity (SSI), sometimes referred to as "informational self-determination", is an interesting potential solution for meeting these challenges in the future. It is implemented by means of an intrinsically secure blockchain and could offer everyone the opportunity to possess and control the elements concerning the digitization of their identity attributes. This with no intervention from a body centralizing the data for access to a service, as demonstrated by the authors of the "Blockchain & identification numérique" (Blockchain and digital identity) White Paper published by the French Ministry of the Interior and IRT Nanoelec, with CEA and Thales, which came out in June 2021.

Even if the precise uses of this technology have yet to be defined, the White Paper helps define the possible outlines. It is thus a part of the essential prospecting work.

> "In many cases, the use of a blockchain in addition to other infrastructures [...] could help separate identification from authentication."

Through seven use cases, ranging from the production of unfalsifiable official personal documents to management of energy self-consumption in a joint

ownership building, the White Paper explores the answers that a blockchain could provide to the trust and facilitation questions created by the digitization of our daily lives.

The authors state that *"in many cases, the use of a blockchain in addition to other infrastructures [...] could help separate identification from authentication."*

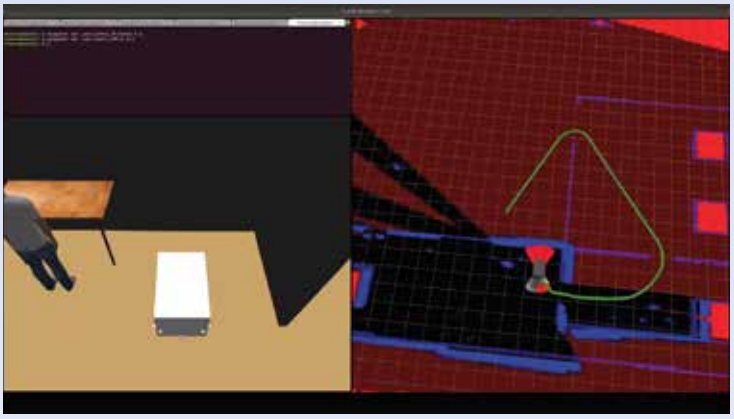
The White Paper suggests the joint implementation of a number of measures by the public authorities and private companies, with the assistance of standardization bodies and research centers. Its authors recommend an approach which could envisage blockchain qualification as a trusted service by the European authorities, in conjunction with the European Blockchain Services Infrastructure (EBSI) project. ◆

** Dated Oct. 2020, the document was published in 2021.*

Safety of industrial robots

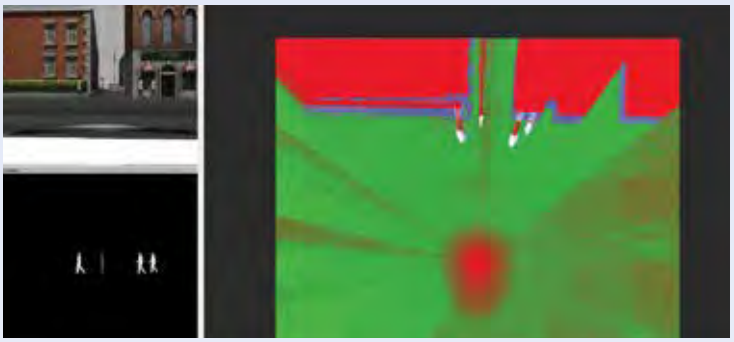
Industrial robotics security

To meet the ever-increasing need for flexibility and productivity in the industrial landscape, autonomous intelligent vehicles (AIV) are now integrated into production lines, enhanced by sensors deployed on the infrastructure.



For industrial robotics security, Inria worked under Nanoelec on planning and navigation through several rooms of the simulated environment.

© Inria



FResults from testing in a simulated environment for industrial robotics security project lead by Inria. The image shows a 2D representation of the 3D probabilistic semantic state grid generated from the fusion of the grid generated by lidars, and the grid generated by projection of the semantic image, before temporal filtering. The pedestrian occupancy is shown in white, the other occupancy is shown in blue, the free regions in green and the unknown regions in red.

© Inria

This mobile transitics introduce new risks in terms of safety of people and equipment. For a safe integration in the production line, in the midst of human employees, the stakes of technological developments are ever higher between sensors, AI and cybersecurity to avoid the machine any dangerous behavior.

The goal of the Industrial Robotics Security project carried out under Nanoelec/Pulse program is to develop, integrate and validate the technologies required to meet the needs of secure mobility in industrial logistics. Lead by Inria, the project integrates original technologies, software and expertise developed in previous Pulse projects, mainly in automotive contexts, the objective is twofold: to adapt these innovative technologies to this new context, while continuing their profound evolution.

In order to secure mobile AIV and their interactions with people and goods, the Industrial Robotics Security project studies embedded-and-collaborative systems-and-AI-methods for data-fusion, perception, localization, navigation, scene-understanding and decision-making, based on various techniques and new sensors of different costs and quality, redundant and distributed between mobiles and infrastructure, as well as their evaluation and validation.

All the sensors, along with a kinematic model of the prototype and a representative test-case environment, have been integrated in 2021 in simulation for hardware-in-the-loop validation of the embedded Inria perception-and-navigation system, having been adapted to these specific constraints. On the other hand, important technologies of data communication-and-fusion by VTX communication, as well as complex scene understanding by spatial semantic detection-and-filtering using AI and Bayesian Filtering have been developed and integrated in the Inria system.

Future work will focus on the integration and testing of these solutions on the physical prototype. ◆

Safety of industrial robots

SMEs and the Cross-Border Digital Innovation Hubs

DigiFed (an EU-funded project launched in 2020 for 3 years) is seeking to create the most impactful mechanism to aid the creation of value and a competitive edge for European SMEs and mid-caps.

Application Experiment AE is the main cascade funding pathway proposed by DigiFed that selects and finances SMEs and mid-caps for the development of CPS solutions based on existing or to-be-developed prototypes and products. A European team presented the evaluation results and success rate of collaborative projects (TWIN AE) against those originating from individual organizations (SINGLE AE) at the DigiFed application stage. The DigiFed consortium relies on a network of 12 Digital Innovation Hubs (DIHs) and Research Technology Organizations (RTOs) to design and experiment with novel innovation support mechanisms for SMEs across Europe. *"The three open calls conducted under DigiFed have created a balanced portfolio of AE types (21 SINGLE projects emerging from a single organization and 23 TWIN for collaborative projects)"*, explains Isabelle Chartier (CEA-Leti) who, within Nanoelec, coordinates the French node of DigiFed. *"The smaller companies (1-10 employees) had a consistently higher success rate in terms of proposal applications for TWIN AE. Equally, companies with a lower digitalization maturity level are more likely to apply for the collaborative AE (TWIN). It is also remarkable that AE appeals mainly to smaller companies, as 90% of applicants are <51 employees, and that large SMEs (51-3000 employees) only apply for TWIN AE, in which the tools foster collaboration between very small and mid-size SMEs."*

Through Nanoelec, CEA-Leti, ST-Microelectronics – in collaboration with the EasyPOC program from the Auvergne-Rhône-Alpes Regional authority – proposed the "Secure Platform for IoT" building block for open call AEs. Two projects that requested this block were selected for funding: Segway headed by Cysec, a Swiss cybersecurity SME, and Tracklog headed by NGS, an Italian SME focused on industrial monitoring and smart logistics. ◆

Three innovation support tools are povided to European companies within the framework of the EU DigiFed program. The French node is coordinated through Nanoelec.
© DR

MARGHERITA VOLPE, ISABELLE CHARTIER, ISABELLE DOR & AL.
EXPERIMENTATION OF CROSS-BORDER DIGITAL INNOVATION HUBS (DIHS) COOPERATION AND IMPACT ON SME SERVICES
PRO-VE Conference, St Etienne, November 2021

- EVENTS -

CSAW Europe contest with Nanoelec experts, brought together 104 students representing 35 European universities from 10 different countries
© Grenoble-INP

CYBERSECURITY AWARENESS WEEK

EVERY YEAR, NANOELEC SUPPORTS THE CYBERSECURITY AWARENESS WEEK SPONSORED IN EUROPE BY THE GRENOBLE-INP/ESISAR ENGINEER SCHOOL.

The 2021 edition of CSAW, the largest international academic cybersecurity competition, was held from November 10 to 14, 2021. The European edition was organized by Grenoble-INP/Esisar and the LCIS laboratory, with the support of Valence Romans Agglo and IRT Nanoelec. It brought together 104 finalists, all being students from 35 European universities and 10 different countries.

They faced each other in 3 competitions in front of a jury of 10 experts from industry and academia. *"For this 2021 edition, we have observed a significant increase in the level of students for the Embedded Security Challenge, a competition dealing specifically with hardware security issues, a very dynamic field in European universities"*, outlines David Hély (Grenoble-INP/UGA & now CEA-Leti) organizer of the event.

"The jury of the Applied Research competition once again praised the exceptional quality of the presentations made by the young researchers. The experts are already volunteering for the 2022 edition. Finally, we observed an undeniable increase in candidates participating in qualifying events in Europe, as well as greater commitment by universities to promote the participation of their students in the various finals (via press releases or on social networks). Interest in cybersecurity is not waning", David Hely comments. *"Students are very sensitive to cybersecurity issues and they are going down this route in increasing numbers."* ◆

David Hely (Grenoble-INP/Esisar) organizes the annual CSAW Europe contest with Nanoelec experts
© Patrick Gardin

- EVENTS -

TALKING ABOUT CYBERSECURITY

NANOELEC TEAMS PRESENTED THEIR LATEST DEVELOPMENTS IN INDUSTRIAL IOT SECURITY AT THE INTERNATIONAL CYBERSECURITY FORUM (SEPTEMBER 2021, LILLE) AND AT EUROPEAN CYBER WEEK (NOVEMBER 2021).

Nanoelec presented its work on Post-Quantum Cryptography (PQC) during a workshop devoted to PQC, during European Cyber Week (ECW), in November 2021. Post-quantum cryptography aims to guarantee the security of information in the face of with the threat of the quantum computer. These computers do not yet exist but PQC can be used to conceptually solve certain computing problems. One of the main problems is the threat of retroactive attacks on sensitive and critical information. Nanoelec is working on PQC algorithms selected within the NIST competition and is developing and optimizing their implementation on microcontrollers in terms of security and performance. The work done by Nanoelec in this field aims to provide security against physical attacks, in particular side-channel attacks, for components supporting PQC algorithms.

ECW brings together key research players, opinion leaders and companies from across Europe, in the strategic areas of cyberdefense, cybersecurity and artificial intelligence.

The Forum international de la cybersécurité (FIC – international cybersecurity forum) is the reference event in Europe for security and digital trust. The 2021 edition attracted more than 480 participants to four plenary sessions, 37 round-tables, 24 conferences, 35 technical demonstrations and 15 masterclasses. Two of these masterclasses were presented by experts from CEA-Leti working within Nanoelec: Olivier Savry presented the technological bases of a secure and sovereign processor, while Pierre-Alain Moellic detailed security issues and challenges when AI is integrated into connected objects. ◆

RISC-V WEEK

HELD ON-LINE BY NANOELEC, INRIA AND CEA, THE "RISC-V WEEK" UNDERLINED THE BENEFITS OF HARDWARE AND SOFTWARE CO-DESIGN AND OPEN SOURCE COLLABORATION.

For the 2021 edition, the event received 20 technical presentations and significant contributions from prominent personalities of our community, such as Prof. Gernot Heiser (UNSW Sidney), Prof. Luca Benini (ETHZ & Univ. Bologna), PhD Rishiyur S. Nikhil (Bluespec), PhD Gabriel L. Somlo (CERT/SEI, CMU) and Dominic Rizzo (Google). Close to 400 scientists from 33 countries (mainly Europe, India and Brazil) attended the various sessions. ◆

- KEY PUBLICATIONS -

Deception strategy for cybersecurity

A joint team from CEA and Mines Saint-Etienne is paving the way for a new approach to defend a remote system against malicious attacks, in which traps are set for the attacker. *"We explain the basics of our defense through the principle of the luring effect, inspired by the notion of robust and non-robust features, and experimentally justify its validity"*, says Rémi Bernhard, as first author of the review paper accepted at the IJCNN 21 conference.

"We propose a new approach to improve the robustness of a remote model against malicious attacks, inspired by the notion of robust and non-robust features. Our method is conceptually innovative as it exploits a new way of defending a remote system: presenting he adversary with various features that are less robust than those of the target model. Technically, it requires no retraining of the model, nor does it make assumptions about the way malicious attacks are designed, or rely on expensive test-time inference procedures."

RÉMI BERNHARD & AL.
LURING TRANSFERABLE ADVERSARIAL PERTURBATIONS FOR DEEP NEURAL NETWORKS
IJCNN 2021 (International Joint Conference on Neural Networks)

Blockchains, smart contracts, and complex sensors for hyper-connected smart cities

In a paper published in 'Computer' review in 2021, a pan-European research team including Mathieu Gallissot (CEA-Leti), within Nanoelec, demonstrated multiple points of innovation when combining blockchain technology with the Internet of Things (IoT) and security frameworks. "IoT products generate a lot of data and this is particularly true in the field of smart cities where they are deployed in large numbers, explains Mathieu Gallissot. Such a quantity of data leads to many challenges such as their ownership, their governance, their interoperability, their reliability and their security. Blockchain technology makes it possible to consider a new approach managing data from IoT products via the marketplace concept. This concept allows to exchange, or even monetize, data from sensors and the applications linked to them. Much of this functionality relies on the hardware security built into the devices to certify that the device from which a data originates is safe and has not been compromised by a hacker. It also enable to react when compromising are detected by putting suspicious data in quarantine and notifying automatically end users are soon as the attack is detected."

The specific marketplace is piloted through a cross-border trial between Santander and Fujisawa, in the context of the EU-Japan M-Sec project, thus validating the interoperability, efficiency, and data protection principles.

GEORGIOS PLAIKRASS & AL.
COMBINING BLOCKCHAINS, SMART CONTRACTS, AND COMPLEX SENSORS MANAGEMENT PLATFORM FOR HYPER-CONNECTED SMARTCITIES: AN IOT DATA MARKETPLACE USE CASE
Computer | October 2021

- KEY PUBLICATIONS -

Gait in patients with axial spondyloarthritis

Gait - the walking attitude- represents a fundamental human motor activity and allows for movement from place to place in daily life, and thus social participation. Assessing gait hence does offer undeniable prospects in a clinical setting. Gait outcomes can indeed advantageously be used to predict diverse outcomes including falls, cognitive decline, or mortality, and to quantify both pharmacological and non-pharmacological therapeutic interventions. To assess gait performance, wearable inertial sensors are now affordable and relatively easy to use. Wearable inertial sensors can be placed, for instance, on the trunk, shank, or feet to perform gait assessment in a corridor, using devices easily transportable between care units. Interestingly, wearable sensors do allow for the analysis of multiple gait cycles in longer distances than laboratory-based gait assessments, which could even be performed continuously in a patients' home in an ecological environment.

On the whole, results presented in Julie Soulard thesis highlight the benefits of using wearable inertial measurement units systems to assess gait parameters in ankylosing spondylitis. Julie demonstrated for the first time that assessing gait in patients with axial spondyloarthritis using foot-worn inertial sensors is feasible and suitable in clinical settings. Spatiotemporal gait parameters (such as stride length or cadence) are the most used parameters in clinical gait analysis and are easy to understand by both clinicians and patients. This work first show that foot-worn inertial sensors allow rapid and easy-to-perform computation of these relevant gait parameters at a low cost and without limitation of the testing environment. Our results further show that these gait parameters measured with foot-worn inertial sensors in patients with axial spondyloarthritis have good reliability in both single- and dual-task walking conditions.

Taken together, results obtained in this PhD suggest that integrating quantitative movement and gait analysis with wearable inertial measurement units systems for clinical assessments could be advantageous for clinicians to better understand movement-related disorders for better functional diagnosis, guidance of treatment planning, monitoring of disease progress, and tracking of recovery. In the near future, we can expect that smart clothes and e-textiles will be used to monitor gait and activities in daily life and permit clinicians to remotely monitor patients' conditions.

JULIE SOULARD
GAIT IN PATIENTS WITH AXIAL SPONDYLOARTHRITIS
Thesis defended at Grenoble-Alpes University in February 2021

LARGE SCALE INSTRUMENTS FOR CHARACTERIZATION

Large scale instruments for characterization program at a glance

VISION

Industrial users must be made aware of the unmatched performance of large-scale instruments for performing advanced characterizations of electronic components and devices.

AMBITION

Develop a competence center for testing radiation hardness of electronic components.

MISSION

Continue to make unique scientific instruments & methodologies available to serve the new challenges of the electronics industry.

PARTNERS

CEA
CNRS/LPSC
ESRF
ILL
Schneider Electric
Soitec
STMicroelectronics
IROC Technologies

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BY

ENNIO CAPRIA,
DEPUTY HEAD OF BUSINESS DEVELOPMENT AT ESRF AND DIRECTOR OF NANOELEC/ CARAC PROGRAM

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The Nanoelec characterization program gives industrial firms and researchers access to world-class tools to check the quality of their processes and to study the effects of ionizing radiation on components and systems. Thanks to the very high penetrating power of neutrons and X-rays, it is possible to do this non-destructively, without opening them or destroying them.
Ennio Capria, Program Director, sheds light on the issue.

2021 reveals a renewed and revitalized commitment to the Characterization program from the industrial partners. What have been the main actions?
STMicroelectronics ran a rich and varied program with us, on themes ranging from fine physical characterization with neutrons and synchrotron X-rays to the irradiation of hardened components. Soitec was able to conduct an ambitious structural characterization program for the development of an in-line methodology. With Schneider Electric we also established the concept of a rapid X-ray inspection instrument (FOR WHAT PURPOSE?). And the arrival of IROC Technologies, as a core partner in the IRT Nanoelec consortium, is a great sign of confidence for the ILL, particularly for the capabilities of its new Tenis irradiation station.

What do you feel is the most motivating aspect of the program for an industrial player?
Large instruments are offering unparalleled performance for advanced characterization of electronic objects. However, access to these instruments was designed for expert users, which is frequently the case among academic researchers, but less so among industrial users. We offer a range of services, from consultancy work to executing sample characterization experiments and analyzing data. Through us, industry can access cutting-edge characterization tools in service mode and in complete confidentiality. We also offer access to some of the world's most knowledgeable experts in the field of material characterization.

You are also broadening international collaboration for the program?
At the end of 2021, we became heavily involved in three European projects in the field of nanotechnology (NFFA Europe Pilot and NanoMECommons) and the irradiation of electronic components (RADNEXT). The existing synergies between the Characterization program and these EU projects will support expansion of the program abroad *(see Nanoelec in the EU chapter)*.

At the same time, you are still developing the Center of excellence in radiation hardness testing.
In recent months, four experimentation campaigns were carried out involving industrial partners. We are in particular looking to examine the emerging problem of loss of reliability which parallels ultimate miniaturization and complex packaging of electronic devices. The cause is the atmospheric radiation background noise present both at altitude and on the ground. The aim is to give our industry a competitive edge in the reliability sector. The large instruments are a very powerful means of measuring the sensitivity of new electronic technologies to ionizing radiation and neutrons, notably the atmospheric radiation background.

Is the Advanced Characterization Platform in Grenoble (PAC-G) still the point of entry to the set of standard services offered by the program?
The program is supporting technological developments at Nanoelec, in photonics, power electronics, smart imagers and displays. Thanks to the collaborative structure of Nanoelec, the academic and industrial research teams in the consortium have access to the characterization capabilities of the large instruments in order to develop new and wide-ranging methodologies.
And, for a broader community of users, the Advanced Characterization Platform in Grenoble (PAC-G) is helping to maximize the value of this work by making it accessible to the national and European industrial ecosystem. ◆

Manon Letiche preparing a sample for irradiation experiments on the Nanoelec neutron beamline called Tenis at the ILL. As a physicist, she runs most of the Nanoelec experiments on the ILL facility. She is also heavily involved in training courses for PhD students at Grenoble-Alpes University.
© P. Jayet/CEA

LARGE SCALE INSTRUMENTS FOR CHARACTERIZATION

A gateway to large-scale instruments dedicated to electronics industry needs

PAC-G is a dedicated gateway giving the electronics industry quick and easy access to some of the world's most advanced characterization facilities.

PAC-G also provides an extremely broad portfolio of individual but complementary characterization techniques. *"We are unique, offering a single, unified point of access to large-scale facilities such as synchrotron- and neutron-based sources through a cost-effective and rapid service tailored to innovation in electronics"*, says Caroline Boudou (ILL), senior scientist in charge of Nanoelec projects at ILL.

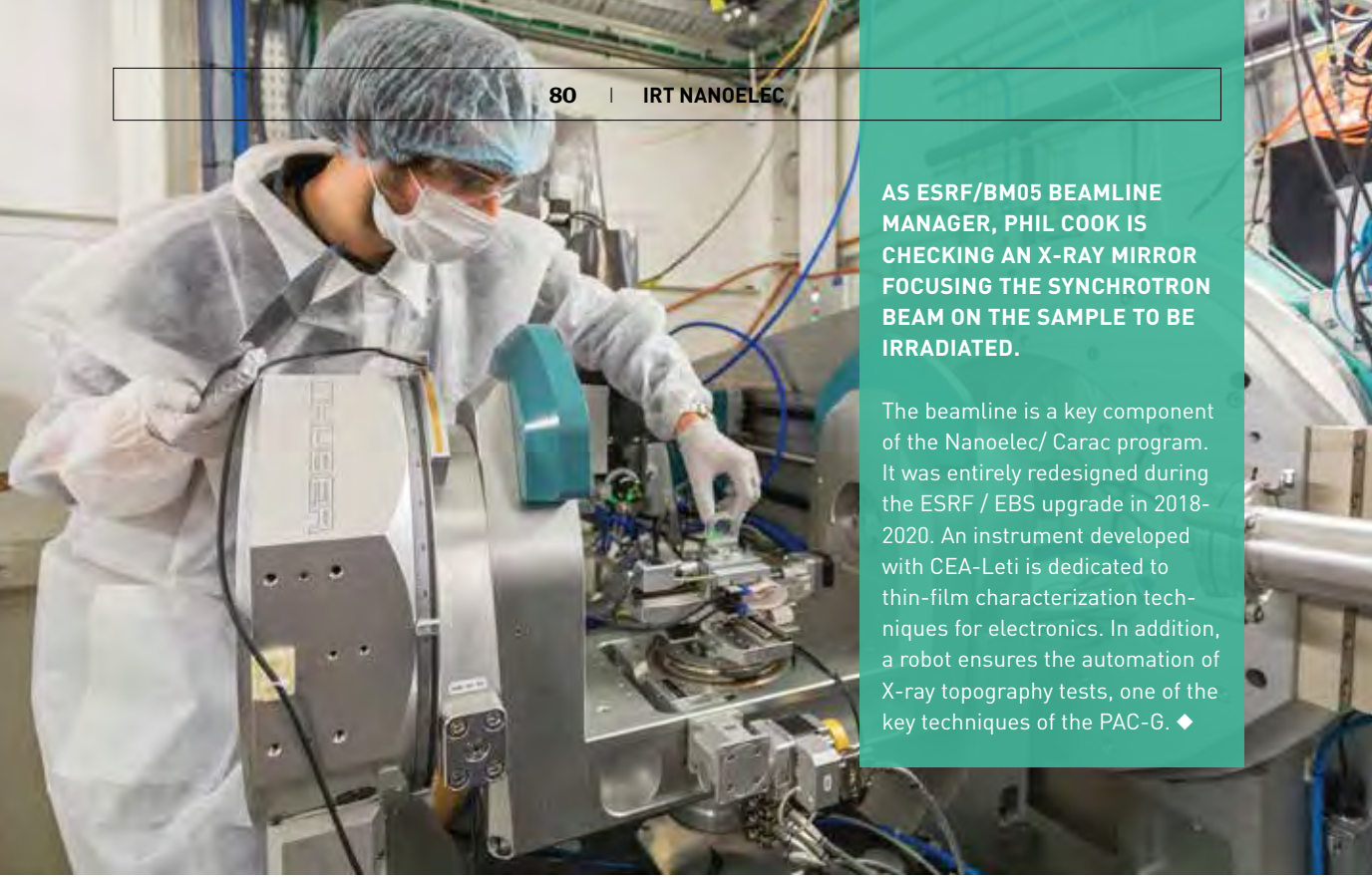
The TENIS irradiation station (ILL) has been operational since March 2021. TENIS has thus benefited from 129 days of operation of the high flux reactor at ILL. The station was used by industry and academics for 31 days of activity, representing 24% of the available time.

The TENIS irradiation station (ILL) has been operational since March 2021.

As regards Genesis (CNRS/LPCS), fifteen weeks were reserved during the course of the year for industrial customers in the field of electronic circuit irradiation, two weeks were reserved for the Tima laboratory and one week for an STMicroelectronics/Iter collaboration. Other weeks have been allocated for tests on particle detectors and one week has been allocated to the RADNEXT collaboration.

At the ESRF, the irradiation program is also ramping up. 2021 saw the start of the iLTP project, with experiments carried out by all the working groups involved, more specifically teams from the CNES, TRAD, Nucletude (Ariane-Group), Montpellier University, IRT Saint Exupéry and STMicroelectronics. The iLTP allows the users to request a long-term commitment from the ESRF in order to provide beamtime during up to six successive scheduling periods (three years). Scientific excellence is the primary criterion for the acceptance of such a Long-Term Proposal (LTP). ◆

PAC-G provides a single, unified point of access to large-scale facilities such as synchrotron- and neutron-based sources through a cost-effective and rapid service tailored to innovation in electronics.
© P. Jayet/CEA



AS ESRF/BM05 BEAMLINE MANAGER, PHIL COOK IS CHECKING AN X-RAY MIRROR FOCUSING THE SYNCHROTRON BEAM ON THE SAMPLE TO BE IRRADIATED.

The beamline is a key component of the Nanoelec/ Carac program. It was entirely redesigned during the ESRF / EBS upgrade in 2018-2020. An instrument developed with CEA-Leti is dedicated to thin-film characterization techniques for electronics. In addition, a robot ensures the automation of X-ray topography tests, one of the key techniques of the PAC-G. ◆

LARGE SCALE INSTRUMENTS FOR CHARACTERIZATION

XRF mapping of Phase Change Random Access Memories (PCRAM)

On ESRF/ID16B beamline, an experimental session conducted with STMicroelectronics verified the distribution of Ge, Sb and Te and their segregation in a ternary Ge-Sb-Te phase change material (PCM) during heat treatment.

"*The data were collected in situ with X-ray fluorescence (XRF) mapping, during annealing on ID16B light lines on PCM. They gave access to the elemental distribution (Ge, Sb, Te) in the material and to the segregation mechanisms*", explains Roberto Simola, engineer at STMicroelectronics.

The nano-fluorescence setup at ID16b was ideal in order to spatially detect the phase segregation in the PCM. However, because of stringent space constraints we had to use a dedicated mini-furnace where our sample was sitting on a 100 micron wide silicon nitride membrane. *"This implied preparing dedicated samples with small dimensions and thickness. It turned out that 30 microns width and 10 microns thickness were ideal and allowed us to follow the phase segregation during annealing"*, complete Roberto Simola. *"We appreciate the access to ID16B granted through the Nanoelec/PAC-G platform that has allowed us to prove the feasability of this experiment. Beamtime allowance for more systematic experiments should be made more easy thanks to this proof-of-concept experiment."* ◆

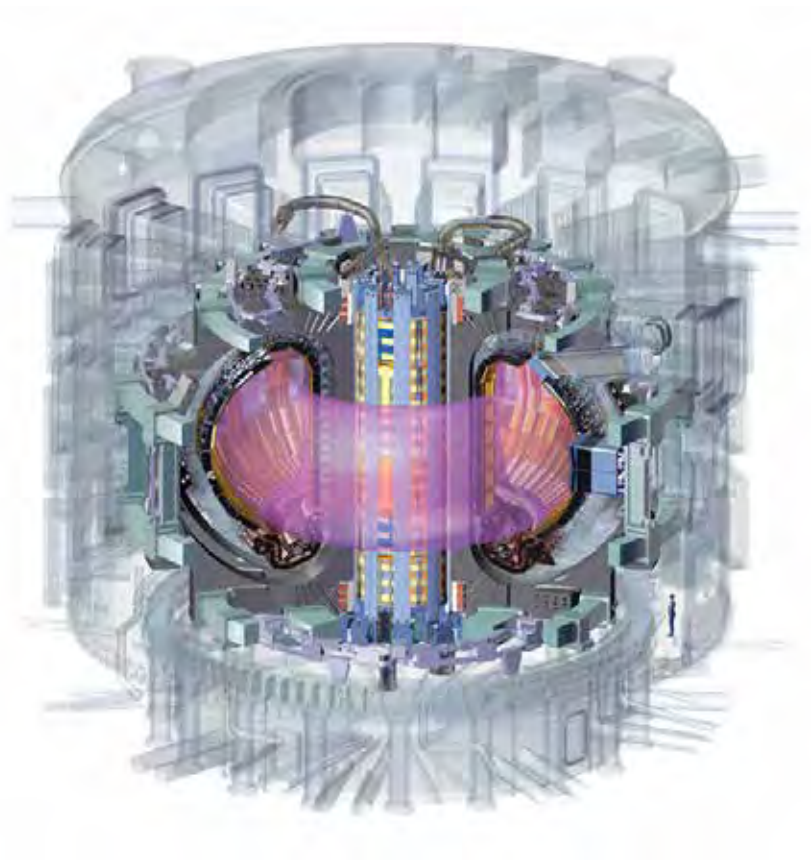
LARGE SCALE INSTRUMENTS FOR CHARACTERIZATION

Reliable electronics for fusion energy

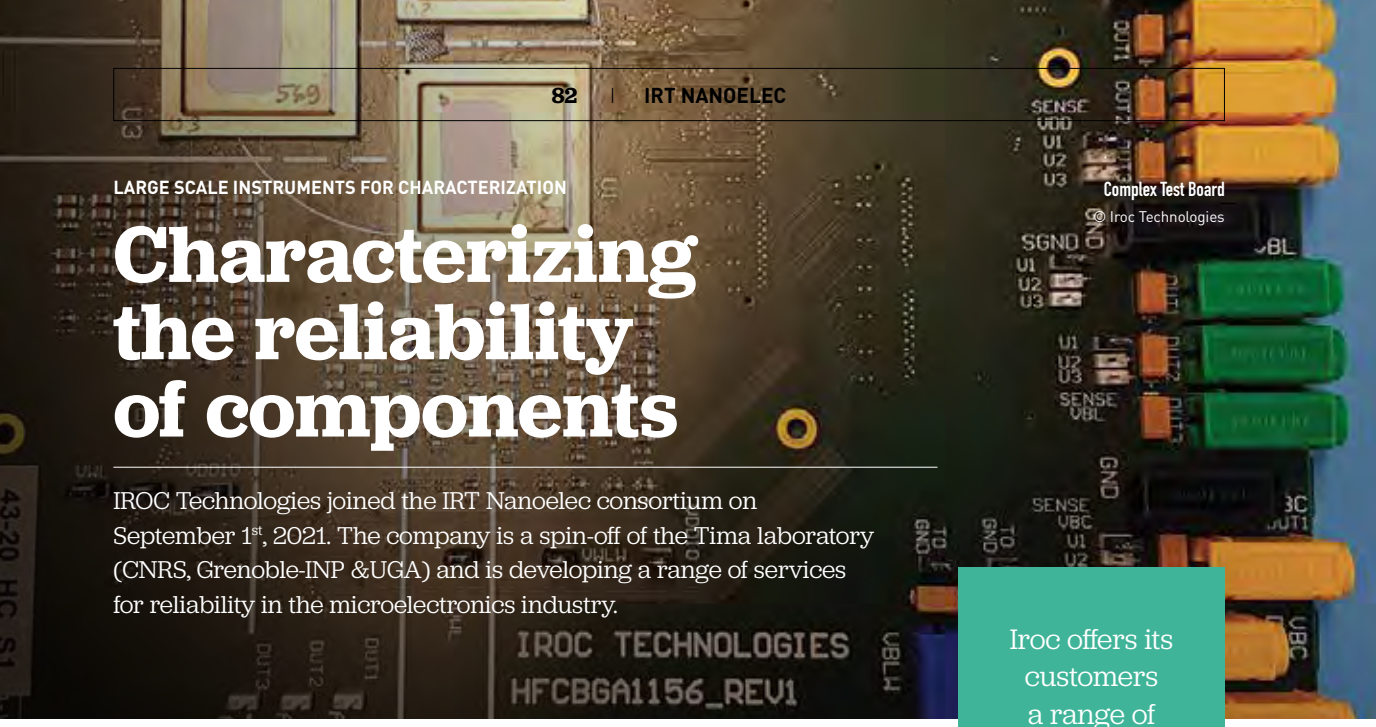
On the future tokamak at ITER, the world project for fusion energy, electronic components will be subject to a high flux of fast neutrons.

To prepare for such technology, STMicroelectronics ran experiments at WEST, the French fusion tokamak at CEA, to characterize neutron-induced errors in SRAMs. In addition to SEUs, unexpectedly high rates of MCUs were detected. Simulations indicated a possible contribution of 14 MeV neutrons from D-T processes, which was confirmed by irradiation of the same components at GENESIS (CNRS/LPSC). These results indicate the non-negligible impact of D-T neutrons in D-D fusion experiments on electronics in tokomak environments, despite their relatively low flux. ◆

Simulations indicated a possible contribution of 14 MeV neutrons from D-T processes, which was confirmed by irradiation of the same components at GENESIS (CNRS/LPSC)



On the future fusion tokamak at Iter, electronic components will be subjected to ultra-fast neutrons with energy of 14 Mev.
© ITER Organization



Complex Test Board
© Iroc Technologies

LARGE SCALE INSTRUMENTS FOR CHARACTERIZATION

Characterizing the reliability of components

IROC Technologies joined the IRT Nanoelec consortium on September 1st, 2021. The company is a spin-off of the Tima laboratory (CNRS, Grenoble-INP &UGA) and is developing a range of services for reliability in the microelectronics industry.

DAN ALEXANDRESCU,
CEO OF IROC TECHNOLOGIES, EXPLAINS THE CHALLENGES IN THIS FIELD, THE IROC APPROACH AND THE SHAPE OF ITS COLLABORATION WITHIN NANOELEC.

WHY IS RELIABILITY A KEY PARAMETER WHEN DEVELOPING COMPONENTS?

Defense and space have always needed special electronic components to carry out missions in harsh environments: radiation testing is in fact part of the military and space certification process. However, the constraints arising from the increasingly widespread use of components, for example in the aeronautics and automotive sectors, are increasingly strict if the dependability goals are to be met for critical equipment.

TO COUNTER THESE VULNERABILITIES, IROC TECHNOLOGIES IS PROVIDING THE CIRCUIT DESIGNERS WITH ANALYSIS SOFTWARE, SERVICES AND EXPERTISE TO IMPROVE THE QUALITY AND RELIABILITY OF COMPONENTS. WHAT IS YOUR APPROACH?

Iroc offers its customers a range of solutions for characterizing and verifying the level of reliability of electronic components before they are placed on the market. Accelerated test activities for electronic components account for 60% of the company's business.

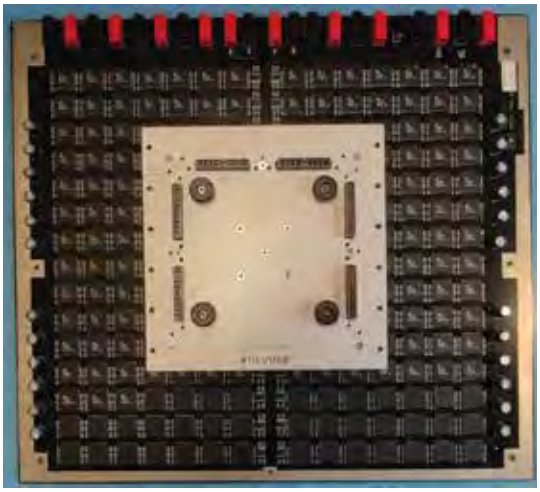
With regard to terrestrial and aeronautical applications, in order to obtain satisfactory predictions concerning the behavior of an electronic circuit, we are working together with laboratories which can provide a spectrum of neutrons similar to the atmospheric spectrum.

Iroc offers its customers a range of solutions for characterizing and verifying the level of reliability of electronic components before they are placed on the market.

AT NANOELEC, YOU INTEND TO WORK MORE SPECIFICALLY ON "SINGLE EVENT EFFECTS"? WHAT ARE THEY?

Single Event Effects (SEE) come from the interaction between an energetic particle and a microelectronic circuit. Ionizing particles or radiation can tear off or excite the electrons of the atoms of the material through which they pass. This disturbance can unexpectedly modify the operation of an electronic circuit. We aim to take part in expanding the expertise of the Nanoelec/Characterization program on the effects of irradiation, in particular if electronic components are affected by these SEEs.

The idea is to innovate by boosting R&D in this field. The aim is to improve the experimental resources and their performance and to develop analytical methods to predict the behavior of a circuit subjected to a neutronic environment, along with simulation tools.



Mega Test Board and Tester
© Iroc Technologies

YOU ARE AIMING IN PARTICULAR TO "QUALIFY" NANOELEC'S IRRADIATION RESOURCES FOR THE NEEDS OF YOUR CUSTOMERS?

We are preparing to qualify a selection of representative electronic circuits – static (SRAM) and dynamic (DRAM) memories, reconfigurable devices (FPGA) based on SRAM or FLASH, analog devices, etc. – for the operating environment. The results obtained will be corroborated by an in-depth analysis using prediction tools and nuclear databases developed by the company.

On the basis of the observations obtained with these tests, we will then propose prediction and simulation methods and tools. We will do this in collaboration with the other Nanoelec partners, because the Carac program brings together the key players in the value chain: the institutes operating large international instruments in Grenoble (ESRF, ILL), academic laboratories (CEA, CNRS) and industry (Schneider Electric, Soitec, STMicroelectronics). ◆

Device Under Test in a Vacuum Chamber during Heavy Ions Testing
© Iroc Technologies

LARGE SCALE INSTRUMENTS FOR CHARACTERIZATION

Education & training

Training design actions are being carried out in collaboration betweenthe characterization and human capital and training design (CHIF) programs at IRT nanoelec. they aim to promote the techniques developed by the carac program.

2021 saw the continuation and improvement of the 15-hour training module intended for 25 students from the EEATS physics and chemistry doctoral schools in Grenoble. This module was run remotely from January 11th to 15th, 2021.

The one-day "X-ray synchrotron and neutron techniques applied to microelectronics" module was created in 2020 and was given remotely for the Nano-Tech master's (about forty students). This one-day program comprises two introductory classes for synchrotron and neutron techniques, followed by an afternoon of tutorials on case studies. The Nanoelec/Chif program comprises a capsule which includes an analysis of nano-devices and materials in the field of nano-electronics through theory sequences (imaging, chemical analysis, study of surfaces and interfaces between materials, etc.), and illustrations with new case studies developed in 2021 on current research subjects conducted by laboratories in the field of nano-electronics. When preparing their thesis or in their last year of their master's, the students thus acquire a better understanding of how the properties of microelectronic devices can be studied at the nanometric scale and using large instruments.

Every year, the Carac program team also contributes at the ESONN' autumn school...

Every year, the Carac program team also intervenes at the ESONN' (European School On Nanoscience and Nanotechnologies) autumn school which hosts forty students. On August 27th, 2021, it ran the "X-ray synchrotron and neutron techniques applied to microelectronics" module. This 1h30 module comprises two short introductions to synchrotron and neutron techniques. ◆

- WORKSHOPS & CONFERENCES -

HIGH PERFORMANCE IMAGING

DEDICATED TO IMAGING TECHNIQUES, THE 8TH EDITION OF CARAC WAS HELD ON NOVEMBER 30, 2021. THIS YEAR, CLOSE TO 60 ATTENDEES HAD THE OPPORTUNITY TO TAKE PART IN A SET OF PRACTICE WORKSHOPS FOCUSED ON SELECTED HIGH PERFORMANCE TECHNIQUES (TOMOGRAPHY, CHEMICAL MAPPING, HIGH-RESOLUTION TOPOGRAPHY AND MORPHOLOGY...).

The Carac Symposium, supported by the Nanoelec/Characterization program and its associated PAC-G platform, is the annual event dedicated to characterization techniques for the electronics field and beyond. Characterization of new electronic components is essential to their design and ultimately to ensuring their reliability. The increasing complexity of electronic components and technologies, as well as the diversification of materials and manufacturing processes in the More-than-Moore approach require characterization that exceeds the performance of conventional laboratory equipment. To accurately correlate the micro and nanoscale characteristics of materials with the macroscopic properties of components, researchers need to gain in spatial resolution, detection capability and acquisition speed. This is why they use very specific beams of photons and neutrons from large instruments which are among the best in the world and are available on the scientific peninsula of Grenoble.
For the occasion, Alessandro Tengattini (ILL/UGA) reviewed the fundamental elements of neutron imaging, from the fundamental equations governing it, to neutron production and detection. He also provided an overview of the advanced techniques developed in recent years and an outlook of ongoing and future developments. "Neutron imaging is a powerful non-destructive method for probing matter in 3D, capable of tackling questions from a plethora of scientific areas. A host of advanced imaging techniques is also rapidly developing and is expanding the range of available contrast options, such as phase contrast, and polarized neutron imaging. Due to its non-destructive nature, it is possible to acquire multiple 3D volumes as the sample evolves, for example through chemo-thermo-hydro-mechanical loading, which in turn allows the spatio-temporally resolved quantification of processes. Recent technological developments even allow the simultaneous acquisition of highly complementary x-ray tomographies", explained Alessandro Tengattini.
Tutorials, abstract and full presentations of Carac'21 are available on irtnnanoelec.fr. ◆

RADIATION FACILITIES AND TESTING OF SEMICONDUCTOR DEVICES AND SYSTEMS FOR INDUSTRY

ON MAY 4TH, 2022 THE WORKSHOP G-RAD(NEXT) WAS DEDICATED TO RADIATION FACILITIES AND TESTING OF SEMICONDUCTOR DEVICES AND SYSTEMS FOR INDUSTRY.
This one-day event was held through a digital platform by ESRF and gathered between 60 and 80 industrial and academic experts.
The G-RAD(NEXT) technical sessions were organized around the main applications in the field of irradiation. Each technical session was organized as follows: first, a presentation by a representative of the industrial stakeholder group described the main challenges and perspectives. Then, a presentation of the most appropriate RADNEXT facilities to meet the needs of the user community. ◆

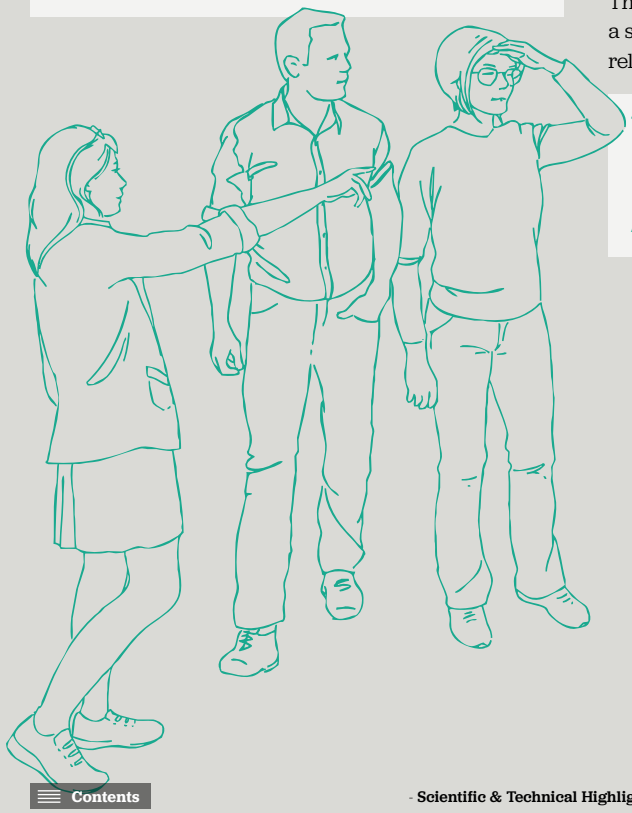
- KEY PUBLICATIONS -

Effects of Thermal Neutron Radiation on a Hardware-Implemented Machine Learning Algorithm

Hardware-implemented machine learning algorithms are finding their way into various fields, including safety-critical applications. These algorithms have to perform correctly even in harsh environmental conditions, such as in avionics at altitude.

Support Vector Machine (SVM) is an important Machine Learning that has been the target of hardware implementation in recent years. A scientific team from UGA, CNRS, Grenoble INP, Universidade Federal do Rio Grande do Sul, (Brazil) and Institut Laue-Langevin (ILL) published the very first work to assess both Binary and Multiclass SVMs under thermal neutron radiation, a type of particle noticeably present at high altitudes. At the ILL, they performed a fault injection campaign along with a radiation test with the D50 thermal neutron source. They demonstrated high intrinsic fault tolerance for both varieties of the SVM algorithm, especially for the Multiclass SVM.

MATHEUS GARAY TRINDADE & AL.
EFFECTS OF THERMAL NEUTRON RADIATION ON A HARDWARE-IMPLEMENTED MACHINE LEARNING ALGORITHM
Microelectronics Reliability, 2022



Modelizing the physics of defects on SiC substrates for power conversion

A scientific team from ESRF, Université Grenoble-Alpes and Soitec studied, using X-ray Bragg diffraction images, the long-range distortion field between parallel dislocations with opposite Burgers vectors in SiC substrates. *"Single crystals of silicon carbide are grown industrially for high-power electronic applications"*, reminds Thu Nhi Tran-Caliste (ESRF). *"And any defect on the substrate impacts immediately the performance of the final component."*

The experiment was carried out on the ID06-HXM beamline of the ESRF on a commercially produced 0.35 mm thick single crystal wafer of 4H-SiC.

"We were able to characterize this weak distortion field through Rocking Curve Imaging (RCI), a highly sensitive Bragg diffraction imaging technique using monochromatic synchrotron radiation. Deviations from the crystal matrix orientation are associated with the long-range distortion field around dislocations. This distortion field does not decay to zero but remains at an angle a between parallel dislocations with opposite Burgers vectors. We propose a simple model for this angular parameter a characterizing the distortion", explains Thu Nhi Tran-Caliste (ESRF). This model indicates that a should approximately vary as 1/D. This appears to be relatively well in line with the experimental data.

THU NHI TRAN-CALISTE & AL.
ROCKING CURVE IMAGING INVESTIGATION OF THE LONG-RANGE DISTORTION FIELD BETWEEN PARALLEL DISLOCATIONS WITH OPPOSITE BURGERS VECTORS
Applied Sciences

TECHNOLOGY DISSEMINATION

Promoting the adoption of emerging technologies in new application fields

© Morel/CEA

BY

ELVIR MUJIC (MINALOGIC) & **SANDRA TOCHON** (CEA) CO-DIRECTORS OF THE NANOELEC TECHNOLOGY DISSEMINATION PROGRAM.

As far as the digital transition is concerned, technologies and components are focused on few mass markets and companies sometimes lack the information and the in-house skills needed to integrate new technologies. However, these technologies are also opportunities to expand their offering and strengthen their commercial position.

With the Technology dissemination program, the partners in Nanoelec are promoting and accelerating the dissemination of emerging devices and new technologies in a variety of application fields; they are drawing more particularly on R&D skills in imaging, artificial intelligence, embedded software and electronic systems design.

The program includes two complementary initiatives:
• System Lab initiative exploit the components developed by the main partners involved in R&D programs at Nanoelec, primarily in the field of multi-modal, multisptectral imagers. New applications are being explored in different use cases.
• Easytech initiative, where advanced electronic blocks from IRT Nanaoelect programs are accessible to SMEs, startups and mid-cap businesses, including those whose core business is anything but digital. The aim is to enable them to take the digital transition on board, to increase the added value of their products or improve their manufacturing processes. ◆

Technology dissemination program at a glance

VISION
Sovereignty in the electronics industry requires efficient dissemination of innovative components and their adoption by national and European integrators and end-users.

AMBITION
To identify weak signals from the market and to accelerate the time to market of technologies developed by Nanoelec partners with fast prototyping and tests.

MISSION
• To help component manufacturers better understand the needs/possibilities of new applications
• To provide companies, notably SMEs, with information to plan ahead for the arrival of new technologies
• To contribute to the ambition of re-industrializing France and Europe.

PARTNERS
CEA
Minalogic
Grenoble-INP
Captronic/Jessica France
STMicroelectronics
Lynred
Prophesee
GEM

EASYTECH

Growing success with SMEs, mid-caps and start-ups

Established in 2012, the Nanoelec/Easytech initiative provides global support for SMEs, startups and mid-caps in their innovation process (creativity, expertise, R&D project). It is run by Minalogic, a global innovation cluster for digital technologies, supported by the Auvergne-Rhône-Alpes Region and local authorities.

© P. Jayet/CEA

ELVIR MUJIC
(MINALOGIC),
CO-DIRECTOR OF
THE TECHNOLOGY
DISSEMINATION
PROGRAM,
IN CHARGE OF
THE EASYTECH
INITIATIVE

YOU TOOK CHARGE OF THE PROGRAM IN 2021. WHAT HAS EASYTECH ACHIEVED SO FAR?

Easytech is attracting a diversity of companies. It offers a simple and easy fast-track for innovation projects. According to our survey, it is really valued by managers of small companies & startups as far as such companies do not necessarily have large R&D departments. 295 Easytech projects have been sponsored with more than 200 companies since 2012.

WHAT ARE THE PROFILES OF THE COMPANIES YOU TARGET?

We deal primarily with SMEs, a few mid-caps, startups and an even fewer number of large companies. Most of these companies are in the Auvergne-Rhône-Alpes region. Their core business is usually electronics but also sometimes maintenance and mechanics, instrumentation, materials, or other fields.Their application markets are highly diversified, ranging from space to health, to new modes of mobility, construction, sport and the agriculture+food industry and many other.

WHAT IS THE CONTRIBUTION OF LOCAL AUTHORITIES?

Like all IRTs, Nanoelec's main focus is not solely thematic, but also regional. This is why the local authorities top up funding for the Easytech projects. This helps bring down the financial risk for the local companies that innovate with us. First of all, the Auvergne-Rhône-Alpes region contributes 20% to the approved projects. Moreover, local authorities (mainly cities and urban areas) can add 10% for projects for SMEs based in their district. This is the case with Grenoble Alpes Métropole, Valence Romans Agglomération, Saint Etienne Métropole, Thonon Agglomération, La communauté du Pays Voironnais, Annemasse Agglomération, Clermont Auvergne Métropole. More than one quarter of our projects are also carried out with companies in other regions of France.

YOU NOW WANT TO TAKE BETTER ACCOUNT OF THE SOCIETAL AND ENVIRONMENTAL IMPACT OF THE INNOVATIONS DEVELOPED IN EASYTECH. HOW?

In 2021, we carried out a pilot experiment called Defi-Ino, in collaboration with Nanoelec and the ITE Ines.2S: we are looking to develop an environmental diagnostic offering for SMEs, mid-caps and startups wishing to work with us. Our priority is to help companies cope with environmental issues of public innovation policies and to provide them with competitive advantages. ◆

SYSTEM LAB

Time for new usages

System Lab was launched in 2020 and established as part of the Nanoelec Dissemination program in 2021. Y.Spot, the open innovation center at CEA, runs the initiative.

© P. Jayet/CEA

SANDRA TOCHON (CEA-Y.SPOT), CO-DIRECTOR OF THE TECHNOLOGY DISSEMINATION PROGRAM, IN CHARGE OF SYSTEM LAB, EXPLAINS

WHERE DID THE IDEA OF CREATING SYSTEM LAB COME FROM?

Together with our main industrial partners, we felt that it would be interesting to enhance Nanoelec's technology dissemination offering, by organizing a stronger and more direct link with the R&D programs. In the SystemLab initiative, we work with the component manufacturers, partners of the Nanoelec IRT, looking to explore new application fields.

WHAT IS THE CONCEPT?

We are exploring the use synergies between Nanoelec IRT R&D programs of new components provided by various partners and on approaches closely linked to the potential users. In the medium or long term, we will use the results of this process to expand or enrich the characteristics of our partners' components and generate opportunities for new technological routes.

SO WHAT IS THE APPROACH?

The System Lab partners share an open technical mock-up, methodologies to support open innovation processes combining creativity skills, exploitation of usage scenarios, value analysis. We created an open platform for use case explorations and evaluations based on multimodal and multispectral imagers. The components are supplied by our partners and we work on their integration at the system level including spatial and temporal coherence.

WHAT FIELDS ARE CONCERNED?

First of all, we work on the functions and services that can be introduced by multispectral imagers. We aim to seek out what has not yet been explored. This means that we have to take account of many additional technical aspects, such as AI, data security and fusion, and communication.

WHAT IS THE DRIVING FORCE BEHIND YOUR COORDINATION OF THE INITIATIVE?

System Lab is a new way of exploiting the technology that we engineers hold so dear. It creates a link between the largest possible number of players, from widely differing backgrounds and sectors. which means meeting committed and fascinating men and women, virtually every day.

We benefit from pathways already opened up by our colleagues in the open innovation team at CEA-Y.Spot. Their methods for leading workgroups and generating new designs are absolutely amazing. It's now up to me to organize and coordinate that for our partners!

WHAT FIELDS ARE CONCERNED?

The developments in System Lab can deal with component architectures, but also new functions (security, signal processing) or manufacturing processes needed for implementation of these innovations on the products. We work first of all on the functions and services that can be introduced by multispectral image sensors as well as data fusion. ◆

TECHNOLOGY DISSEMINATION

System Lab

A fictional startup to evaluate customer potential

To identify the usages for STMicroelectronics visible optical sensors, Lynred infrared optical sensors and Prophesee event-driven sensors, an energy-independent camera capable of transmitting a count or an alert in a scene has been designed..

© P. Jayet/CEA

The product presented as the reference for the fictional startup Advisia was used to query numerous potential users by email. Immediately, the product would appear to be of use for the surveillance of property and people and process quality control markets. ◆


Sébastien Balle, engineer, and Germain Magat, designer (CEA), are setting up the System Lab technical platform at the Y.Spot studiobox dedicated to Nanoelec
© P. Jayet/CEA

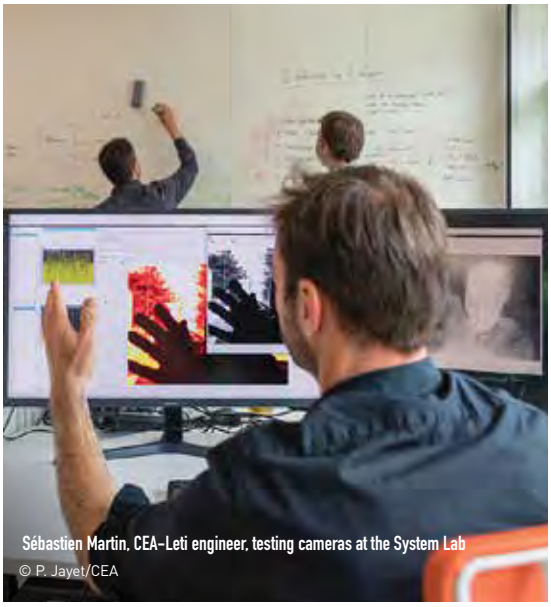
System Lab

An operational platform

Thanks to the provision of imagers from STMicroelectronics, Lynred and Prophesee as well as the development of interfacing software to ensure the spatial coherence and temporal synchronization of the sensors data, the System Lab was commissioned at the end of 2021.

It aims to prototype usage ideas for merging data from these multispectral sensors. The platform was presented to fifteen industrial firms and at the SIDO Paris fair and has already been the subject of discussion between experts on applications as diverse as gas leak detection, the creation of digital twins for buildings or waste sorting among other. ◆

© P. Jayet/CEA



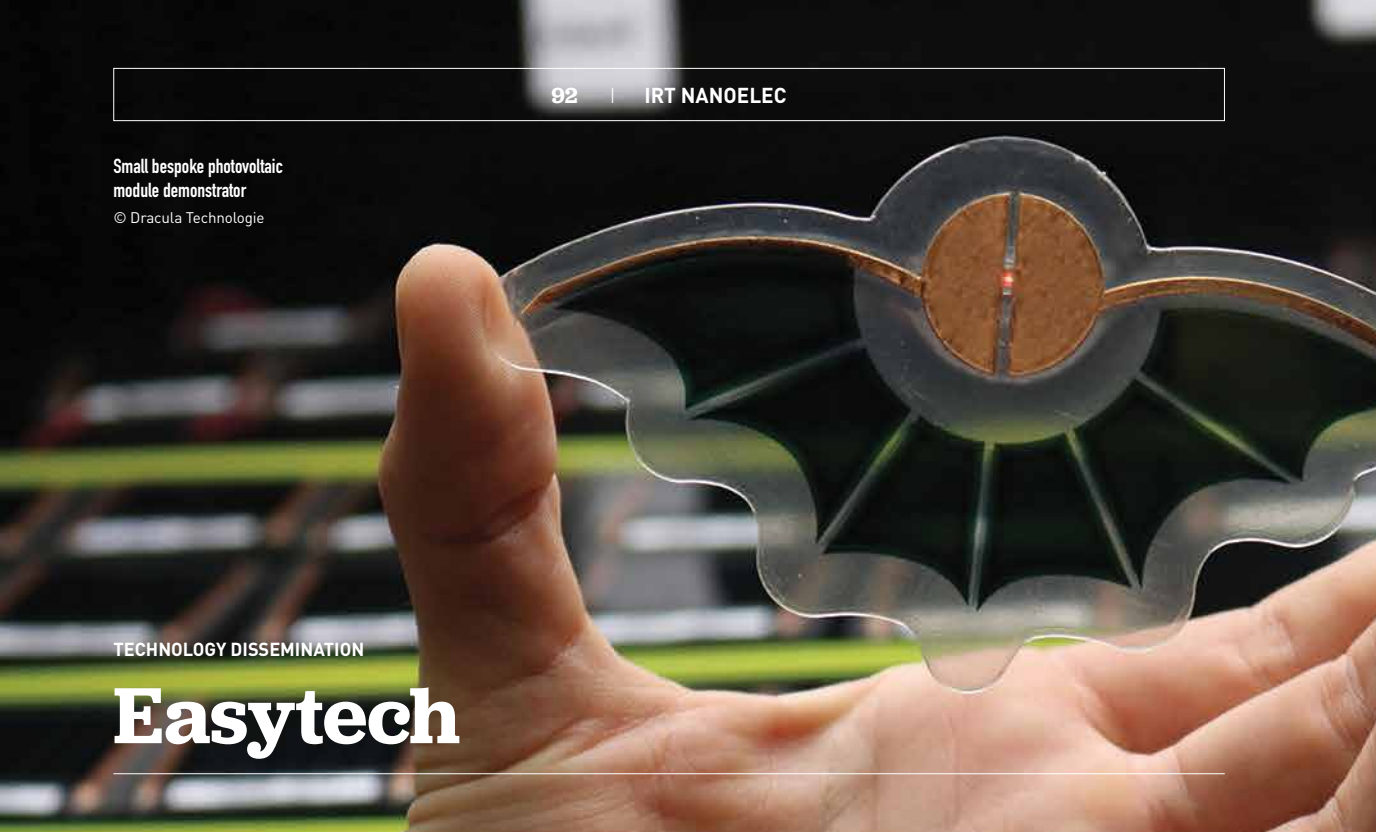
Sébastien Martin, CEA-Leti engineer, testing cameras at the System Lab
© P. Jayet/CEA

System lab

Launch of the open access platform

In collaboration with STMicroelectronics, Lynred, Prophesee and 4 institutional players -Minalogic, Captronic, CEA and Grenoble Business School (GEM)-, IRT Nanoelec has officially launched in 2021 the System Lab initiative to develop new imaging applications by combining the information from existing optical components.

The approach aims to close the gap between potential users and R&D actors in Optical Sensing to explore, anticipate, and conquer the challenges of tomorrow. ◆



Small bespoke photovoltaic module demonstrator

TECHNOLOGY DISSEMINATION

Easytech

Light energy for industrial connected objects

With Easytech, the Dracula Technologie company aims to bring down maintenance costs on industrial wireless sensors. This Deeptech start-up created in 2011 is developing "bespoke" flexible organic photovoltaic modules.

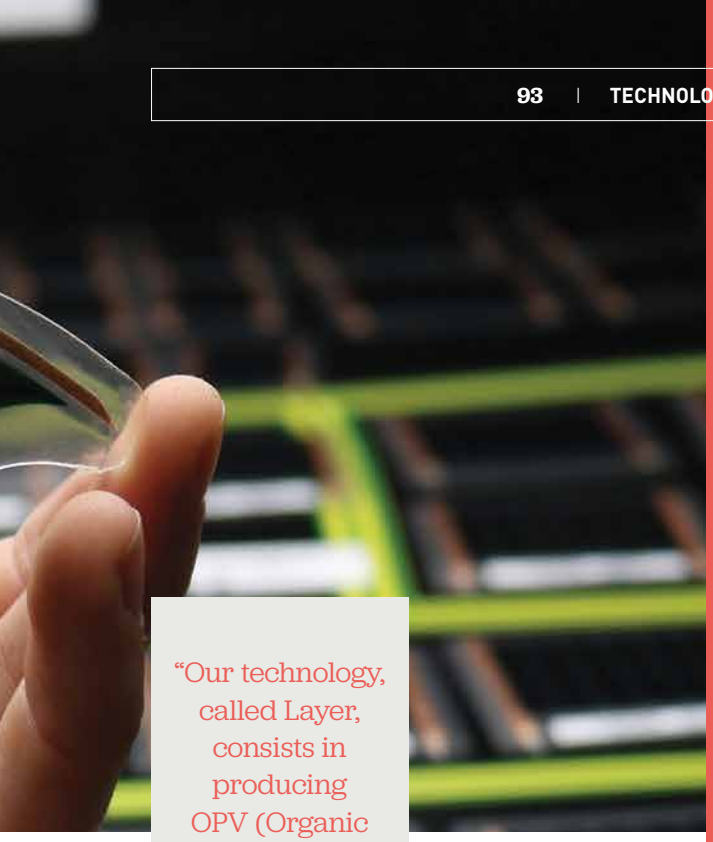
FIVE QUESTIONS FOR **BRICE CRUCHON,** THE COMPANY'S CEO.

YOU TURN LIGHT INTO ENERGY. WHAT ARE THE APPLICATIONS?
We are developing electrical power solutions using ambient light, for electronic objects requiring micro-power levels. Dracula Technologies is more specifically targeting industrial firms which need to digitize their processes, in which they have to use sensors at various stages. Supplying these sensors using ambient light helps limit the need for cells or batteries, thus bringing down maintenance times and cutting waste!

HOW DO YOU MAKE THE TRANSITION FROM THE WORLD OF DIGITAL PRINTING TO THAT OF THE IOT?
Our technology, called Layer, consists in producing OPV (Organic PhotoVoltaic) modules using inkjet digital printing techniques. We can thus create small bespoke photovoltaic modules to produce just the right amount of energy for a given application in a given light environment.

IS YOUR APPROACH FRUGAL?
We use very few materials to make our modules and pay close attention to the environmental and economic impact of our processes. Our solutions are also tailored to provide just what is needed for each application and are never over-sized.

IN 2022, WITH GRENOBLE-INP UNDER THE EASYTECH INITIATIVE, YOU ARE DEVELOPING A RAPID PROTOTYPING KIT. WHAT ARE YOU HOPING TO ACHIEVE?
Our core business is flexible photovoltaics. With Easytech, we obtained support from Grenoble-INP for the development of the management electronics for our photovoltaic panels. More specifically, we are aiming



"Our technology, called Layer, consists in producing OPV (Organic PhotoVoltaic) modules using inkjet digital printing techniques."

to develop a rapid prototyping platform with reusable technological building blocks: depending on a customer's specific needs, we will be able to propose a complete system tailored precisely to their requirements. We are working on a light sensor which will enable our Layer technology to be incorporated into a low-consumption electronic module, with the assembly being tested in the customer's various use scenarios.

YOU ALREADY WORKED WITHIN NANOELEC/EASYTECH IN 2014 AND 2019. WHAT DID YOU GAIN FROM THESE EXPERIENCES?

In the previous projects with Grenoble-INP, we were able to build up expertise and enhance our ability to develop the electronics needed to control our photovoltaic modules. We also demonstrated that by supplying an RFID tag with our small flexible photovoltaic sensors, we could increase the detection range by a factor of 4. We raised 2.4 million euros in 2019 to launch pre-industrialization of our module for this particular application. The performance gains are attracting the RFID tag manufacturers, with whom we are currently negotiating on various large applications markets. ◆

KEY FIGURES FOR EASYTECH

Under the Easytech initiative, with the support of the Auvergne-Rhône-Alpes region and local authorities, Nanoelec has accompanied more than 200 companies since 2012.

In 2021, we carried out a socio-economic impact study on **101 of these projects:** the analysis reveals that **more than 3 out of 4 projects** result in expanded activity after the Easytech phase and that it takes on average **2 years** for a project to enter the commercialization phase.

Easytech

Innovative prosthetics

Trinytec was created in 2018 and designs, builds and sells a range of bespoke prosthetics for patients having undergone amputations.

The company has developed expertise in the fields of biomechanics, materials and customized manufacturing. It is today moving towards mechatronics and connected prosthetics. Following two Easytech projects run at Grenoble-INP/Esisar, Trinytec validated the feasibility of its idea. The company decided to continue with development by hiring engineers and creating an R&D department within Trinytec devoted solely to the development and pre-industrialization of this system. A partnership was signed with three rehabilitation centers, so that a multicentric study can be carried out this year.

Trinytec took part in the pilot phase of Defi-Ino, a project for a rapid environmental and societal impact diagnostic carried out by Nanoelec and ITE Ines.2S in 2021. ◆

Trinytec designs, builds and sells a range of bespoke prosthetics for patients having undergone amputations

Following on from the Easytech project carried out in 2020/2021, Aryballe launched the marketing of its NeOse Advance odor sensor
© Aryballe

Easytech

Monitoring and characterizing odors

After an Easytech project carried out at CEA, Aryballe initiated in 2020 the transfer of the manufacturing process to a foundry to make a rapid transition to the product industrialization and marketing phase.

Aryballe's commercial strategy is today primarily focused on marketing an odor sensor utilizing this technology jointly developed with CEA. Aryballe Technologies raised 7 million euros in July 2020 to industrialize its electronic nose. In May 2021, following on from the Easytech project carried out in 2020/2021, Aryballe launched the marketing of its NeOse Advance odor sensor. During the year, Aryballe took part in the pilot phase of Defi-Ino, a project for a rapid environmental and societal impact diagnostic run by Nanoelec and ITE Ines.2S. ◆

Easytech

Management of natural environments

Scimabio Interface is a consulting company created in 2014 dedicated to the management of natural environments.

The company collaborates with various research institutes and aims to develop and provide managers with new tools and solutions for monitoring aquatic biodiversity, assessing river restoration, measuring ecological continuity and the conservation status of fish population in natural environments. *"To determine the franchisability of barriers to migration (dams, water intake, ...) generally equipped with fish passes, Scimabio supplies and installs two kinds of systems: videocounters with optical counting, and/or RFID tag readers"*, explains Alexandre Richard, General Director with Scimabio. *"After fish tagging using small chips called "PIT tags", the fishways are equipped with antennas connected to a tag reader. As existing solutions are expensive and not specific enough, the company has decided to produce its own PIT tag reader (fixed and mobile)."* This was made possible, in 2017-2019, by the Cap'tronic expertise within Nanoelec/Easytech. A new firm called Stream-Innov was then created to start marketing the readers in 2019, in France and abroad. ◆

Mobile tracking of fish using a mobile PIT tag reader in a river
© Scimabio

- TWO COMPANIES INCUBATED BY THE LINKSIUM TECHNOLOGY TRANSFER ACCELERATOR BENEFITED FROM EASYTECH PROJECTS IN 2021 -

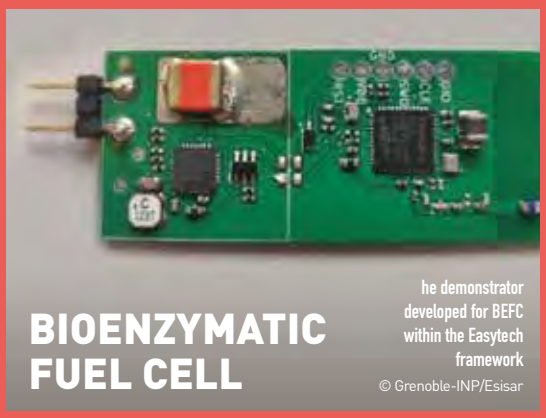
Linksium
technology transfer & startup building
Grenoble Alpes

The imager demonstrator developed at Grenoble-INP/Esisar for Nanobiose
© Grenoble-INP/Esisar

MORE EFFECTIVE EVALUATION OF HEALTH PRODUCTS

THE NANOBIOSE COMPANY FOUNDED IN 2016 NEAR CHAMBERY TARGETS CUSTOMERS IN THE PHARMACY, BIOTECHNOLOGY AND COSMETICS SECTORS.

"Today, 90% of the candidate drugs are rejected for reasons of toxicity and/or ineffectiveness, not detected in the early stages of R&D", says Damien Fleury, founder of Nanobiose. The company proposes an on-chip laboratory solution for earlier and more predictive evaluation of health products.
In 2021, an Easytech project run by Grenoble-INP/Esisar studied and developed two demonstrators, one for an incubator, the other for an imager. This should enable Nanobiose to propose a complete and coherent environment to its users, to facilitate and promote the use of its technology and thus the sale of its consumables. *"The demonstrators were used during a presentation day for our new range of instruments, and the concepts studied in the Easytech project are currently being industrialized"* explains Damien Fleury.
Nanobiose was incubated by the Linksium technology transfer accelerator (SATT). ◆



BIOENZYMATIC FUEL CELL

he demonstrator developed for BEFC within the Easytech framework
© Grenoble-INP/Esisar

BEFC IS A GRENOBLE STARTUP FOUNDED FOLLOWING DEVELOPMENT OF AN ECOLOGICAL FUEL CELL BASED ON PAPER AND ENZYMES CALLED BEFC (BIOENZYMATIC FUEL CELL).

This company thus produces biofuel cells based on paper, carbon and glucose. Their cells therefore aim to counter the problems of portability, toxicity or durability of energy sources for electronics in various fields (medical, logistics, etc.).
"We aim to carve out a position on the market for embedded liquid leak detection solutions. Our aim is to meet the growing need for embedded electronic devices requiring a low power but ultra-portable source (such as monitoring the transport conditions of a package, various applications in the medical field, etc.)", explains Alban Thierry, computing and electronics engineer at BEFC (Bioenzymatic Fuel Cells).
Under an Easytech project in 2021, the Grenoble-INP/Esisar students studied a power board and a wireless communication protocol and built a functional prototype / demonstrator. *"With this project, we now have the complete state of the art solutions we need"*, says Alban Thierry. *"We were able to test the best solution according to the context. Subsequently, we will continue with technological development on the two aspects."*
BEFC is incubated by the Linksium SATT. ◆

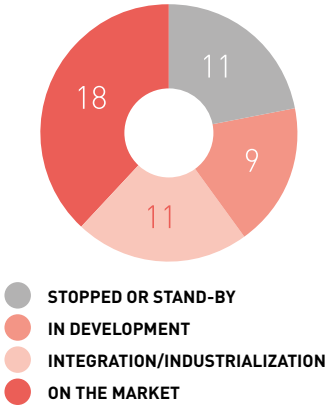
Easytech

An impactful initiative

An impact assessment was carried out in 2021 with a sample of 60 companies supported since 2012 by Nanoelec/Easytech. The Easytech system is acclaimed by the companies contacted, for its impact, the quality of the skills made available and the rapidity of the approval and contract awards process.

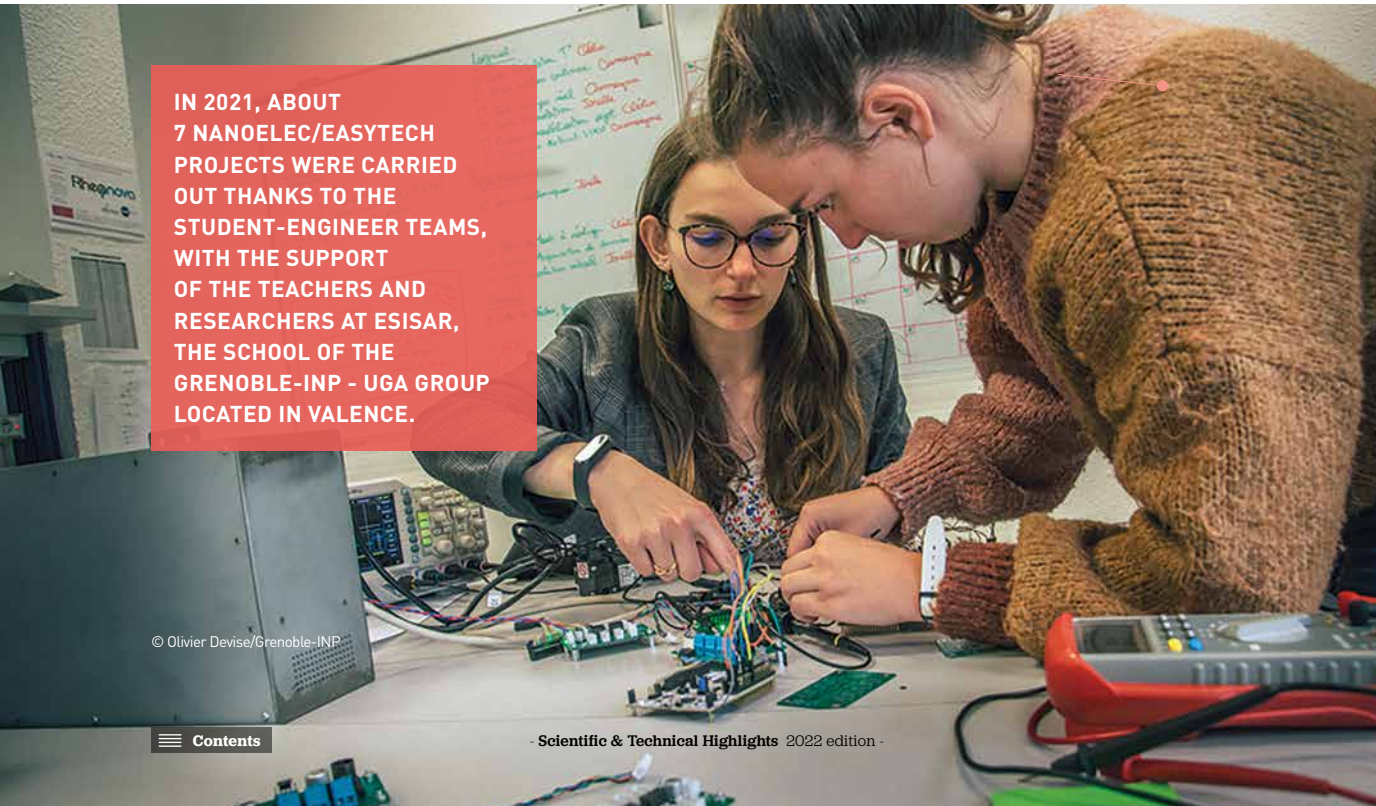
The core businesses of the companies in the sample are relatively concentrated: electronics, IT, instrumentation and maintenance/mechanics, account for 80%, but their application markets are far more diversified (health, mobility, building and construction, energy, culture, etc.). This confirms the pervasive nature of digital technologies across many areas of activity in society.

The typical company supported by Easytech is a small one (median of €1.3M in sales and workforce of 14). Three projects out of four are followed up and more than half reach the industrialization or marketing stage within 2 years. This result is far greater than expected and far greater than the figures generally obtained by technological innovation surveys.



The survey revealed that a very small proportion of the projects were not followed up. As shown in the graph besides, just over 20% of the projects were abandoned or placed on hold by the companies following their collaboration with Easytech. Nearly 40% of the projects analyzed are undergoing development or industrialization. Finally, more than 36% of these projects have led to commercialization or integration in the company process.

The median duration between the end of Easytech collaboration and commercialization (or integration) of the project, is 24 months. This is a short period of time in the field of technological research. Overall, following its Easytech project, the company passes a development milestone every year. ◆



IN 2021, ABOUT 7 NANOELEC/EASYTECH PROJECTS WERE CARRIED OUT THANKS TO THE STUDENT-ENGINEER TEAMS, WITH THE SUPPORT OF THE TEACHERS AND RESEARCHERS AT ESISAR, THE SCHOOL OF THE GRENOBLE-INP - UGA GROUP LOCATED IN VALENCE.

© Olivier Devise/Grenoble-INP

Easytech

Défi-Ino : designing an environmental and societal impact diagnostic for companies

As the trend in Europe and France towards the circular economy dips, sustainable innovation or "Eco-innovation" is becoming a key factor in competitiveness for companies. Nanoelec, in collaboration with ITE Ines.2s, is developing a flash diagnostic for the innovation projects run with SMEs, mid-caps and startups, under the Easytech initiative, run by Minalogic. Elise Monnier (CEA-Liten) and Peggy Zwolinsky (Grenoble-INP) coordinated the pilot phase in 2021 on behalf of IRT Nanoelec and ITE Ines.2s. They look back at the various aspects of this approach.

© DR

ELISE MONNIER
REFERENT-EXPERT IN ECO-INNOVATION & SUSTAINABILITY AT CEA-LITEN

© DR

PEGGY ZWOLINSKY
PROFESSOR AT GRENOBLE INP/UGA AND MEMBER OF THE G-SCOP LABORATORY (UGA & CNRS)

DEFI-INO IS A FLASH DIAGNOSTIC OF THE ENVIRONMENTAL AND SOCIETAL IMPACT OF AN INNOVATION PROJECT. HOW IS IT ORGANIZED?

Elise Monnier - At IRT Nanoelec and indeed at ITE Ines.2S, companies come along with a project aiming to integrate a new technology into a process, product or service. Defi-Ino aims to reinforce the project assessment and evaluation criteria. This is a flash diagnostic: it takes 1 day and costs about 1,000 euros. The company is interviewed by an expert who provides them with a confidential analysis of the weak and strong points of the project and its business model, in terms of its environmental and societal footprint.

Peggy Zwolinsky - In less than a full day of work, experts and members of the company management jointly identify possible routes for improvement to cope with eco-design requirements. This preliminary work can then be supplemented by a true eco-innovation approach focused on the project and the company, backed by public policy support for the circular economy.

YOU CARRIED OUT THE PILOT PHASE IN 2021. WERE THE COMPANIES CONVINCED?

Peggy Zwolinsky - 8 volunteer companies - 5 of which came through the Easytech initiative from IRT Nanoelec and 3 through Ines.2S - took part in this pilot phase. Their projects were analyzed by 4 categories of experts: two public laboratories (CEA, with its Liten institute and its collaborative innovation platform Y-Spot and Grenoble-INP, via its G-SCOP laboratory) and two private firms (Circulab and SolidCreativity).

Elise Monnier - The participating companies are urging us to continue with this initiative. Their feedback confirms that they know that eco-design, eco-innovation and the circular economy are now key factors in their competitiveness. This feedback also enables us to fine-tune the Défi-Ino offering to be designed and marketed , as several types of diagnostic have been tested.

PRECISELY, WHAT "TOOLS" DO THE COMPANIES CONSIDER TO BE MOST USEFUL?

Elise Monnier - The companies all agree that this face-to-face work outside the context of the company with a team of experts, but also with members of the team not directly involved in R&D (marketing, communication, finance, etc.) generates considerable added value. The brainstorming phases are all the more productive.

Peggy Zwolinsky - More "analytical" diagnostics also make an important contribution: they objectively confirm certain assumptions. For the companies, this is a guarantee of credibility and responsibility.

CAN DEFI-INO BE APPLIED TO ALL TYPES OF PROJECTS?

Peggy Zwolinsky - Prior to the diagnostic, it is worth questioning the technological maturity of the product and of the company itself with regard to eco-innovation. The diagnostic would appear to be vital for relatively immature products or companies with respect to the question of the societal and environmental impact. In the case of an established product, the diagnostic can also be of use if the company proves lacks expertise and resources in eco-innovation.

HOW DO COMPANIES ASSIMILATE THE APPROACH AND THE RESULTS?

Elise Monnier - Generally speaking, companies use this to improve how they communicate regarding their offering (with both customers and investors) and to open up new fields of innovation for their concepts. In the pilot phase, many extended the initiative in a variety of ways. For example, one of them now has an engineer who devotes 1 day a week to eco-design; another is focusing on the search for solutions concerning a point raised in the diagnostic: recycling; a third is now incorporating eco-design into its future projects.

Peggy Zwolinsky - This shows us that even with methods that differ from one project to another, the diagnostic, in all cases, acts as a catalyst for what comes after. Even for companies already aware of the social and economic aspects, for whom Défi-Ino brings credibility to the approach.

WHAT ARE THE KEYS TO A "WINNING" DIAGNOSTIC?

Peggy Zwolinsky - The auditor must have expertise in questions of sustainability and in the use of their tools, because the absence of data makes it hard to analyze a product or service lacking in maturity. This is all the more important because in one half-day it is possible to rapidly reach banal or even erroneous recommendations if the expert does not master the concepts of sustainable development and the diagnostic technique. Their high level of qualification helps to ensure that, although extremely fast, the diagnostic incorporates a "lifecycle" approach, provides a systemic vision, allows an understanding of impact transfers and, finally, provides a 360° overview of the three dimensions of sustainable development (economic, environmental, societal).

Elise Monnier - Moreover, in order to be efficient and effective, the approach must be "sponsored" at the optimum level of company governance. The personal convictions of the manager are decisive in ensuring that the flash diagnostic actually leads to tangible action. ◆


© Esisar

"For innovation, sustainable development is a criteria for competitiveness that is as strong as the purely economic impact"

The Defi-Ino experiment is based on an original idea from Bruno Ragué, former deputy director of Nanoelec and today Adviser to the managing director of CEA and a CEA director of ITE Ines.2S. *"For companies, explicitly and transparently taking account of the environmental and societal footprint of an innovation is a criterion for competitiveness that is as strong as its purely economic impact. Public financing sources now make their help for innovation dependent on information on the three areas of sustainable development (economic, environmental and social)"*, explains Bruno Ragué. *"Above all, environmental concerns give a sense of meaning to the persons involved and are a key factor in motivation. The Defi-Ino approach also makes it possible to imagine new types of products or services specifically tailored to the circular economy. All of this offers real added value for companies, with various types of benefits (attractiveness to young talent, investors, customers, etc.)."* ◆

HUMAN CAPITAL & TRAINING DESIGN

Sustainability as a driver of innovation

BY

SYLVIE BLANCO (PROFESSOR AT GEM) &
PANAGIOTA MORFOULI (PROFESSOR AT GRENOBLE-INP/UGA),
CO-DIRECTORS OF THE NANOELEC/ HUMAN CAPITAL
& TRAINING DESIGN PROGRAM

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Chif program at a glance

VISION
The competitiveness of the electronics sector is tied into the development of interdisciplinary, agile collaboration capacities.

AMBITION
Design and experiment with an integrative and customized learning and training design system that strengthens the human capital and the dynamic innovation capabilities of the institute and its academic and industry partners.

MISSION
Design and develop new training module contents and formats within three areas: fundamental skills, experience-based learning, learning communities to tackle emerging challenges.

PARTNERS
Grenoble-INP/UGA
GEM
STMicroelectronics
Schneider Electric

Competitiveness in the electronics sector is closely linked to the development of interdisciplinary and agile collaboration capacity within the R&D and production teams. The Nanoelec/Human Capital and Training Design program (Chif) supports this trend in skills evolution, the appearance of new trades and rapid market change. It also incorporates the need for a broader vision including the ability to interface with application sectors such as energy, health, or mobility, as well as the complexity of the value chain ranging from components to digital services.

2021 marks the start of the shared and collaborative Elise teaching design platform within the CHIF program. The question of the assimilation of this teaching material by all program stakeholders and beyond (academic and industrial establishments) rapidly appeared as a key success factor. This point led us to adopt an agile and iterative approach to the production and testing of content on all the work packages involving significant synergy with the partners, for co-construction of the content, in particular with Schneider Electric, which joined the program in 2021, and with STMicroelectronics, a program partner since 2018.
The work of the CHIF program enabled the design of modules linked to the scientific topics of the other Nanoelec programs or other academic structures (MIAI, Idex UGA) to be continued, but also in the fields of large instruments for characterization of materials, components and systems, cybersecurity, digital trust, or artificial intelligence. They supplement the modules relating to the dissemination of innovation (from creativity to business model) in the specific case of Nanoelec applications as well as the questions of eco-creativity and innovation culture for sustainable development by companies and society. ◆

HUMAN CAPITAL & TRAINING DESIGN

Collaborative access training resources

The teams engaged by GEM and Grenoble-INP within the Chif program are developing a *Learning Management System* (LMS) for on-line training resources in Nanoelec's strategic and priority areas.

The LMS will make the teaching material easily accessible to all the partners in the consortium wishing to take part in their design, testing, evaluation and utilization for operational training. At the same time, rigorous and pragmatic experience-based learning, agility and flexibility methods for the persons trained are being implemented through courses. *"For example, our 'Odyssey Design Technology (ODT)' course places the future managers trained at GEM in a situation as integrators-users of digital solutions such as those developed in the IRT. Another example is the PISTE course (standing for sober, technological and eco-responsible engineering) implemented at Grenoble-INP, which associates capacities such as a systemic vision of problems and impacts; creativity based on sobriety and sustainability as a priority, rather than growth-based approaches; analysis of the impacts of the solutions proposed, throughout their entire lifecycle; co-design of solutions"*, explains Maria Christou (Grenoble-INP), learning engineer for the CHIF program.

Access to the trainer resources will be via the ELISE training system, a platform that will integrate co-designed and remote access modules dedicated to Nanoelec's partners. ELISE comprises three fields, according to the "T-shaped " skills concept, thus ranging from technology to market: scientific and technical; market and innovation; cross-cutting skills (sustainable development agile projects, etc.). It targets a variety of profiles, including engineers and managers, for initial, professional and autonomous training and aims to accelerate production and facilitate the assimilation of learning material of use for a broad audience. ◆

Access to the trainer resources will be via the ELISE training system, a platform that will integrate co-designed and remote access modules dedicated to Nanoelec's partners.

Extracts from the capsule "Introduction to embedded artificial intelligence"

HUMAN CAPITAL & TRAINING DESIGN

Scientific and technical skills

Nanoelec/CHIF program introduces the students to embedded artificial intelligence and train them to discuss the limits of this technology.

Edge AI

In collaboration with the MIAI institute (Idex Université Grenoble-Alpes), the Nanoelec/CHIF program developed and digitalized the module entitled "Introduction to embedded artificial intelligence".

It introduces the students to embedded artificial intelligence (for example, image recognition, identification of audible keywords) and is able to qualify and quantify the limits of this technology.

During a session managed by a specialist in the method (Université Paris-Sorbonne), the ABCD – Activity Based Curriculum Design Learning approach – enabled the teams to identify the target learning goals, construct steps combining multiple activities and estimate the evaluation times and methods.

An "Embedded AI" video capsule is currently under development; it will comprise a script of learning sequences, videos and course material. The capsule will eventually be usable by an autonomous instructor, including within a company, for both in-person and/or remote settings. ◆

During the Schneider Electric Discovery Week in September 2021.
© Schneider Electric

HUMAN CAPITAL & TRAINING DESIGN

Markets, innovation and entrepreneurship

Voice of customer

The Schneider Electric R&D setup comprises a worldwide network of 'Customer labs', third-party locations where Schneider Electric utilizes its products in spaces recreating realistic environments, such as a hospital's electrical control panels.

> "In these 'labs', the aim is to gain a better understanding of the customer's problems and needs according to their profiles, following their pathway through innovation labs..."

In 2021, Schneider Electric joined the Nanoelec/CHIFprogram, because they were particularly interested in developing the notion of customer orientation in the upstream R&D and innovation phases. *"In these 'labs', the aim is to gain a better understanding of the customer's problems and needs according to their profiles, following their pathway through innovation labs: by interaction, by immersion, by the emotions in the face of innovative solutions, the teams can collect usage ideas, value arguments perceived by the customers, specific areas of expertise, while increasing customer satisfaction with the company as a whole"*, explains Nicolas Raynaud, Customer & Innovation Labs Director at Schneider Electric.

An experience-based learning path "Voice of the customer" was created and deployed in 2021 within Nanoelec, to be pursued in 2022. ◆

Markets, innovation and entrepreneurship

Towards collaborative innovation

In February 2022, at the initiative of GEM, 18 members of the CHIF program (experts from STMicroelectronics, Schneider Electric, AceWithYou Consulting, CEA and GEM) took part in an open and responsible innovation workshop coordinated by SoScience. For the participants, the aim was to take a fresh look at transverse collaboration methodologies.

The Future Of... (TFO)" methodology consists in taking the time to co-define the problem (collective work) which is to align industrial, scientific and societal issues. *"We are looking to mobilize a diverse range of experts, not only researchers and those from industry, who we ask to track weak signals from society and social entrepreneurs"*, says Julie Jouvencel, Managing Director of SoScience, a private office working on networking for open innovation & research, which is developing and implementing TFO. These actors together define a short-term action plan to validate the collaboration and together build tables of simple but multiple criteria to guide the choices to be made throughout the project: economic, societal, innovation, diversity of actors, and other impacts.

"The concept presented generated considerable debate within the group brought together by the CHIF program", says Julie Jouvencel, who also noted considerable enthusiasm *"regarding the commitment and collaboration by the various stakeholders"*. In parallel with this workshop, the Nanoelec/SystemLab initiative is contributing to the "TFO TEXTILES & FOOTWEAR RECYCLING" program coordinated by SoScience. ◆

HUMAN CAPITAL & TRAINING DESIGN

Transversal skills

Sustainable electronics for smart buildings

Once again in 2022, Nanoelec's Human Capital and Training Design program designed and implemented a new training module on sustainable electronics with the Grenoble Institute of Technology (Grenoble-INP) and Grenoble Ecole de Management (GEM). For two half-days, about 60 students at GEM and Grenoble-INP as well as Erasmus European exchange students, worked hand-in-hand with professionals from STMicroelectronics, Akileo Formation, with researchers from the French Alternative Energies and Atomic Energy Commission (CEA) and members of the Think What Matters association.

© P. Jayet/CEA

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PANAGIOTA MORFOULI, PROFESSOR AT GRENOBLE-INP AND CO-DIRECTOR OF NANOELEC/CHIF, REPORTS.

WHAT DESIGN CHALLENGES DO TRAINING PROGRAMS IN SUSTAINABLE ELECTRONICS INVOLVE?

Our students tell us that, more than ever, they are in search of meaning in their job; they are looking for jobs that make a real contribution to society. We must therefore adapt our training offers to this new demand. This is what we have been doing for the past

→

three years within the Nanoelec Human Capital and Training Design program: developing different modules that include a sustainable dimension.

WHAT ARE THE EXPECTATIONS OF YOUR INDUSTRIAL PARTNERS?

The microelectronics industry has a longstanding commitment to reducing its environmental impact across the entire lifecycle of products. Our partners are convinced that microelectronics engineers and managers must now take action at their own level, both as experts with highly specialized skills and as responsible citizens, to control the impact of technologies, create new "eco-friendly instincts" and help reduce humanity's environmental footprint in general.

THE MODULE ESSENTIALLY CONSISTS OF A 2-STEP WORKSHOP. WHAT IS THE OUTLINE OF THE EDUCATIONAL PROGRAM?

A first session sheds light on various technical aspects concerning the environmental impact of microelectronics. We are working on eco-design concepts through a method that consists of integrating environmental parameters into the design and implementation of a manufacturing process.

The workshop also aims to develop cross-cutting skills, for example by leading future engineers or managers to understand the complexity of the world and its scientific, ethical and political dimensions. This will enable them to become drivers of a real change in attitudes and behaviors by proposing new ways of approaching and working on the issues facing their company.

One month after the workshop, the group of six students who won first place was able to visit and truly appreciate the exhibition "1000+ Solutions for Cities"...

HOW ARE YOU INITIATING A REAL EDUCATIONAL CHANGE?

With this type of module, our students begin their semester by thinking about the future; they are encouraged to get involved as a driving force behind changes in the world. It's also an opportunity to work directly with industry experts who share their experience with them and guide them in their thinking for two half-days.

THIS WAS THE THIRD SESSION OF THE SUSTAINABLE MICROELECTRONICS WORKSHOP. WHAT ARE THE MAIN ELEMENTS?

After addressing the topic of a 'green' smartphone and its lifecycle in 2020 and 2021, the 2022 event was dedicated to IoT for smart buildings. The 54 students were split up into six groups and, with the help of our experts, each group worked on different technical subjects based on an initial scenario: transforming an office floor into a "smart floor" by using the IoT technologies to cut energy costs (while reducing the overall carbon footprint) and improving the safety and comfort of employees.

WHAT SURPRISED YOU IN THE FINAL OUTCOME OF THE WORK? WHAT STOOD OUT?

The students found themselves in the shoes of engineers and managers, faced with practical problems similar to those found in the real industrial world. We were struck by the quality of the discussions they had and the teamwork. They were highly motivated and committed, and they took a very pragmatic approach to the problems in order to design and implement real action plans.

WHAT HAPPENED AFTER THE WORKSHOP?

One month after the workshop, the group of six students who won first place was able to visit and truly appreciate the exhibition "1000+ Solutions for Cities" created by the Solar Impulse Foundation and Schneider Electric, focusing on the themes of energy, buildings, waste, production and consumption, mobility and infrastructure.

And as a result of the ideas that emerged during the workshop, a second group, very interested in the challenges of smart buildings and the contribution the microelectronics technology can make, decided to work throughout the entire semester on a project entitled "IoT for smart buildings", with the help of the start-up Akileo Formation.

HOW WILL THIS ACTIVITY SUBSEQUENTLY BE APPLIED?

We are going to continue this experience by involving more students from diverse backgrounds and possibly lengthen the duration of the workshop. This could allow more in-depth work and therefore ease the participants' frustration at not being able to take their thinking and ideas further. ◆

“This year, the module focused on the design of a smart, adaptable and connected building. Excerpt from the scenario: “You are employees of the company “Green IoT for smart buildings”.

Eric Jouseau (Akileo Formation)
© Grenoble -INP

With a view to the construction of a new office building, you must propose a prototype for the use of new technical services for management and for monitoring the occupancy rate (optimize room occupancy and the quality of the environment, anticipate energy consumption, etc.). You should integrate the use of artificial intelligence (AI) (powerful neural network embedded on a microcontroller) as much as possible in order to manage the IoT data (thermal, optical, chemical, etc. sensors)”.
“The direct feedback we get from the students is a real motivation for questions of sustainable development. Over and above the technical skills – because we are looking for colleagues – it’s their involvement in these problems of development, ecology and their ability to innovate in this field, to see environmental issues differently from the previous generation”.
Eric Jouseau, co-founder of Akileo Formation and AceWithYou, during the all-new session “Sustainable electronics/Smart building” of the Nanoelec/CHIF program in February 2022

“During their professional life, each of these students will be an environmental player. During this workshop, we showed them all the means and tools they will be able to use. We were able to see highly creative solutions, and this is also a very important point in terms of innovation. You have to “think outside the box” and reach out to all possible ideas in this field.”

Thierry Fench (STMicroelectronics)
© DR

Thierry Fensch, Innovation & Collaborations Director, STMicroelectronics Grenoble, during the all-new session “Sustainable electronics /Smart building” of the Nanoelec/CHIF program in February 2022. ◆

Transversal skills

The learning community now faces the emerging challenges of responsible microelectronics

Because the development of sustainable technologies is essential if our societies are to create a cleaner, safer and fairer world, a team headed by GEM, Grenoble INP - UGA with Idex Need for IOT, initiated dialogue on environmental and societal impacts of the electronics sector.

“*To do this, we proposed a jointly constructed, hybrid event for debate between various actors and experts from microelectronics, combining a challenge and a webinar. To discuss good practices in eco-design, we drew on the results of our eco-creativity challenge, during which fourteen multidisciplinary and multinational teams (professionals, academics, researchers, students) imagined the smartphone of tomorrow, using the Eco-Créanov serious game”*, says Manon Fourmanoir, Deputy Director of the CHIF program for Grenoble-INP/UGA until April 2022. The 14 teams came up with 110 original and responsible ideas, five of which were selected for the debate during the webinar entitled “Responsible microelectronics: what realities and good practices for sustainable transition” in the presence of 120 participants, in July 2021. ◆

Transversal skills

Designing a sustainable phone through a serious game approach

57 students from Grenoble-INP/Phelma and Grenoble Ecole de management (GEM) took part in a "Sustainable Electronics" workshop organized in February 21 by the CHIF program.

"*During the two sessions, the students worked in small groups, with the industrial and academic experts, with the aim of conducting an in-depth analysis of the design of a 'green' smartphone incorporating micro-electronic components designed in a spirit of sustainable development (greenphone)*", explains Panagiota Morfouli (Grenoble-INP).

The educational approach was devised and led by experts from CEA, STMicroelectronics, Grenoble INP (UGA), Time for the Planet and Grenoble Ecole de management, and prototyped within Nanoelec. At the beginning of the workshop, the students worked on the societal challenges of sustainable development from an industrial viewpoint, with STMicroelectronics, and from a legal and ethical viewpoint, with GEM. They used a brand-new serious game, called "My IoT" co-designed and co-produced by IRT Nanoelec & the cross-disciplinary program of Idex UGA, Need For IoT. ◆

Transversal skills

Society's digital challenges

Smart fiction, dystopia and societal challenges related to technology, in-person: this was the working program for the 700 first-year students of the Programme Grande Ecole de Grenoble Ecole de Management in September 2021.

In a futuristic world, our civilization has given itself over to excessive use of digital", this is the pitch for the adventure they were proposed for the 2021 back to school challenge.

"Through the enthusiastic presentations of their projects, our students demonstrate keen interest in innovations and transitions with a high technological content. They also demonstrate a significant societal engagement", notes Fédérico Pigni, Dean of the faculty of Grenoble-Ecole de management.

This totally unprecedented immersive course imagined by the innovation and learning teams at GEM was developed with the assistance of the Nanoelec/Human Capital & Training Design program.

"By reinforcing our connections with the ecosystem of research, the microelectronics industry and the digital world in general, Nanoelec's Human Capital and Training Design program contributes to expanding our students' perspective regarding the impacts of the digital world on the real world", adds Fédérico Pigni.

The students thus learned to explore and study the hidden face of 18 day-to-day connected objects, service or practices (smart pacemakers, or delivery drones for example) expressed in the form of a controversy concerning one of the following 6 main fields: health, sport & wellbeing / smart building / mobility & transport / hybrid working / urban space / customer pathway. As future managers, their work aimed to design initiatives to encourage awareness, action or inspiration around digital usages, as well as to communicate them via various formats such as podcasts. ◆

A podcast recording session during the GEM back to school challenge 2021, supported by Nanoelec/Human Capital & Training design program
© GEM

Workshop based on the Supply Story serious game created by Grenoble-INP/UGA with the Nanoelec/Human capital & Training Design program. The RnDyneo module developed in 2018-2019 by the partners of the program, deals with the agile behavior of R&D teams at STMicroelectronics involved in transverse projects, following on from the action taken by the company with its Manufacturing teams. Based on the principle of a serious game, the Supply Chain module is aimed at continuing professional training of industry personnel as well as initial training of engineers and international masters.

HUMAN CAPITAL & TRAINING DESIGN

Serious games

Silo Story & Supply Story

Agility of R&D teams and agility on the market

At the initiative of STMicroelectronics, the RnDyneo training course was developed to enhance the agility, innovation, accountability and collaborative work of R&D teams in an increasingly complex environment.

In he need for innovative learning on emerging behavioral subjects (the agile mindset in an R&D team) addressing international audiences and multi-site teams, but also the health crisis, led to the development of autonomous remote training capsules lasting a maximum of four hours, including quizzes and a digital version of the "Silo Story" serious game.

"After the success of the in-person RnDyneo training, the digital version was a must for our local teams during the pandemic, but also to ensure involvement of our remote sites", says Thierry Fensch, Innovation & Collaborations Director and STMicroelectronics representative on the Nanoelec/CHIF program. *"Even with less direct interactions during simulations, the learning teams at Grenoble INP and GEM were able to retain the essence of this active leap into the heart of "lean" behaviors in R&D activities. The dissemination of this new program has begun with the ST teams and this adaptation is very welcome. As with the original RnDyneo, we are counting on this version to encourage effective and appropriate behaviors in our organizations, in a spirit of cooperation, learning and development of our employees."*

Like Silo Story, the Supply Story serious game tackles questions of team agility, no longer from the viewpoint of transverse collaboration within the project teams, but rather that of business streams.

The main learning goals of "Supply Story" are to develop the skills of the participants by making them aware of the complementarity between the quality of customer/supplier collaboration and the quality of in-house collaboration within the company. Complementarity in the customer-supplier relationship, from motivation factors to health factors designed to avoid dissatisfaction, is also examined.

The game involves 7 to 12 players. It is a role-playing game with two customers manufacturing taxi-drones, 2 tier-1 battery suppliers and one tier-2 service provider. Within a limited time, the customer must provide the best response for a market. ◆

My IOT
© P. Jayet/CEA

Serious game

My IOT

A smartphone lifecycle and its environmental impact

My IoT is a discovery serious game created by the CHIF/Nanoelec program and the Need for IoT project (Idex Grenoble-Alpes University).

The game is a support for interactive sessions with students & professionals involved in electronics design and fabrication. This game invites participants to take a bird's eye view of the electronic industry, and playfully discover each stage in the lifecycle of a product and the associated ecological & social impacts using a flagship application; the smartphone. Through dialogue in breakout groups, participants share their knowledge to create the green smartphone lifecycle. Next, they match illustrated impact cards to each phase of the lifecycle: from mining the minerals needed, to the manufacturing process, distribution, retail & brand marketing, to recycling.

"This collaborative game aims to raise awareness and initiate a change in mentalities and behaviors regarding the impacts of the globalized micro and nanotechnology industry in an accessible, innovative and engaging way", explains Laetitia Thomas, pedagogical engineer at UGA and designer of the tool. *"After having been made aware of the various impacts of the IoT supply chain, participants together create possible solutions in line with circular economy goals."* ◆

Creanov
© GEM

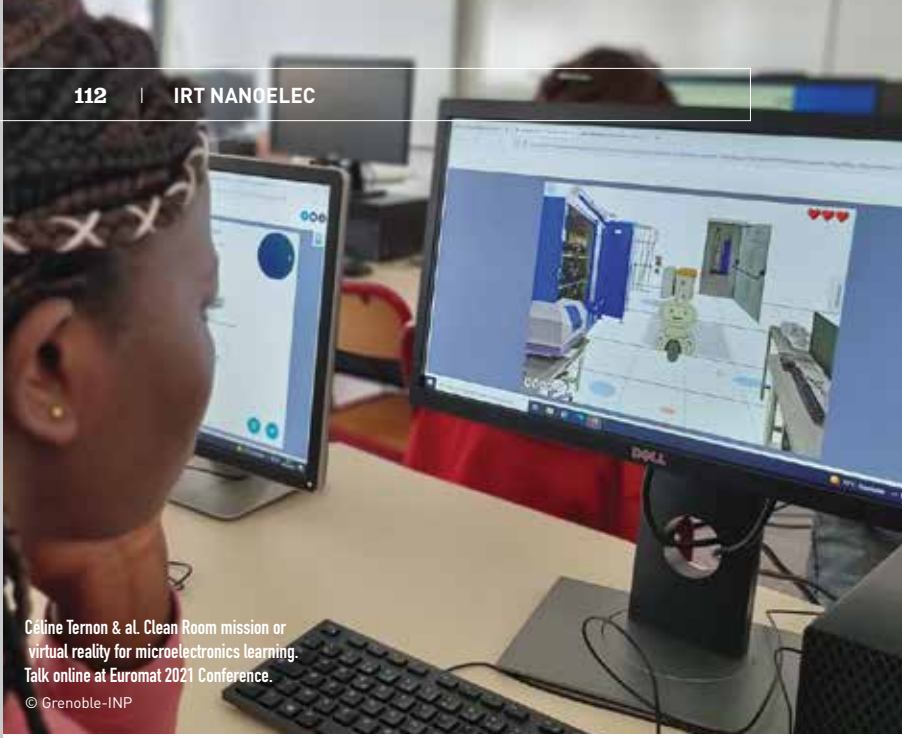
Serious game

Creanov

Innovation and creativity teachers as well as corporate innovation teams

By means of a statistical game, finding two thirds of the possible innovations in a category of products or services: this is what GEM proposes with Creanov.

This game is intended for innovation and creativity teachers as well as corporate innovation teams. It was developed to implement a scientifically proven method. It was prototyped and published within Nanoelec for the face-to-face sessions and digital format for the remote sessions. *"The validated methodology of the basic structure demonstrated its pertinence in supporting the innovation process at a number of companies. It is based on analytical and systematic approaches and is particularly relevant for engineering environments. It consists in breaking down an existing product into characteristics of two types – its components and its attributes – before then exploring their various configuration possibilities. This is extremely effective for product digitization issues"*, recalls David Gotteland, professor at GEM and one of the two designers of the game with Aurélie Merle. Creanov is targeting two audiences: students and managers in charge of innovation: product managers, R&D managers. More than 1,100 students and 110 persons in executive training programs have already used the board game version of Créanov. *"On 4 January 2021, 750 GEM students used the digital game. Twenty teachers had been trained to coordinate the remote sessions on-line"*, explains Isabelle Patroix, Playground Manager at GEM, who was responsible for digitization. ◆



Céline Ternon & al. Clean Room mission or virtual reality for microelectronics learning. Talk online at Euromat 2021 Conference.
© Grenoble-INP

Serious game

Team Up

Using the Team Up serious game, engineering students can experience a recruitment interview from both standpoints: the candidate side and the recruiter side.

The game enables the students in a recruitment situation to identify the important points and typical errors to be avoided during a recruitment interview. Team Up was designed by Grenoble-INP as part of the Human Capital and Training Design program at Nanoelec. Faced with a group of recruiters, the player in the recruitment situation must answer 6 questions drawn randomly from a selection of 14.
Each recruiter chooses the criteria they observe in the player-candidate: non-verbal communication, motivation, soft skills, technical skills and know-how, examples and anecdotes. ◆

Serious game

Clean Room mission

For awareness on clean rooms and their process flows

An educative team lead by Céline Ternon, professor at Grenoble-INP/UGA, has developed two virtual reality tools, under the Nanoelec/CHIF program, with the aim of enabling as many students as possible to discover the microelectronics clean room environment, the notion of process flow and the various characterization techniques required to monitor a technological process in microelectronics hardware fabrication.

We chose to rely on an electronic device attractive to students: the photovoltaic cell" Céline Ternon says. First of all, a virtual reality visit to the CIME-Nanotech clean room - developed with the Maison pour la science under the Idex UGA project and Nanolec/Chif program - allows immersion in the situation, a presentation of the process flow, the machines and the environment. Next, a video game allows students to characterize the materials throughout the integration process as if they were actually in the clean room. *"Finally, we have chosen an original scenario to arouse the curiosity and motivation of the participants. Thus, the players take on the role of a spy for an activist association wishing to make all the inventions and technologies that are beneficial to the planet and humanity available to all mankind. The association's next mission is to obtain the architecture of the latest first-generation solar cell manufactured in the CIME-Nanotech clean room. To do this, the spy first joins a visit to the clean room open to the public (virtual tour), which enables her or him to prepare the spying mission during which the target data are collected (video game)"*, reports Céline Ternon. ◆

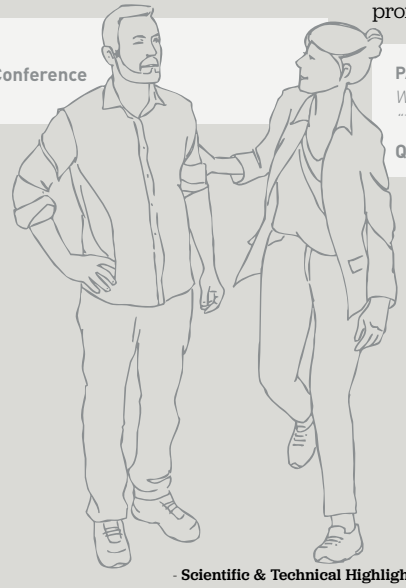
- KEY PUBLICATIONS -

Platform - Innovation & entrepreneurship in Education technologies.

The first period of the Nanoelec Education & training program led to the creation of the GEM Labs in the Grenoble scientific ecosystem, a place where the ecosystem of innovation is more than 100 years old. In a talk at the EETN ISP KU Conference, Sylvie Blanco, co-director of the Nanoelec/CHIF program and professor and executive-director of innovation at Grenoble Ecole de Management reported on several use cases developed through the GEM Labs in recent years. "*The training design activities supported by Nanoelec at Grenoble-Ecole de Management are presented as use-cases to reinforce the innovation capacity of the Grenoble ecosystem, through new trends in education and training, especially focused on digital transition. Some of these examples underline how it is possible to extend learning solutions (augmented real-life learning experiences) and to reconsider the learner environment (VR, communities for collaboration and challenges)*", she says.

"Leading innovative firms are well-established in the area, such as Schneider Electric, STMicroelectronics, Soitec, Aledia, Cap Gemini or Rossignol. The next step for the ecosystem actors will be to reinforce their ambition, engagement and legitimacy, their capacity for co-experimentation in mutual trust collaborative projects. GEM is preparing the creation of the TIM Live Academy as a new organization dedicated to promoting new creative entrepreneurial talents for a sustainable digital future", explains Sylvie Blanco. LIVE stands for Learning Impact, Values and Engagement.

SYLVIE BLANCO.
Talk at EETN ISP KU Conference
Leuven | April 21



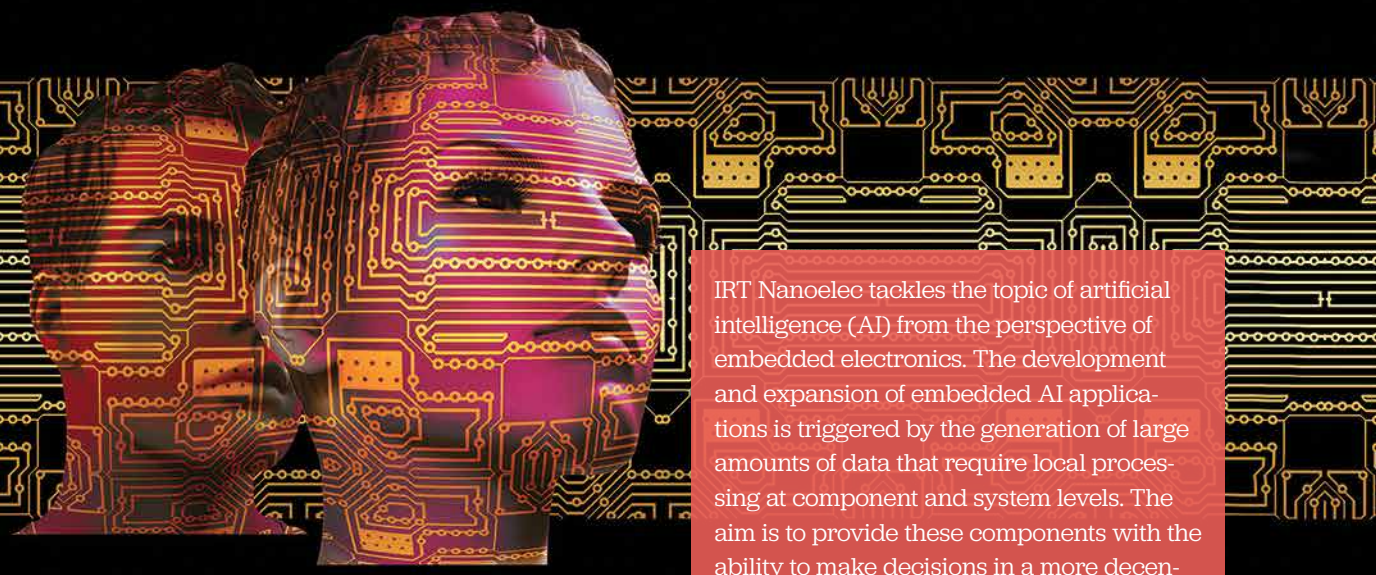
Workshop – Challenge "Towards sustainable microelectronics"

A workshop-challenge "Towards Sustainable Microelectronics - Creating the green smartphone of tomorrow " was held on February 5 and 12, 2021, bringing together 55 students from Grenoble INP and Grenoble Ecole de Management, as well as around ten experts. It was spread over two half-days adapted to distance learning conditions and offered completely in English. Students of the International Nanotech Master, of the Integrated Electronic Systems (SEI) program of G INP/Phelma and of Grenoble Ecole de Management (GEM) took part, using various digital tools (Zoom & Mural), in group activities aimed at increasing their awareness of environmental and social responsibility in their future missions as engineers / managers in the microelectronics sector.

The major innovation of the event was the use of the "My IoT" serious game developed within the CDP "Need for IoT" program from Idex UGA (https://need.univ-grenoble-alpes.fr) and in collaboration with the IRT Nanoelec training program (https://irtnanoelec.fr). The game allowed the students to identify the environmental impacts and the levers of action at all stages in the lifecycle of a product (a green smartphone): from the mining of raw materials, to design, manufacturing and distribution, to product use and end-of-life. The students worked in small groups to meet the design challenge by applying a sustainable development approach to a smartphone. The teams were supervised by experts from the industry (ST Microelectronics), academic partners (UGA and LETI/CEA), as well as professors from Grenoble INP and GEM.

PANAGIOTA MORFOULI & AL.
WORKSHOP-CHALLENGE
"TOWARDS SUSTAINABLE MICROELECTRONICS"
QPES 21 conference I La Rochelle I January 22

INCREASINGLY INVOLVED IN EMBEDDED ARTIFICIAL INTELLIGENCE



IRT Nanoelec tackles the topic of artificial intelligence (AI) from the perspective of embedded electronics. The development and expansion of embedded AI applications is triggered by the generation of large amounts of data that require local processing at component and system levels. The aim is to provide these components with the ability to make decisions in a more decentralized, autonomous and reliable manner. Therefore, processing must be integrated close to the sensor in order to optimize the flow of data and to ensure that it remains undamaged and confidential.
This allows a good trade-off between data flows from the sensor to the user and the related energy footprints of both the sensor and the central computer handling reduced amounts of data.
The teams involved at Nanoelec are mainly focusing on image sensors and on the security of AI components and systems.

Cybersecurity of edge AI

Future connected objects will need reliable implementations of embedded AI algorithms and security mechanisms to protect them from potential software and hardware threats.

Securing the implementation of AI algorithms in embedded systems is critical to the deployment and safe use of this technology in smart IoT systems.
Researchers from academic labs are working together with industrial teams within the Nanoelec/Pulse program on the secure implementation and deployment of AI algorithms, in particular machine learning algorithms embedded in IoT components.

Concerning autonomous robots, program teams are looking at the validation of the safety of artificial intelligence on robotic applications. The issue of evaluating and validating the effectiveness of these technologies is one of the last central issues delaying the adoption of embedded context capture technologies. It is therefore a major challenge for the market access of the autonomous vehicles. ◆

Smart Imagers

Imaging is one of the three main fields that use AI.

The aim is not only to achieve better image quality, but also to extract relevant data from the image, taking account of the environment, the object and the scene (potentially across a range of lighting conditions), and knowledge of the context.
The main objective of the Nanoelec/Smart Imager program is to evaluate the advantages of using 3D-stack technology to integrate the processing of artificial intelligence into the third layer of an image sensor.
The research teams are focusing on developing generic AI building blocks and the associated processing as well as on exploring the impact of these blocks on low-energy imager architectures. ◆

Application demonstrators for imagers

Teams involved in the Nanoelec/System Lab initiative define, develop and test cases using embedded AI technologies that are integrated into or associated with image sensors.

The project aims to develop functional demonstrators and explore new applications scenarios. Merging the data from optical sensors is based on artificial intelligence solutions in order to exploit the pertinent data. AI is usually developed specifically for the given use case. The System Lab teams are looking to identify the generic added value of AI, independently of the use cases. ◆

Training on Embedded AI

In collaboration with the MIAI institute (Idex Université Grenoble-Alpes), the Nanoelec/Chif program developed and digitalized the module entitled "Introduction to embedded artificial intelligence", in 2021.

The learning capsule contains theory and test sequences in the form of short videos. It is aimed at student in engineering or management curricula as well as professionals fromthe microelectronics industry. It introduces the learners to embedded artificial intelligence (for example, image recognition or identification of spoken keywords) and is able to qualify and quantify the limits of this technology. ◆

SUSTAINABLE DEVELOPMENT

For sustainable competitiveness in the electronic industry

BY

SANDRINE MAUBERT,
DEPUTY DIRECTOR
OF NANOELEC

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Inspired by its industrial partners, Nanoelec is active in four areas of work in line with the United Nations' framework for sustainable development goals. We have just begun a Life Cycle Assessment (LCA) applied to R&D for a new display manufacturing process under development at Nanoelec.

At the same time, we are evaluating and setting up with Minalogic a methodology for fast diagnosis to help SMEs assess the societal and environmental impact of their innovation projects. We are also working on human capital and skills, building a full range of training modules for sustainable electronics. And finally, in spring 2022 we launched our first ever competition for women in technology research.

Even if our major areas of focus remain technological, we are fully aware that a competitive sector is one that satisfactorily manages its environmental and societal impact. ◆

Four work areas for sustainable development

After a survey seminar in November 2020, IRT Nanoelec launched a number of cross-cutting work areas in 2021 in the field of sustainable development, in response to the recommendations accompanying the decision to continue with funding. The IRT Nanoelec "Sustainable Development" action plan comprises four areas of work.

ECO-INNOVATION APPLIED TO R&D PROJECTS

→ A quick and inexpensive diagnostic solution for companies (SMEs & startups) looking to run a project within the Easytech framework;

→ An eco-innovation tool in the R&D phase for the new-generation display production sector, currently under development with Aledia through the Displed program.

MANAGEMENT, SKILLS AND GOVERNANCE

→ Events to promote greater professional gender equality in the electronics sector;

→ The design of training courses for sustainable electronics, through the Human Capital and Training Engineering program.

Running R&D projects and eco-innovation

With the ongoing trend in Europe and France towards circular economy, companies are adopting sustainable innovation and eco-innovation concepts, which take account of economic, environmental and societal aspects.[1] The explicit and legible incorporation of these concepts is also becoming a strong factor in competitiveness for companies. To address these issues and the requirements of the Secrétariat général pour l'investissement (SGPI), Nanoelec committed itself to two specific projects in 2021: Defi-Ino and Ecodispled.

Quick diagnostic for Easytech: Defi-Ino

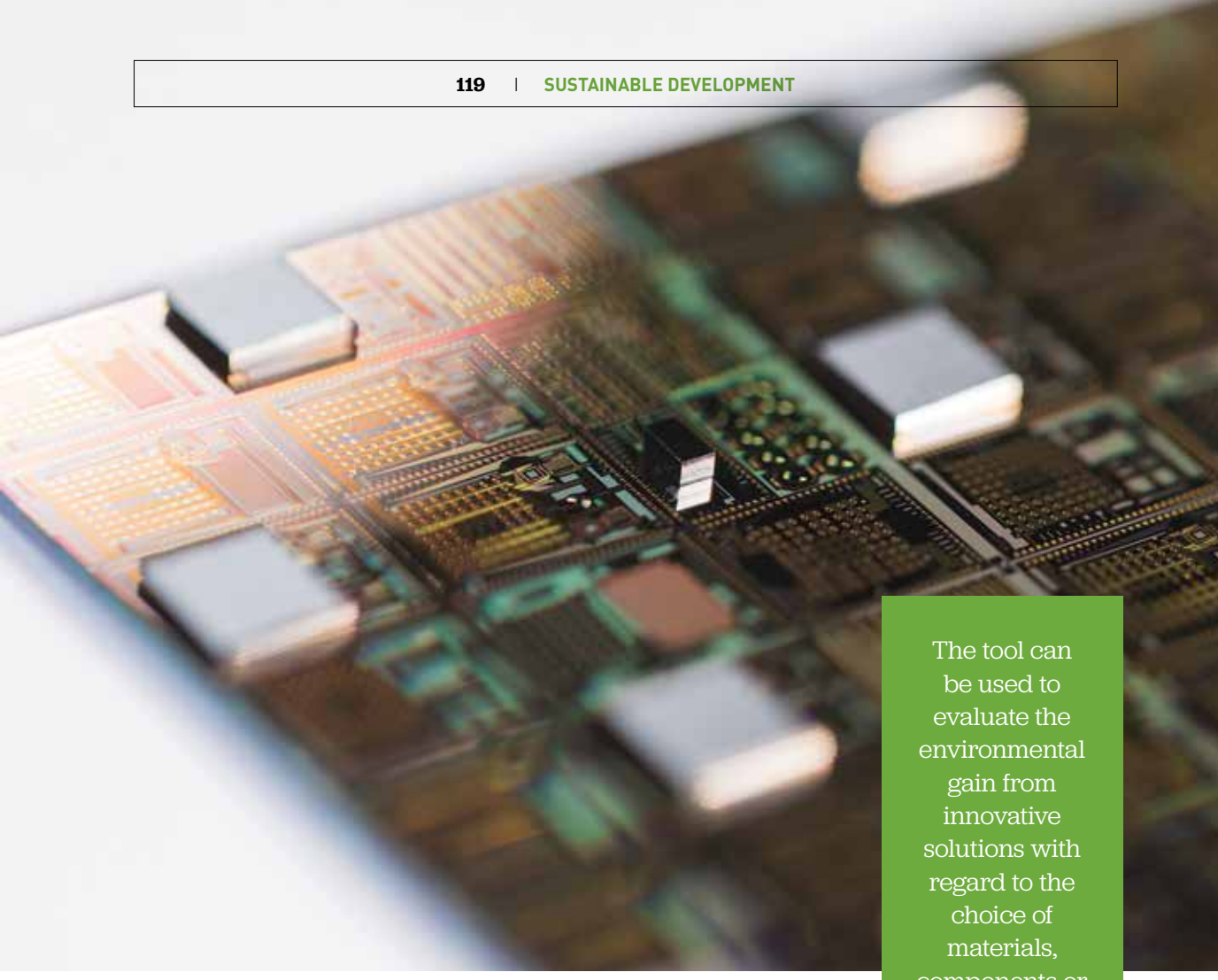
In close collaboration with Minalogic and Grenoble-INP, IRT Nanoelec launched the Defi-Ino project in 2021.

The project was initiated in conjunction with Ines.2S Energy Transition Institute (ITE). It consists in developing an "eco-innovation" type diagnosis for companies such as SMEs, mid-caps, and start-ups, launching an innovation project with the the expertise of one of the two institutes. The proposed diagnostic is quick and inexpensive. It does not replace an actual environmental assessment, nor a life cycle assessment (LCA), but aims to be a simple evaluation, which could encourage the company to commit to a more detailed study and towards a change in its environmental responsibility culture. The action is detailed in the "Technological dissemination" report. 2021 was devoted to the pilot phase with a definition of the process; two dummy tests run on completed projects allowed to generate an initial evaluation and select specialized private firms; eight "full scale" tests on current projects, in close cooperation with volunteering companies (3 Inec.2S projects and 5 Nanoelec projects).

This phase was coordinated by two academic laboratories specializing in the environmental and social impacts of technologies, with the participation of two private firms specializing in eco-innovation.

This phase was coordinated by two academic laboratories specializing in the environmental and social impacts of technologies (CEA-Liten and G-Scop./UGA), with the participation of two private firms specializing in eco-innovation (Circulab and Solid Creativity). The aim was to combine the feedback from these players in order to test SME interest in this type of service and the degree of acceptance of the methods proposed (confidentiality, mobilization, time, etc.). The experts built on the best practices for this audience by comparing the tools used and the projects already completed. The conclusions of this pilot phase are presented in the "Technological dissemination" chapter. ◆

1. For example, see the impact assessment of the Act on combatting waste and on the circular economy adopted in 2020 https://www.legifrance.gouv.fr/contenu/Media/Files/autour-de-la-loi/legislatif-et-reglementaire/etudes-d-impact-des-lois/ei_art_39_2020/ei_trep1902395l_cm_10.07.2019.pdf



Running R&D projects and eco-innovation

Eco-design in the R&D phase: Eco-Displɛd

In parallel with the R&D actions of the Displed prgram, Nanoelec is launching an R&D phase eco-design project, in close coordination with Aledia.

Some Life Cycle Analysis (LCA) tools are available, although they require a stabilized production framework and access to large volumes of data. The aim of the project is to implement an eco-design tool as of the R&D phase, appropriate for a sector that is not yet mature and devoted to Smart Pixel technology for the production of new-generation displays. To address the electronics needs, this will consist in adapting a method and a tool already developed by CEA-Liten for photovoltaics.

The tool can be used to evaluate the environmental gain from innovative solutions with regard to the choice of materials, components or procurement routes, by comparison with a reference process.

The tool can be used to evaluate the environmental gain from innovative solutions with regard to the choice of materials, components or procurement routes, by comparison with a reference process. An LCA of the reference sector based on standards 14040 and 14044 requires recent inventory data offering the optimum representation of the Smart Pixel concept. Data collection will rely on a bibliography as well as on interviews with experts. They will be supplemented by analysis of data from the EcoInvent international database, accompanied by calculations and estimations specific to the study.

The year 2021 was devoted to configuration of the action. The CEA-Liten method was assessed with regard to Nanoelec's requirements. Operational implementation is under way in 2022. ◆

Management, skills and governance

Sustainable development is built on two pillars: on the one hand, protecting the environment and, on the other, protecting humankind. Gender equality is one of the 17 sustainable development goals adopted by the United Nations as targets to be achieved by 2030.

Employment in the microelectronics sector is under stress and attracting talent, both men and women, is a real challenge. Students and professionals in the sector are looking for meaning and values. To hire and retain personnel, the players in the sector such as STMicroelectronics, Schneider Electric, Siemens EDA and CEA have implemented initiatives built around sustainable development and human resources. ◆

Training engineering

Several actions within the Nanoelec/Human Capital and Training Engineering program are helping to strengthen the sustainable development culture and skills of the sector's current and future professionals.

They are detailed in the report devoted to the CHIF program. A quick overview is given below.

FUNDAMENTAL SKILLS

- Development of the PISTE approach (French acronym for sober, technological and eco-responsible engineering (G INP)
- Development of the Odyssey Design Technology (ODT) approach - Adoption of innovation by the customer, incorporating a sustainable culture (GEM)
- Development of the Regional Energy and Environmental Transition Master's (G INP/Ense3)

LEARNING COMMUNITIES FACED WITH EMERGING CHALLENGES

- Design of an on-line challenge workshop: "For sustainable microelectronics; creating the green smartphone of tomorrow"
- Design of an eco-creativity challenge and a *"Responsible microelectronics, what are the realities"* webinar
- *"Semiconductor products & environmental footprint"* seminar as part of the Nanotech international Master's
- The GEM 2021 post-summer challenge *"Early influencers for sustainable digitals"* ◆

HR, diversity, inclusion, professional parity and equality

The approach adopted by IRT Nanoelec to address professional parity and equality was initiated further to proposals by few representatives of our Steering Committee.

Following this intervention, we took a number of pragmatic and operational steps, taking account of the particular status of IRT Nanoelec, which does not have its own legal identity and cannot therefore take over the role of the employers. The steps taken are designed to foster exchanges between the consortium's partners and the gradual construction of a collective culture on the subject. ◆

8 MARCH 2021

In-house webinar intended for all the Nanoelec team members. Round-up of possible actions - governance, webinars-testimonials and scientific awards. Bénédicte Henry-Canudas presented some CEA undertakings and Flore Gouaux and Jean-Marie Saint-Paul discussed the Women's Impact Network @Siemens.

29 APRIL 2021

In-house webinar intended for all the Nanoelec team members.
Further to a proposal by the Schneider Electric representative on the IRT Steering Committee, testimonials by several employees of the company; presentation of the 5 pillars underpinning professional gender equality.

30 MAY 2021

In-house webinar intended for all the Nanoelec team members.
At the invitation of Assia Tria, which was a the time a cybersecurity specialist at CEA-Leti involved in the scientific coordination of the Nanoelec/Pulse program, testimonial by Nacira Salvan, the creator and Chair of the Women's Cybersecurity Circle (CEFCYS).

17 JUNE 2021

In-house webinar intended for all the Nanoelec team members.
At the initiative of two CEA employees involved in the Nanoelec/Pulse program, debate and feedback from interventions in schools, in the presence of an educational actions manager from the Giant campus.

23 JUNE 2021

On the occasion of the International Women in Engineering Day on 23 June 2021, IRT Nanoelec and the Giant campus organized a public round-table, both face-to-face and remote, at the Maison Minatec, in Grenoble. Three speakers, who are employees in member companies or organizations of the Nanoelec consortium, recounted their career paths: Caroline Boudou (ILL), Séverine Cheramy (Aledia) and Flore Gouaux (Siemens EDA ex. Mentor Graphics). Two speakers shared the vision and strategy of their respective institutions in terms of parity: Céline Ternon (Grenoble-INP) and Sandrine Menduni (Grenoble local education authority). And two keynote speakers shared their visions: Jacqueline Etay (Senior scientist, Chair of the Association Parité-Science, Grenoble) and Juliette Cassagne (GEM-G-INP double major student, co-founder of the Think What Matters student and young researchers association).

21 OCTOBER 2021

Testimonial webinar with Florence Robin, co-founder of Limatech, supported by a Nanoelec/Easytech project in 2017.
In September 2021, Florence Robin received the Women's Industry award from Global Industrie. This award is for Limatech's commitment to diversity as well as the contribution of its technologies to ecological transition. Limatech is developing a new generation of Lithium battery packs for the aeronautical and defense sectors (in particular with Airbus). Limatech is a spin-off from CEA and is an Airbus Développement winner which has raised more than 2.5 million euros. This year, the company is housing the world's first aerospace accelerator, Starburst.

AND **EARLY 2022**

Nanoelec joins the "Femmes ingénieures" and "Parité-Science" associations.

ENGAGEMENT IN THE EUROPEAN R&D SPACE

Nanoelec has taken part in 28 European projects since 2012. Eleven are ongoing in 2022.

SMART IMAGER

EXASCALE COMPUTING

Mont Blanc 2020 is a collaborative H2020 project which aims to define the architecture of a SoC System-On-Chip) processor in order to build a European low-consumption Exascale system (50 Gflops/W) for high-performance computing by 2022.

With the support of Nanoelec, CEA is contributing to the project by providing real applications linked to the use of HPC infrastructure, the supply of various IP (communication, consumption management) and the final demonstration using its hardware emulation infrastructure. The other French contributors are Kalray and Bull, responsible for project coordination. The MB2020 architecture is relying on 2.5D integration technologies in order to assemble computing chiplets close to memories on a silicon interposer. During the project, CEA developed a solution for 3D short range communication links with an innovative auto-calibration mechanism to prevent transmission failure between chiplets. The results of the project are now being transferred to the European Processor Initiative (EPI) project.

https://www.montblanc-project.eu/

PHOTONIC SENSORS

CYTOMETRY

CEA-Leti and Prophesee, both partners in the Nanoelec consortium, are taking part in the Neoteric project. The Neoteric partners are aiming to develop a reconfigurable photonic circuit to detect cancer cells in a solution (cytometry).
https://neoterich2020.eu/

TRANSCEIVERS (EMBEDDED TRANSMITTER+RECEIVER)

The Masstart EU project will lead to the production of several Datacom and Telecom demonstrators. It focuses on the development of advanced packaging and test methods for producing very high speed transceivers (800 Gbps and 1.6 Tbps), with reduced form factors (COBO type).
CEA-Leti and Almae, partners in the Nanoelec consortium, are contributing to this project. A first generation of circuits was produced using the Silphide Design Kit developed within Nanoelec, and used by the partner Bright Photonics in its Nazca tool.
https://masstart.eu/

PACKAGING OPTOELECTRONIC COMPONENTS

The purpose of Pixapp, standing for Photonic Integrated Circuit Assembly and Packaging Pilot line, is to set up a European platform for packaging photonic components. It brings together 18 partners comprising photonic on silicon components manufacturers, component assembly specialists, systems assemblers, and players in the reliability field. Within Nanoelec, CEA-Leti is also a contributor. It is focusing on the demonstration of a self-assembly technique for micro-lenses on photonic on silicon components, in order to relax the optical alignment constraints between chips and fiber connectors, by shifting constraints to the precision of the photolithographic techniques. This packaging technological building block is generic and could be used for many applications.
https://pixapp.eu/

CHARACTERIZATION

Three European projects involving IRT Nanoelec, and more particularly its Carac program, were launched in 2021.

ADDRESSING KEY BOTTLENECKS OF NANOSCIENCE RESEARCH

NFFA (Europe's Nano Foundries and Fine Analysis Pilot) is an H2020 collaborative project which prefigures the first distributed research infrastructure within the EU, offering access to high-level instrumentation in the field of nanosciences and nanotechnologies. Within the NFFA consortium, IRT Nanoelec provides access to the ESRF/BM05 synchrotron beamline.

https://www.nffa.eu/

NANOMECHANICAL MATERIALS CHARACTERIZATION IN INDUSTRY

NanoMECommons is an H2020 collaborative project focusing on the development of new characterization methodologies tailored to industrial needs in the nano-mechanical field. ESRF is in charge of developing a deformation microscope to be installed on ESRF/ ID01 to complete a suite of instruments which also includes a Raman spectrometer reconditioned with the support of Nanoelec, which will be included in the Nanoelec/ PAC-G offering. This tool will support research activities in band-gap design for various microelectronics applications, in particular the study of new materials and substrates for optoelectronic devices.

https://www.nanomecommons.net/

EXPLORING RADIATION EFFECTS FOR INDUSTRY AND RESEARCH

Radnext (for RADiation facility Network for the EXploration of effects for indusTry and research), is an H2020 collaborative project aiming to launch a distributed research infrastructure within the EU devoted to the industrial and university irradiation community. The projet coordinator is Cern in Switzerland. The consortium houses a range of equipment/ installations offering time on different beam families for electronic components.
The available beams are: heavy ions, protons, neutrons, lasers, X-rays, electrons, gamma radiation. The collaborations with industry are coordinated by the ESRF, which also heads a Committee of industrial advisers. The Nanoelec/ Characterization program teams (ESR, ILL and Iroc Technologies) are involved and will concentrate on harmonizing the initiative with the operations to launch the Irradiation competence center.

https://radnext.web.cern.ch/

PULSE

DIGITIZING SMES

DigiFed is run by Nanoelec through its founding partners, CEA, STMicroelectronics and Minalogic. The aim is to demonstrate the potential of digital technologies in terms of hardware security, human-machine interaction, and autonomy for small and medium enterprises. DigiFed involves nearly 200 European SMEs in its innovation program. 80 of them can receive financial support and benefit from one of the DigiFed innovation channels. Half of them will be companies initiating their digital transformation.

https://digifed.org/

SECURE ARCHITECTURE FOR SMART CITIES

Nanoelec contributes to M-Sec, an #H2020-type Europe-Japan project, through CEA-Leti. Its goal is to achieve a proof-of-concept secure architecture for smart cities with two deployment sites, Santander in Spain and Fujisawa in Japan. Communication gateway security and security characterizations are carried out in the Nanoelec Product & Technologies Living Lab (PTL).

https://msecproject.eu/

ARTIFICIAL INTELLIGENCE OF OBJECTS

The European InSecTT (Intelligent, Secure, Trustable Things) project is an ECSEL (Electronic Components and Systems for European Leadership initiative) project, in which the participants include CEA and STMicroelectronics, within Nanoelec. InSecTT aims to combine the Internet of Things (IoT) with Artificial Intelligence (AI) by building trust in AI-based smart systems and solutions, which constitute a significant part of the concept of the artificial intelligence of things (AIoT), which is the natural evolution of AI and the IoT. The projet comprises 52 partners (12 nationalities) and is coordinated by Austria (Virtual Vehicle). The project began on 15 June 2020 and will last a total of three years.

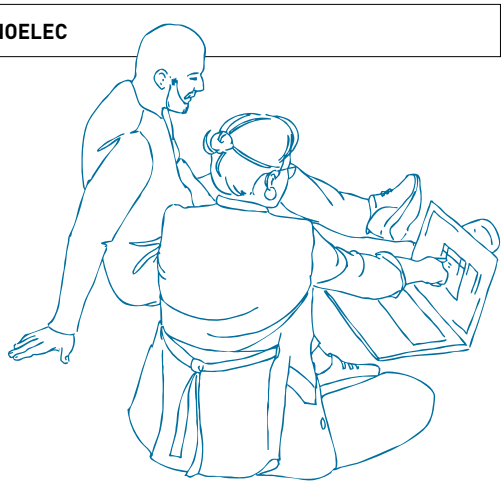
https://www.insectt.eu/

SECURE IOT FOR AGRICULTURE

To meet the needs of agriculture, the H2020 Sarmenti project is developing in-situ, real-time solutions to measure the various nutrients present in the soil and the gas emissions just above the soil, in order to improve management of natural or chemical fertilizer inputs, to maximize crop growth, minimize environmental losses and thus reduce the pollution linked to poor fertilizer management. The Pulse program at Nanoelec, which more particularly involves CEA and STMicroelectronics, provides solutions to secure sensors in IoT mode against side channel attacks. Open-field experiments are ongoing in France, Romania and Ireland.

https://sarmenti-project.eu/

Governance



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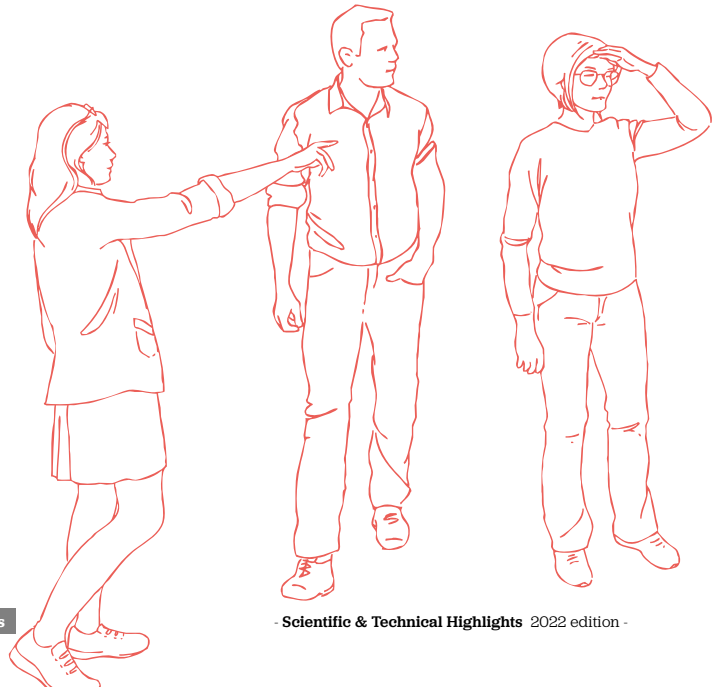
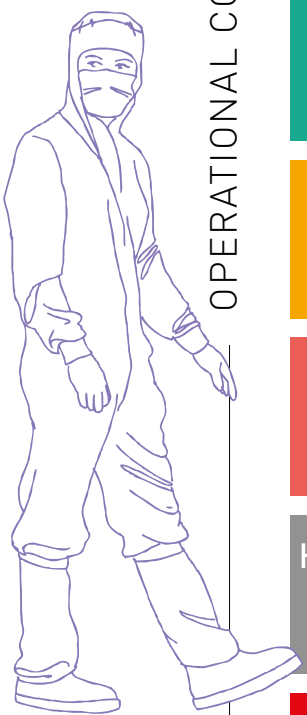


OPERATIONAL COMMITTEE



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