

Scientific & technical highlights

NANOELEC.

2020 EDITION



“ *The technological research institute IRT Nanoelec is a consortium of 21 members from the private and public sectors dedicated to innovation in microelectronics.*

Table of contents

4

Delving into the heart of microelectronics of the future

IRT Nanoelec
at a glance

6

Key figures of the institute

December 2019

8

Digital as an option for resilience

Director's Foreword

10

Highlights

18

3D Integration

28

Silicon photonics

36

Pulse

48

PowerGaN

54

Human capital and education design activities

62

Large-scale instruments characterisation

68

Easytech

Scientific & technical highlights of the IRT Nanoelec • 2020 EDITION

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Grenoble, June 2020

> Delving into the heart of microelectronics of the future

IRT Nanoelec at a glance

IRT Nanoelec runs multi-partner technology dissemination and development programs to make the microelectronics sector more competitive.

The aim of IRT Nanoelec members is to work together to carry out research and development programs to help businesses create value and grow.

Since 2012, 238 associated partners, including 184 SMEs and 17 foreign companies have carried out projects with Nanoelec.

At Nanoelec, information and communication technologies professionals work in the digital transition, energy transition and secure connected systems fields.

IRT Nanoelec also has a training program to prepare human capital for changes at its partner organizations, and a technology dissemination program for SMEs and mid-caps. These two programs receive support from the French State and local authorities, among which the AURA region.

Nanoelec has been operational since 2012 and is one of the eight technological research institutes (IRT) launched as part of the Investments for the Future Program (PIA). These institutes are R&D operators, bringing together an ecosystem of public laboratories and private partners, each with a specific focus on a technological field.



“

Work together to carry out research and development programs to help businesses create value and grow.

Anticipating future human, material and technological needs

→ Innovation in Microelectronics

- Carry out world-class collaborative R&D in four main areas: 3D integration technologies, silicon photonics, GaN-on-Si power components and digital trust for embedded systems and components
- Give industry players access to development, prototyping and advanced characterisation resources

→ Technology Dissemination

- Develop and transfer these technologies to our partners, to create the electronic circuits of the future
- Help businesses in the field of information and communication technologies meet the challenges of IoT and digital trust and security
- Promote cooperation between SMEs, mid-caps and large companies

→ Development of Human Capital

- Attract more young people into jobs in electronics
- Map out needs and assess employment opportunities
- Design training courses to meet current needs
- Anticipate future skills required in the electronics industry

> Key figures of the institute

December 2019



A consortium of
**public
& private**
members*

* 22 partners in december 2019



€60M
annual budget



238
associated partners,
including 184 small
& medium size
companies

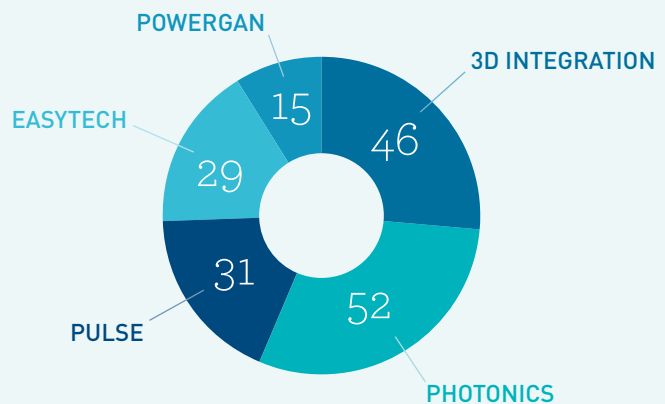


394
scientific or technical
publications &
communications
since 2015

“Anticipating future human and technical needs

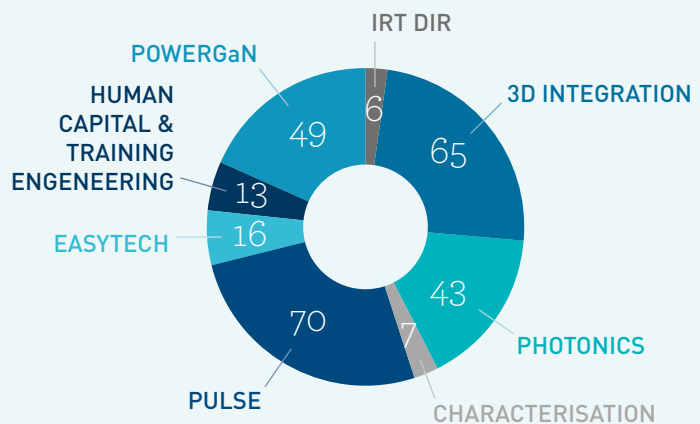


173
patents and **36**
software solutions
filed since 2012



269
full time jobs,
33% coming from
private companies

Human resources at the Institute
(in Equivalent full-time)



> Digital as an option for resilience

Director's Foreword



HUGHES METRAS

*Director of the
Technological
Research Institute
IRT Nanoelec*

“*The media hardly noticed it but many activities carried on thanks to digital technology.*”

From the start of confinement, while usual social activities were abruptly reduced and our offices, shops, factories, movie theaters and streets were emptied, the digital world took over and helped us to keep in touch with our loved ones, friends, partners and coworkers.

Digital technologies enabled many businesses and economic actors to continue their operations during this period of quarantine. These solutions helped maintain the ties that are the very fabric of our societies. The media hardly noticed it but many activities carried on thanks to digital technology: virtual classes in education, TV programs, health instructions and solidarity on radio channels, remote banking and contactless payments and, last but not least, the now famous teleconferences from our home offices are just examples of the “digital experiences” that each of us lived in the recent weeks.

The coming world will bring accelerated changes, most of which are based on digital tools. Connectivity and image technologies have proven particularly essential in this context. Their use, at a scale never seen before, also underlines the need for continuous innovation in the field, towards more efficient components and software with more advanced functionalities, endowed with artificial intelligence and deep learning functions.

Today, a few months after the outbreak of an unprecedented health and economic crisis, the electronics industry intends to meet the challenges of recovery and economic sovereignty. Provided that the infrastructures on which they are based evolve, semiconductor technologies could be a solid pillar of the revival of the economy.

“ We confirmed our ability to contribute to the vitality of the microelectronic sector in France and Europe by involving more and more innovative SMEs and mid-caps.

These considerations inspired us to choose a leaf of Gingko Biloba for the cover of this activity report. It is a perfect symbol of resilience. At Nanoelec, we are convinced that innovation in electronics, carried out in a multidisciplinary and multi-partner framework, is one of the drivers of this resilience. Our mission is to implement new ideas.

Upgrading our programs to an increasingly competitive and multi-application environment will require open innovation initiatives. This seems particularly urgent and essential in fast changing fields such as imaging technology which connects the physical and digital worlds. It is also critical in the field of energy conversion, so important for the electrification of transportation systems, or in the domain of secure components and embedded systems necessary for resilient and sovereign infrastructures.

We are a consortium at the interface between academic research, education and industry & services, supported by the French Government¹. Above all, our impact and our results come from the excellence of the teams engaged by all of our partners, relying on a set of technological means that make Grenoble a unique ecosystem in our fields.

Browsing the last 18 months over the pages of this report, you will see that Nanoelec is continuously evolving to keep up with the evolutions of the microelectronics sector. As an example, our 3D and photonics programs, initially positioned on disruptive solutions for computation are now also addressing the field of sensors. Similarly, our Pulse program continues its transition to cybersecurity, placing us at the heart of the challenges of sovereignty and digital trust.

We have also confirmed our ability to contribute to the vitality of the microelectronics in France and Europe by involving more and more innovative SMEs and mid-caps. The entry into the consortium of Akeoplus, Prophesee, Aledia and Lynred illustrates this as much as the numerous projects carried out within the framework of Easytech, the program also funded by the French region AURA and local institutions

A little less than a year after taking office to pursue the task of my predecessor Michel Wolny, I am pleased to introduce this reflection of a very intense activity. The excellence of the results, as well as the extent and diversity of the subjects dealt with in this report, are a witness of the quality of the work carried out over the past eight years and I would therefore like to thank Michel and his team who accompanied me during these first months.

¹ The French Government confirmed on Jun 4, 2020, its support to its 16 institutes dedicated to technological research and Energy transition, federated in the FIT Association.

Highlights



OCTOBER 2018

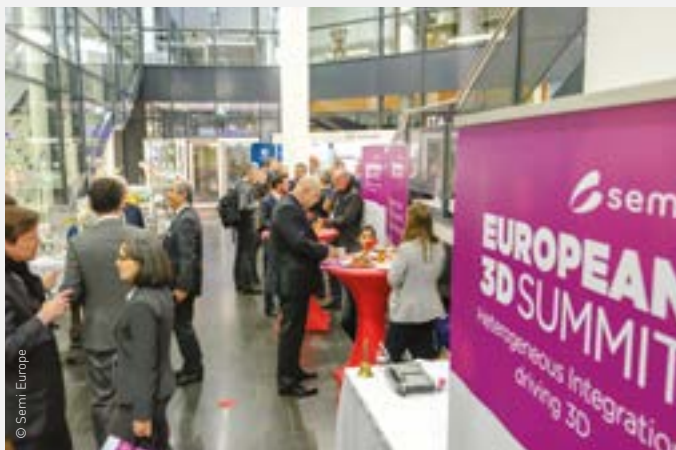
Digital transformation

→ Akeoplus, a company involved in the digital transformation of factories, specifically in the automotive and aeronautical fields, joins the Nanoelec consortium.

NOVEMBER 2018

GaN workshop

→ 70 innovation professionals from the electronic sector take part in a national workshop on GaN-based power components, which was organized by Nanoelec in Paris.



JANUARY 2019

Semi 3D Summit

→ Developed under Nanoelec, IntAct, an active interposer demonstrator for High performance computing (HPC), and Harmony, the world's first demonstrator of a 3D integrated image sensor with a pitch of 1.44 micron, are presented to 200 participants at the Semi 3D Summit in Germany.

JANUARY 2019

Characterisation platform

→ The PAC-G characterisation platform is presented to Jean-Eric Paquet, General Manager for research and innovation at the European Commission.



FEBRUARY 2019

Lean Management

→ Official launch of RNDYNEO, a training in Lean Management applied to R&D.



FEBRUARY 2019

Photonics West

→ Nanoelec presents a photonic fiber-chip coupling by nano-structured network with only 1 dB of optical losses, at the Photonics West conference (USA).



MARCH 2019

General Assembly

→ 150 participants attend IRT Nanoelec's general assembly.

MAY 2019

Immersive learning space

→ First version of the “TIM Lab” (GEM), an immersive learning space dedicated to the management of innovation and technology that fosters collective intelligence and “phygital” tools.



MAY 2019

Award

→ “Best Paper Award” at the ECTC conference (May 2019, Las Vegas, USA) for his article entitled “Active Interposer Technology for Chiplet-Based Advanced 3D System Architectures”.

JUNE 2019

3D integration

→ Aledia, a start-up involved in 3D LED technology, and Prophesee, a neuromorphic imaging system start-up, join the Nanoelec consortium to participate in the 3D integration program.



JUNE 2019

Digital Tech for care

→ Samba, a software and hardware solution for welcoming hearing-impaired students to university, offers fast and smooth speech transcription that staff at the front desk can correct or enhance in real time.



SEPTEMBER 2019

Semicon Taiwan

→ SET launches the new NEO HB hybrid bonding machine at Semicon Taiwan. NeoHB was developed through the Nanoelec/3D integration program.

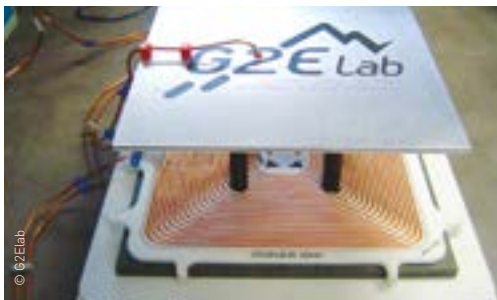


© SET

SEPTEMBER 2019

Powergan consortium

→ G2ELab joins the Nanoelec/Powergan consortium, bringing its expertise on electromagnetic compatibility.



© G2ELab

SEPTEMBER 2019

Management

→ Hugues Métras is appointed Director of the institute, taking over from Michel Wolny.



© Jayet / CEA

SEPTEMBER 2019

Sport trade fair

→ Nanoelec/EasyTech and the SMEs, Ido Data and Microoled jointly participate to the Sport Unlimitech trade fair, in Lyon.



SEPTEMBER 2019

Power electronics

→ STMicroelectronics invests €100 million in a pilot line for power electronics, based on a technology developed as part of Nanoelec.



© STMicroelectronics

SEPTEMBER 2019

Starting-up Photonics

→ Scintil Photonics, a start-up that integrates photonic technologies developed as part of Nanoelec, raises €4 million during a first round of funding.



OCTOBER 2019

RISC-V forum

→ 120 participants attend the RISC-V forum organized by Nanoelec in Paris. RISC-V is the international standard for open architecture in electronics industry.

OCTOBER 2019

3DVLSI workshop

→ Around 60 professionals participate in the sixth 3DVLSI workshop (high-density 3D-IC and CoolCube technologies) organized by CEA-Leti, NanoElec and Qualcomm, on the sidelines of the IEEE 2019 S3S conference.



OCTOBER 2019

Forum for the institutes of technologies

→ 250 professionals from Institutes for energy transition and technological research (members of FIT association) meet in Lille for their annual forum.

NOVEMBER 2019

Carac conference

→ Carac 2019 is an international conference on the characterization of materials and components for industry. Organized under Nanoelec, it brings together more than 60 European experts.



NOVEMBER 2019

European Cybersecurity Week

→ The book "Physical security of systems - Vulnerability of processors and operating techniques" receives a literary award during the European Cybersecurity Week. Its authors take part in Nanoelec/Pulse program.



NOVEMBER 2019

Genesis upgrade

→ A gain, by a factor of 10 in neutron flux is obtained from Genesis, a part of the Nanoelec PAC-G characterisation platform.



Table of contents

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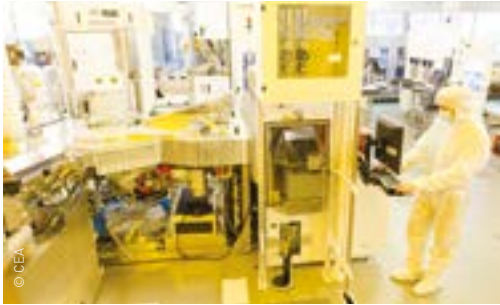
NOVEMBER 2019

International training

→ RNDYNEO spreads its wings in India: after being delivered to professors of Amrita Vishwa Vidyapeetham University, the training is deployed in STMicroelectronics factories.



Table of contents



NOVEMBER 2019

SGPI visit

→ IRT is visited by Guillaume Boudy, Secretary General for Investment (SGPI) at French government.

DECEMBER 2019

ANR forum

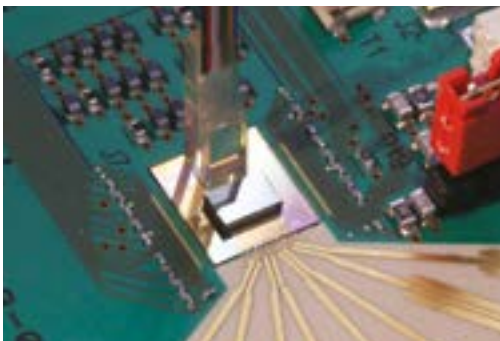
→ At the ANR forum in Paris, the Nanoelec booth is visited by Guillaume Boudy, Secretary General for investment (SGPI), Thierry Damerval, Director-General of the French National Agency for Scientific Research (ANR) and Olivier Ginez, Advisor to the French Ministry of Research and Higher Education.



JANUARY 2020

Sustainable Electronics

→ First "Sustainable Electronics" module rolled out with experts from STMicroelectronics, CEA and UGA to 40 master's students.



FEBRUARY 2020

Photonics process flow

→ New developments of the CEA-Leti silicon photonic process flow developed as part of Nanoelec, presented at Photonics West (USA). It now includes integration of two layers of optical waveguides and automated design of advanced applications.

MARCH 2020

Lithium battery for aeronautics

→ Limatech, a start-up that has benefited from the support of Nanoelec/Easy-Tech, raises €2 million for the development of its lithium batteries for aeronautics.



MARCH 2020

From technology to design

→ International webinar "From Technology to Design" is organized by Nanoelec at the occasion of DATE 2020 international conference. 3D Integration, Powergan and Photonics at a glance are provided online.

APRIL 2020

MIT Global Startup Workshop 2020

→ Lancey Energy Storage, a start-up that has received Nanoelec/EasyTech support, ranks second in the "Sustainable Society Startup Challenge" of the MIT Global Startup Workshop 2020.



MAY 2020

Lynred joins Nanoelec

→ Lynred IR detectors are key components of many top brands in commercial thermal imaging equipment sold across Europe, Asia and North America. Lynred joins the Nanoelec consortium in May 2020.

3D Integration



SÉVERINE CHERAMY

Director of Nanoelec 3D Integration program

Look & outlook

With the advent of Industry 4.0 and the era of connectivity, electronic devices use an ever increasing number of components. At a time when Moore's Law is running out of steam, 3D integration represents an alternative for further developing multifunction chips while reducing overall dimensions. These 3D techniques increase performance (for example, the bandwidth between a processor and the memory), reduce electrical consumption by replacing a long horizontal connection with a short vertical connection, lower production costs by using technology adapted to the desired functionality, and reduce the form factor.

These advantages are of great interest to both academic research groups and the microelectronics industry. In addition, the rapid emergence of this technology in the industry requires a global approach that takes into account both the development of the technology and the design of new 3D circuit architectures, as well as the development of design, testing and reliability tools. For these reasons, 3D integration is a natural part of Nanoelec's core programs.





Through the use of 3D electronics, it has become possible to transfer processing functions with high added value, such as object recognition or motion capture. On a mobile system, such as a cell phone, the challenge is to relieve the central processor of computing capacity, energy consumption and heat dissipation. This is how Nanoelec 3D Integration program has gradually shifted towards developing technologies for capturing and interpreting images, with more autonomous and smarter components in mind, while incorporating ever more complex image processing functions.

Another field of application addressed by the partners of the 3D program is high-performance computing, an area for which 3D integration and advanced packaging technologies have gradually become the norm, due to the increasing need for performance. Silicon interposers, first passive and then active, i.e., smart, are now widely deployed in high-performance systems. The 3D program has been a pioneer in this area with the development of smart interposers. This was demonstrated in 2019 by a number of significant advances reported in the scientific publications presented below.

These publications also open up vast scientific and technological fields that will need to be explored to enable manufacturers to incorporate 3D architectures into their processes and products. Many questions arise especially with respect to interfaces, such as mastery of hybrid bonding, conductive channels (vias) or even interposers.

To mention only certain major advances: since the start of the program in 2012, we have produced two world-class proofs of concept: a 3D-integrated image sensor with a connection pitch of 1.4 μm ; and an active interposer incorporating power supply and power management functions. Both have received high-profile scientific recognition, with publications in IEEE IEDM and IEEE ISSCC.

Another success story of the program is the introduction of a new equipment on the market by the equipment manufacturer SET. This equipment, apart from being an important event for the company with less than 100 employees, is also a major advance for microelectronics. In fact, it is the first equipment of its kind in the world.

The success of a project is also measured by its appeal. Started with three partners in 2012, the 3D program had grown to six partners at the end of 2019. Prophesee, a French start-up specializing in event-based image sensors, and Aledia, specializing in displays, joined the consortium in mid-2019. In 2020, Lynred, global leader in designing and manufacturing IR imaging technologies, also joined the consortium. On the one hand, they are proof of the relevance of the consortium's choices with respect to 3D technologies for image capture and, on the other hand, of the generic nature of the technological building blocks to explore new applications that can create high added value for new French start-ups.



> New members at Nanoelec

> Mobilizing a global ecosystem for reliable and profitable 3D products

Nearly 60 people took part in the sixth 3DVLSI workshop, on October 15, 2019, on the sidelines of the IEEE 2019 S3S conference (in San José, USA).

Organized by CEA-Leti, IRT Nanoelec and Qualcomm, the workshop focused on high-density 3D-IC and CoolCube technologies. "We have been working on building a complete ecosystem that goes from design technology to production", explained Séverine Cheramy (CEA-Leti), director of the 3D program at IRT Nanoelec, who opened the working session. "Over the course of six events, this workshop has become a forum to foster the sharing of experience and know-how within this ecosystem. The goal is to bring out technologies using 3D architectures that are truly industrially viable for reliable and profitable products", she added.

Scientists and engineers from various key players in the field also gave presentations: CEA-Leti, STMicroelectronics, EVG, SET, Mentor Graphics—all

members of Nanoelec's 3D program—as well as zGlue, LAM Research and Applied Materials. "Since the first 3DVLSI workshop held in San Diego in 2014, we have benefited from contributions from Qualcomm, Applied Materials, ARM, Atrenta, Cadence, CEA-Leti, GeorgiaTech, Global Foundries, HPE, Intel, Mentor Graphics, TSMC and many others", said Séverine Cheramy. •



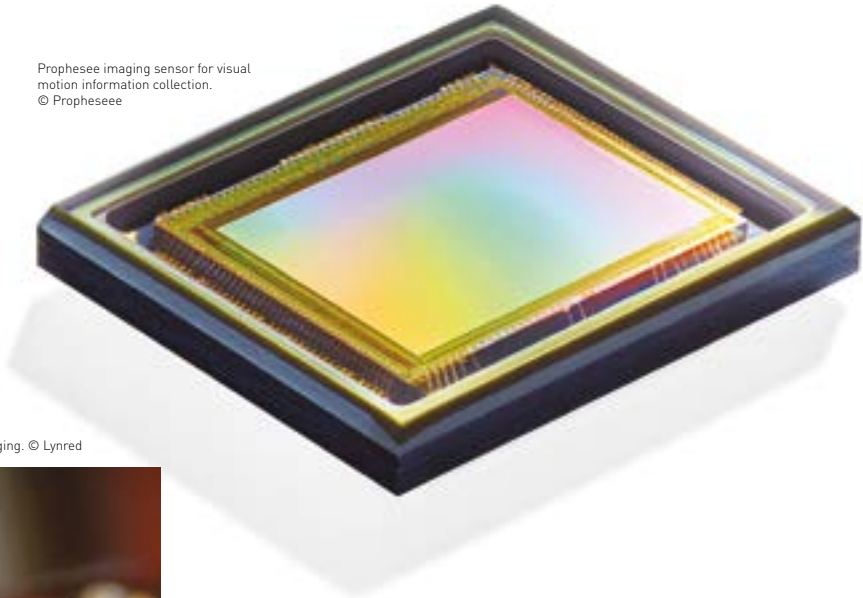
Lynred, Aledia and Prophesee join the Nanoelec consortium.

Aledia is developing LED (Light-Emitting Diode) technologies for displays based on a unique 3D nanowire architecture.

The technology enables high image quality and exceptional brightness, for both indoor or outdoor use, with very low consumption. "Aledia joined the Nanoelec/3D Integration program in 2019, opening up a new field of application for 3D integration by direct plate-to-plate bonding. Linking LEDs to 3D nanowires, the heterogeneous integration offered by bonding will allow us to continue the development of our technology", explained Xavier Hugon, managing director of Aledia, which is targeting the connected watch, telephone, television as well as augmented and virtual reality markets.

"The Prophesee sensors continuously collect essential visual motion information in the scene, pixel by pixel, as do our retinal photosensitive cells", said Prophesee president, Luca Verre. The startup, which raised €25 million at the end of 2019, is developing a new category of bio-inspired artificial vision systems using patented artificial intelligence sensors and algorithms.

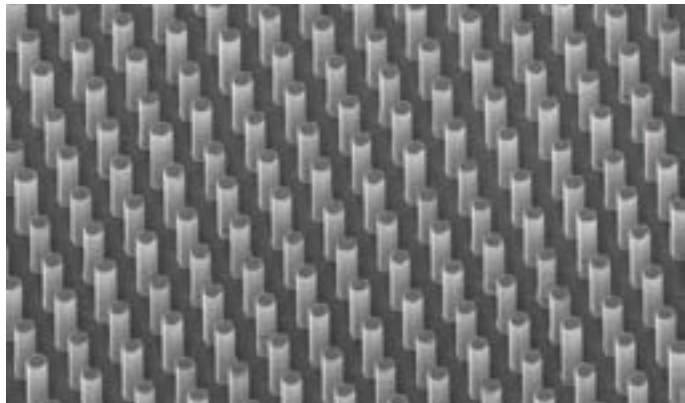
Prophesee imaging sensor for visual motion information collection.
© Prophesee



A Lynred sensor for IR imaging. © Lynred



Aledia's nanowire-based LEDs for display. © Aledia



"Through Nanoelec, we're going to integrate hybrid plate-to-plate bonding with a low interconnection pitch ($<5\ \mu\text{m}$) to develop future generations of vision sensors", explained Luca Verre. Lynred infrared detectors are key components of many top brands in commercial thermal imaging equipment sold across Europe, Asia and North America. The company is a global

leader in designing and manufacturing high quality infrared technologies for aerospace, defense and commercial markets. Lynred joined the Nanoelec consortium in May 2020. *"3D stacking technology will contribute to address the major development trend in IR detectors: shrinking the pixel pitch, an important parameter for increased image resolution. Advances*

in this area will enable Lynred to integrate new functions at the level of the pixel, while producing even smaller, lighter IR devices", said David Billon-Lanfrey, Chief Strategy Officer of Lynred. "We are interested making progress on the path of smart imagers and we think the multipartenarial projects of Nanoelec is a fitted frame to do it". •



Industrializing rapid and precise chip-to-plate bonding in production streams

In September 2019, SET chose the Semicon Taiwan trade fair to showcase its latest production equipment, NEO HB, developed in partnership with Nanoelec.

The machine produces chip-to-plate assemblies by hybrid/direct bonding. The main technical features are high precision after assembly, high throughput, processing of several hundred chips per hour, and a very low level of added defects compatible with direct bonding. These features make it possible to accommodate production markets where the interconnection pitches are very small, less than 10 μm . Applications such as high-performance computing or even memory stacking can be carried out using NEO HB.

"Being in a consortium within IRT Nanoelec enables us, right from the R&D phase, to adapt the design if necessary and to qualify our machines by having access to real components and industrial production challenges. The work and discussions within the IRT provide us with an end-user vision for our machines", explained SET president, Pascal Metzger.

The installation of a SET prototype direct bonding machine



inside the CEA-Leti cleanrooms since 2017, and its gradual qualification have led to several publications in major conferences in the field, which has led to increased visibility for SET. *"In fact, the opportunities to publish scientific articles with academic teams has strengthened our credibility and our visibility in the inherently very narrow and demanding microelectronics equipment market", he added.*

The company, from the Haute-Savoie region in France, was set up in 1975 and has the specificity of being a worker cooperative since 2012, following a takeover by its employees. With more than 350 machines installed in cleanrooms around the

world, it is a recognized leader in the market for high-precision flip-chip bonders.

"Nanoelec represents a very stimulating multicultural opening for us", explained Pascal Metzger, who also pointed out that the scheme of the IRTs had greatly contributed to the realization of the SET production machine project. "We are continuing our work within Nanoelec to characterize potential markets for NEO HB-in particular the production of electronic components for memory and intensive computing - but also to strengthen our positioning within the more general market of precision assembly", added the SET president. •



Key publications



INCREASING CHIP-TO-CHIP BANDWIDTH IN AN ACTIVE 3D INTERPOSER

Perceval Coudrain (CEA-Leti) who works on 3D integration and advanced packaging as part of the 3D Integration program, received the "Best Paper Award" at the ECTC conference (in May 2019, Las Vegas, USA) for his article titled "Active interposer technology for chiplet-based advanced 3D system architectures". "An active interposer enables the addition of smart features to the final 3D system, such

as advanced network-on-chip (NoC) interconnects, fast I/Os for off-chip communication, embedded power management and system-on-chip (SoC) infrastructure", Coudrain said. "Our paper reported on the first successful technological integration of chiplets on a fully processed, packaged and tested active silicon interposer".

The prize was officially announced in January 2020.

→ **COUDRAIN & AL.,
Active interposer
technology for chiplet-
based advanced 3D system
architectures**

2019 IEEE 69th Electronic
Components and Technology
Conference (ECTC)

DOI:10.1109/
ECTC.2019.00092



RELEASING HPC & BIG DATA APPLICATIONS FOR 3D TECHNOLOGY

At the ISSCC 2020 conference, (February 2020, San Francisco, USA), CEA teams reported on a high-performance processor breakthrough achieved as part of the 3D Integration program. They implemented an active interposer as a modular and energy-efficient silicon platform that enables efficient integration of large-scale chiplet-based computing systems for high-performance computing (HPC) and big-data applications.

"This is a breakthrough in terms of system-and-architecture integration, achieved all the way from the architectural design down to a silicon prototype", said Pascal Vivet (CEA-Leti), the lead author of the paper. "In addition, 3D technology and associated design techniques are now available for implementing large-scale computing systems, thus offering a chiplet-based 96-core computing architecture for the first time."



Pascal Vivet (CEA) presenting Nanoelec results at the ISSCC 2019. © DR

→ **VIVET & AL., A 220GOPS 96-Core Processor with 6 Chiplets 3D-Stacked on an Active Interposer offering 0.6 ns/mm Latency, 3 Tb/s/mm² Inter-Chiplet Interconnects and 156 mW/mm² @ 82% Peak-Efficiency DC-DC Converters**
ISSCC (February 2020)

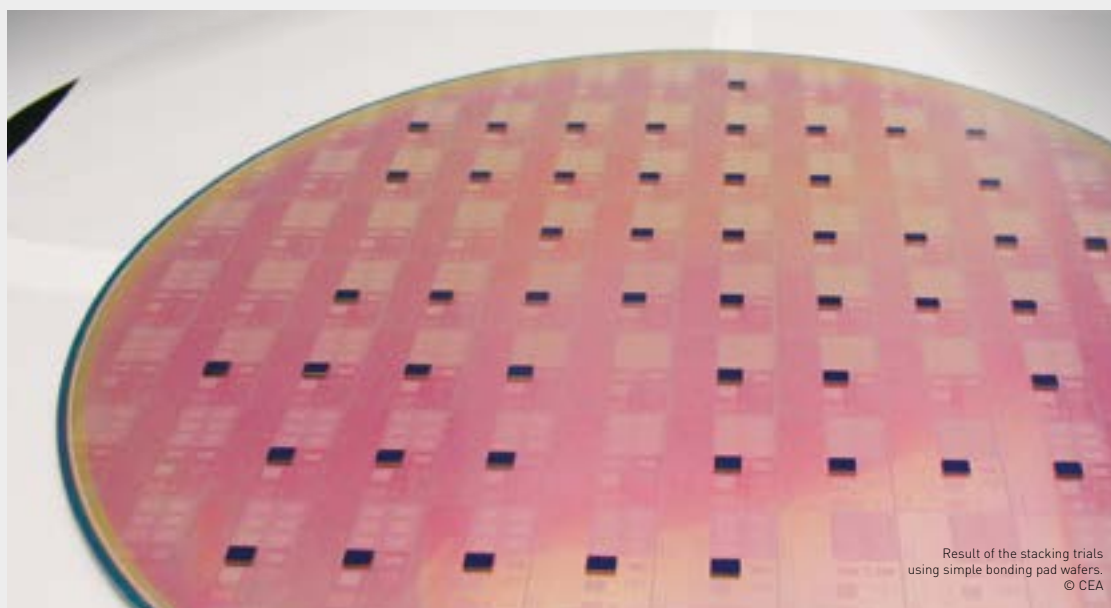
APPLYING 3D TECHNOLOGY TO SMART IMAGE SENSORS

At the Date 2019 conference, teams from CEA-Leti gave an overview of recent 3D technology solutions for image sensors developed as part of the Nanoelec 3D Integration program, including hybrid bonding technology and the Monolithic 3D CoolCube™ technology, which have 3D interconnect pitches in the order of 1 μm and 100 nm, respectively. *"Multi-layer 3D image sensors*

based on events and spiking will reduce power consumption with new detection and learning processing capabilities. By displaying our recent 3D image sensors, we have demonstrated the capability of 3D technology to implement fine grain pixel acquisition and processing with ultra-high speed image acquisition and tile-based processing", Pascal Vivet (CEA-Leti) explained.



→ **VIVET & AL., Advanced 3D Technologies and Architectures for 3D Smart Image Sensors**
Design, Automation & Test in Europe Conference & Exhibition (DATE), March 2019
DOI:10.23919/
DATE.2019.8714886



SHAPING 3D TECHNOLOGY FOR 300 MM WAFER PROCESSES

Die-To-Wafer (D2W) direct hybrid bonding is seen as a major breakthrough for the future of 3D components; however, its industrialization raises additional challenges compared to Wafer-To-Wafer processing. As part of the 3D Integration program, a complete 300 mm wafer solution was developed by CEA-Leti and SET to improve the bonding yield of D2W hybrid bonding using copper inter-

connections for the assessment of the electrical performance. *"In a dedicated 300 mm electrical test vehicle and robust stacking system, stackings with a +/- 1.5 μm alignment accuracy and excellent bonding interface were obtained (80% bonding yield)"*, explained Amandine Jouve, first author of a paper presenting the study at the 3DIC conference in Japan. *"After stacking and annealing, the die*

can be thinned down to 10 μm without any damage. Electrical yield measured on daisy-chains with more than 20,000 connections showed a yield of more than 75% and very limited drift following preliminary environmental reliability tests".

These results confirmed the significant industrial potential of D2W hybrid bonding technology.

→ **JOUVE ET AL., Die to Wafer Direct Hybrid Bonding Demonstration with High Alignment Accuracy and Electrical Yields**

International 3D Systems Integration Conference (3DIC), October 2019



CHARACTERIZING ELECTROMIGRATION-INDUCED DEGRADATION IN 3D COMPONENTS

As part of Nanoelec, hybrid bonding-based test structures have been characterized for further development of backside-illuminated CMOS image sensors. Scientists from CEA-Leti, ST-Microelectronics and ESRF used synchrotron radiation tomography to demonstrate proportionality between electromigration (EM) induced void volumes and time-to-failure related to vias redundancy and the microstructure. *"We observed a conventional failure by voiding BEOL metal levels, but not hybrid bonding metal levels. Process induced bonding voids have no impact on the robustness of the analyzed samples. These results confirm that this type of hybrid bonding stack is immune to electromigration"*, explained Stephane Moreau (CEA-Leti).

In the 1960s, soon after the development of the first integrated



View of the vacuum chamber of ESRF's ID16A tomograph, on which characterisation of the hybrid bonding was carried out on test structures. © Cloetens/ESRF

circuits, the EM phenomenon had already been considered as critical for the future of the microelectronics market. *"More recently, hybrid bonding processes have reached a mass-production maturity, but the aggressive scaling of interconnect dimensions and ever increasing current densities means that EM-induced degradation remains a topic of interest"*, Moreau explained.

→ **MOREAU ET AL.,**
Correlation between Electromigration-Related void volumes and time-to-failure by high resolution X-ray tomography and modeling

IEEE Electron Device Letters
(Volume: 40, Issue: 11),
November 2019

DOI: 10.1109/
LED.2019.2945089

APPLYING 3D TECHNOLOGY TO SMART IMAGE SENSORS

Scientific and technological work undertaken as part of Nanoelec has indicated the possibility of producing more complex image systems with three levels of stacked images, for capturing light to deep processing (date processing, AI, VR/AR and memory). At the Advanced SiP Technology conference (USA, June 25-27, 2019), Jean Michailos, senior program manager at STMicroelectronics, demonstrated how parallel hybrid bonding combined with sequential stacking

are complementary for the complex 3D architectures required for the next generation of image sensors. *"3D Sequential architecture may save up to 40-60% of the area on dies compared to 2D"*, explained Jean Michailos.

"Sequential stacking and hybrid bonding provide more scalable solutions compared with direct or hybrid bonding, which is currently used, but such a complex stack still requires further development", he added.



→ **J. MICHAILOS,**
Innovative Fine Pitch Architectures dedicated to Image Sensors: from Hybrid Bonding to 3D Sequential integration
Invited paper, Advanced SiP Technology conference in June 2019



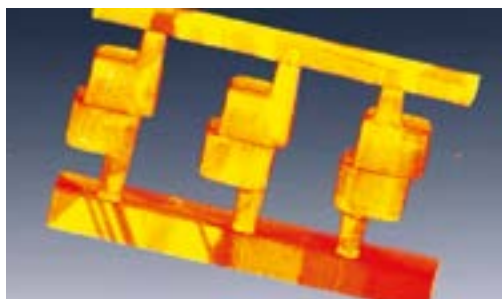
Theses defended in 2019

Reducing interconnection pitches

The creation of new 3D architectures requires a thorough understanding of the effects linked to the densification of interconnections and to technological processes, particularly plate-to-plate assembly processes.

Among the existing techniques, direct hybrid bonding Cu-SiO₂ offers excellent robustness and a density in the order of 10⁶ interconnections/cm² for a pitch of 10 μm. Switching to an interconnection pitch of 1.44 μm would mean this density could be multiplied by 50. As part of his thesis, Joris Jourdon studied direct Cu-SiO₂ hybrid bonding, using electrical measurements and aging tests on test vehicles with various interconnection pitches. An advanced morphological characterisation of the bonding pads of different sizes has enabled a correlation between the integration robustness and the interconnection pitch to be established.

For example, variants of bonding annealing and passivation have been tested in order to lower the thermal budget of bonding annealing and guaranteeing the compatibility of the “hybrid bonding” technological brick with the entire integration. Joris Jourdon also demonstrated that direct bonding was insensitive to aging by electromigration up to a bonding pitch of 1.44 μm.



Bonding pitch of 1.44 μm developed during Joris Jourdon's PhD. © CEA

JORIS JOURDON

3D integration by hybrid bonding: Challenges of interconnection pitch shrinkage

Thesis defended on November 19, 2019, at the University of Bordeaux, in partnership with the Laboratoire de l'Intégration du Matériau au Système (Talence, Gironde).

Testing and characterizing high-density 3D interconnections

The development of 3D technology brings about high interconnection densities (pitches in the range of μm), which is promising in terms of performance gains. While the prior art is between 5 and 10 μm, such architectures at densities in the order of micrometers require the characterisation of technologies and the testing of application circuits that are usually well separated.

Imed Jani has developed test vehicles to intricately characterize hybrid bonding technologies, in particular the alignment of wafers and/or dies. The structure allows for characterisation of the alignment due to a certain number of defects, in order to optimize the technological process. This structure also enables measurements of the electrical characteristics (R, L, C) of the 3D interconnections. Lastly, this same structure is also used to characterize 3D interconnections in an application circuit connected with its test infrastructure.

The testing of application circuits uses standard techniques based on BIST (Built-In-Self-Test), SCAN and JTAG structures, which enables dies to be sorted after production. The work as a whole has led to numerous publications and to a joint development between the CEA and STMicroelectronics.



After the thesis defense by Imed Jani. © DR

IMED JANI

Testing and characterisation of high-density 3D interconnections

Thesis defended on November 28, 2019, at The Université Grenoble Alpes, as part of the electronic, electrotechnical, automatic, signal processing doctoral school and in partnership with CEA-Leti.

Silicon photonics

CHRISTOPHE KOPP

*Director of the
Nanoelec Silicon
Photonics program*



Look & outlook

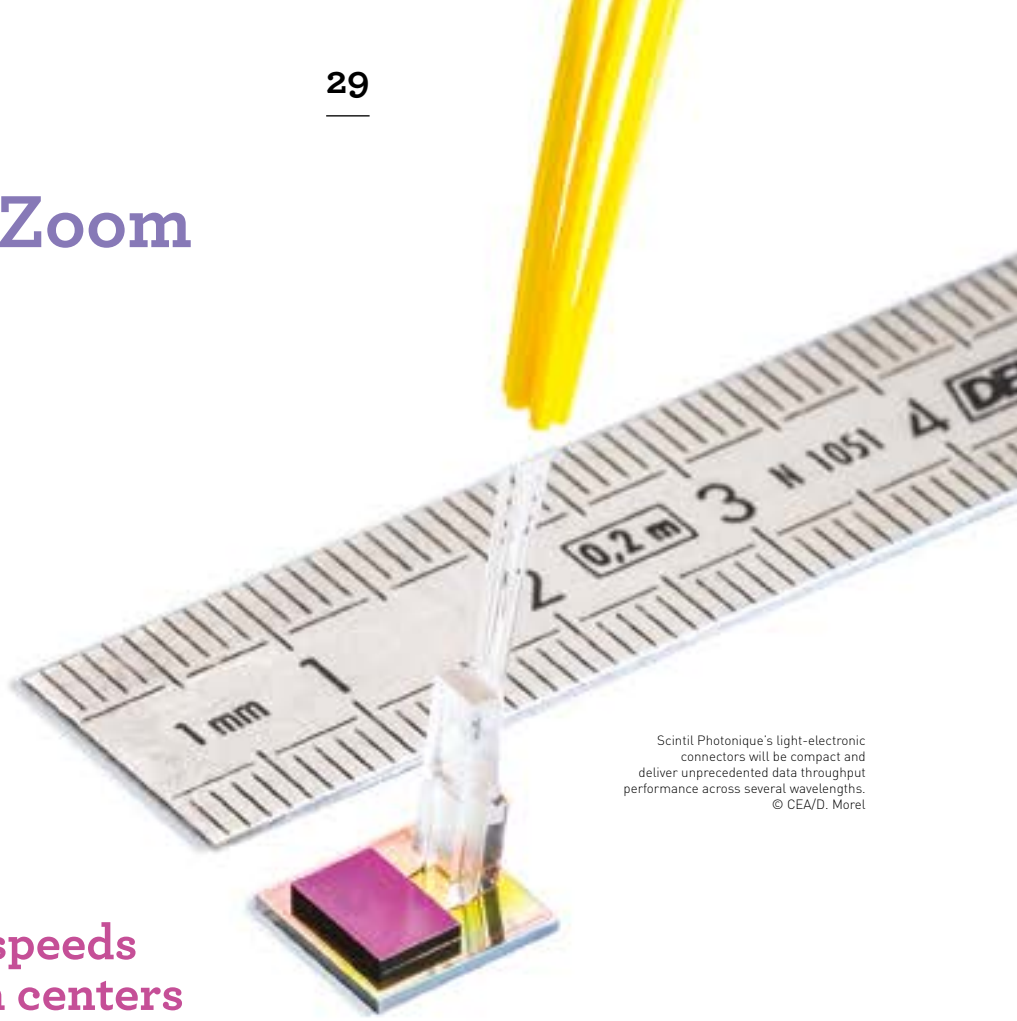
Silicon photonics is a key technology to support the growth of the Internet network, by ensuring increasingly dense and rapid digital data transfers over optical fiber. The Internet now connects billions of users, but also tens of billions of connected and interactive systems and objects in real time. Today, the optical transceivers sector in the datacoms field represents the largest share of the market for this technology. Supply chains have been set up from suppliers of substrates, design companies, silicon foundries, equipment, to operators.

Beyond datacoms, new applications are emerging to exploit silicon photonics technology. This is particularly true in the field of optical sensors for automotive and transportation, industrial and medical applications, urban planning and environment and, of course, for general public activities. While the advantages of optical sensors are well known (selectivity, speed, precision etc.), silicon photonics enables them to be radically miniaturized to allow widespread deployment. Indeed, silicon photonics makes it possible to integrate thousands of optical functions on the same chip, thus reducing the cost of the final system (simplified assembly, reduced electrical consumption, and decreased size/weight of products).

In this new context, light can be used for three very different functions, such as scanning a scene by an embedded Lidar, converting a detection signal with a miniature optical gyroscope, or analyzing data with a neuromorphic processor. Thus, following requests by our industrial partners, we are supporting the emergence of these applications by developing our silicon photonics technology. Our technology today benefits from major technological assets such as ultra low-loss silicon guides, superimposed level of silicon nitride guides and laser integration. In addition, it also offers a whole library of mature components and a design environment capable of managing these new complex circuits.



Zoom



Scintil Photonique's light-electronic connectors will be compact and deliver unprecedented data throughput performance across several wavelengths.
© CEA/D. Morel

> High speeds for data centers

Launched in 2018, the start-up Scintil Photonics, which embeds technologies developed as part of the NANOelec Silicon Photonics program, raised €4 million during a first round of funding in September 2019.

Scintil Photonics develops silicon photonics circuits that incorporate all the elements necessary for the transmission and reception of data at very high speeds. The first products will support up to 800 Gb/s and will target the market of fiber communications networks for storage or computing centers, which are large users of optical transmitters to connect

tens of thousands of servers. This growing market is increasingly turning towards integrated photonics solutions due to the increase in transported throughputs (near electronic-optical integration, multiplexing of several wavelengths) and increased volumes associated with more competitive price expectations (historical technologies that required manual assembly of parts are no longer sufficient).

NANOelec assisted the start-up in the production of III-V/Si integrated circuit prototypes based on technological building blocks such as wafer bonding, the production of the III-V part on sili-

con, the transfer of certain technological building blocks to a production foundry and support for design and testing.

The integration on silicon developed in the program is the core of the startup's technology. This integration enables the creation of an externally modulated laser whose expected performance is state of art and uses a process with low production costs. 2019 saw the creation of the first demonstrators, currently being tested, as well as the preparation of several building blocks of the design and manufacturing process. •



> World first for photonics at an industrial scale

Thanks to mask characterisation campaigns, Daphne/Pic50 technology was validated in 2019 by the complete integration of active silicon components (modulator and photodiodes), passive components (waveguide, multiplexer, network couplers) with silicon nitride.

This is a world first on 300 mm wafers. It positions Nanoelec at the state of the art in the photonics field. This platform is currently used for the manufacture of the Acturus mask which carries the contributions of Lot 3 (gyroscope and Lidar circuits). (Read below the summary of the paper: "Silicon photonics technology for 400 Gbits/s applications"). •

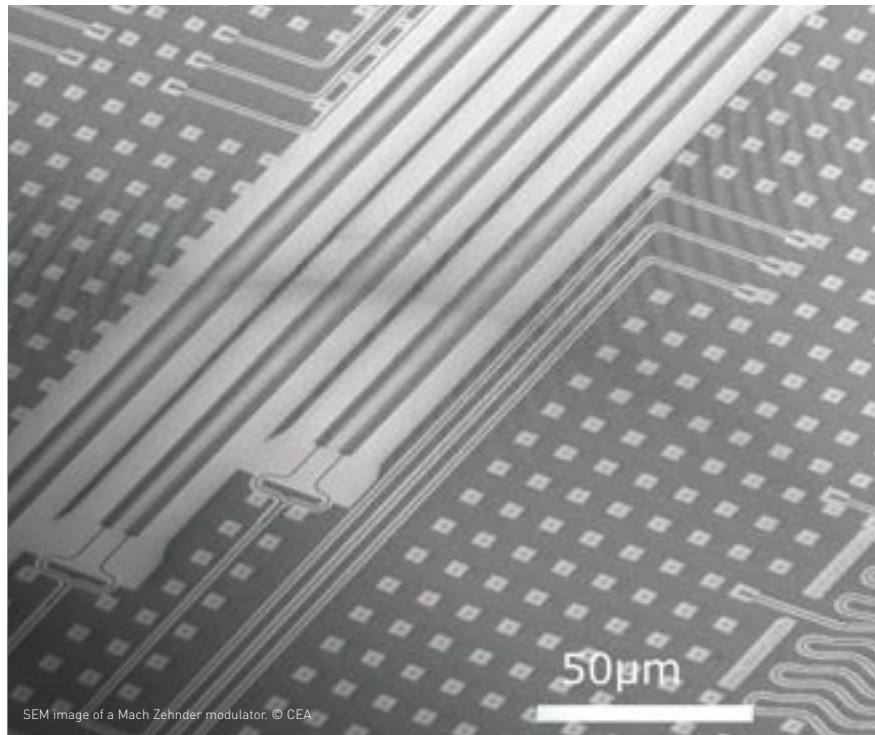
A step forward for silicon photonics technology

The latest developments of the CEA-Leti silicon photonics process flow (production & integration) under Nanoelec were presented at the Photonic West (February 4-6, 2020, San Francisco, USA) and Optical Fiber Communication (March 10-12, 2020 San Francisco, USA) conferences.

Specifically, a process was developed to integrate two layers of optical waveguides –Si and

SiN– with active components (modulators, photodiodes and III-V laser sources).

Furthermore, with the implementation of Mentor Graphic's Lightsuite Photonics compiler, it is now possible to automate the placement and routing operations of thousands of individual components in order to design advanced applications such as high-speed interconnections, Lidar and neuromorphic computing. •





Key publications



UNPRECEDENTED RESULT ON LOSSES IN SILICON WAVEGUIDES

Developments of low-loss silicon guides, achieved in recent years on an exploratory basis by the CNRS-LTM teams as part of the Nanoelec/ Photonics program, have been successfully transferred to the CEA-Leti photonics process flow. This enables to produce waveguides that achieve unprecedented loss.

"We applied a smoothing annealing to the waveguide that results in practically no morphological deformation.

We achieved record-low losses at 1310 nm with 0.1 dB/cm for single mode waveguides, with the performance of the other devices of the process being preserved", explained Quentin Wilmart (CEA-Leti) who presented this result with his CNRS-LTM colleagues at IEEE Group IV Photonics (August 2019, Singapore). "The annealing step can be introduced into the production process of the 200 mm photonics structures without any degradation in the complex devices", he specified.

GFP2019
GROUP IV PHOTONICS

→ **Q. WILMART ET AL.**
Ultra low-loss silicon waveguides for 200 mm photonics platform
GFP, 2019
DOI: 10.1109/
GROUP4.2019.8925610



LOW-LOSS WAVEGUIDES FOR NONLINEAR AND QUANTUM APPLICATIONS

At the Photonics West Conference (January 2019, USA), a team from CEA-Leti, Grenoble-Alpes University, CNRS-LTM (acting together under the Nanoelec Photonics program) and the Ecole Centrale de Lyon presented technological advances on the production of low-loss Si and SiN waveguides for nonlinear and quantum optics applications.

"Silicon-on-insulator (SOI) technology is an interesting application for on-chip entangled photon pair sources that can be used for quantum cryptography and computing, while SiN-on-insulator (SiNOI) technology is promising for high-power photonics as well as for generating Kerr frequency combs with several target applications in sight, such as atomic clocks, on-chip spectroscopy, and terabit coherent communications", explained Corrado Sciancalepore, who directed two PhDs on the collaboration before being

hired by Soitec. "In both cases, ultra low-loss optical waveguides are required to obtain efficient nonlinear sources along with the photonics circuitry needed for quantum applications", he explained.

The collaboration reported on at Photonics West regarding the production and testing of both SiN and Si waveguides featuring record-low loss values that can be used as technology building blocks for low power consumption optical frequency comb sources and more efficient entangled photon pairs generated on a chip, respectively.

In sub-micrometric Si waveguides, scattering losses are the primary source of optical propagation losses. "We introduced a high temperature H₂ annealing treatment in the Si waveguide production process to reduce the silicon waveguide sidewall roughness down to the atomic scale", Corrado Sciancalepore explained. "In this way, we obtained a reduction of the

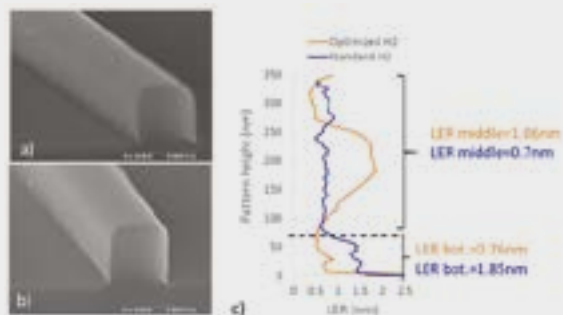
optical attenuation coefficient of the lightwave propagation down to an unprecedented record-low value for single-mode high-confinement strip waveguides in the C-band at 1,550 nm".

In terms of SiN photonics, N-H bond overtone absorption losses in the film is the limiting factor for achieving low losses. "We developed a tailored SiN deposition method, which controls tensile strain and minimizes the hydrogen content in the deposited film. Such a film provides the devices with the right specification to underpin Kerr frequency combs", Sciancalepore explained before adding that "more recent results combining this film deposition technology with cutting-edge etching and annealing treatments resulted in ultra low-loss lightwave propagation in tightly confined SiN waveguides, with record-low attenuation coefficients down to a few dB of loss per meter."

→ C. BELLEGARDE ET AL. Technological advances on Si and Si₃N₄ low-losses waveguide platforms for nonlinear and quantum optics applications

Proc. SPIE OPTO 10933, Advances in Photonics of Quantum Computing, Memory, and Communication XII, 1093309 (2019)

Doi: 10.1117/12.2508617



a) Tilted SEM cross section images of the STRIP waveguide profiles after a) standard and b) optimized H₂ annealing; c) Line edge roughness measured by AFM along the STRIP sidewalls after the standard and optimized H₂ annealing treatment. © DR

GERMANIUM FOR PHOTODETECTORS AND LASERS



Best Paper Award of IWJT-2019 award ceremony: Philippe Rodriguez (CEA Leti) and Satoshi Shibata (Program Chair). © Frédéric Mazen (CEA Leti)

Work on the establishment of CMOS ohmic contacts compatible with Germanium-Tin alloys (under Nanoelec/Photonics program) received the “Best article” award at the International Workshop on Junction Technology (IWJT, June 2019, Japan). “This award is for the tremendous work done by Andrea Quintero (CEA Leti) in particular during his thesis”, said Philippe Rodriguez (CEA Leti), project manager for Nanoelec. “Our work identifies possible ways to make contacts for future active silicon components such as ultra-sensitive photo-detectors or even Germanium-based lasers”.

The collaboration, made up of researchers from CEA-Leti, CNRS, Grenoble Alpes and Paris-Saclay universities, gave a presentation in Japan on the physico-chemical properties of Ni-based alloys for making

GeSn contacts. In particular, the addition of Pt or Co to modify the properties of Ni-based contacts and their thermal stability was discussed during the presentation.

“We have shown that the addition of an alloy element, Pt in particular, can significantly improve the thermal stability of the contacts. This is a crucial technological barrier for GeSn-based devices”, explained Andrea Quintero, first author of the paper (Quintero2019, Quintero2020).

Mr. Rodriguez’s team had already received an award (the best student article) at this same conference, in 2015, for its results on CMOS compatible contacts on III-V materials, results that have been successfully implemented for hybrid lasers (Szelag2017, Szelag2019).

- **B. SZELAG ET AL.**
Hybrid III-V/Si DFB laser integration on a 200 mm fully CMOS-compatible silicon photonics platform
2017 IEEE International Electron Devices Meeting (IEDM 2017), 24.1
- **B. SZELAG ET AL.**
Hybrid III-V/Silicon technology for laser integration on a 200 mm fully CMOS-compatible silicon photonics platform
IEEE J. Select. Topics Quantum Electron. 25, 8201210 (2019)
- **A. QUINTERO ET AL.**
Effects of alloying elements (Pt or Co) on nickel-based contact technology for GeSn layers
19th International Workshop on Junction Technology (IWJT-2019)
- **A. QUINTERO ET AL.**
Impact of alloying elements (Co, Pt) on nickel stanogermanide formation
Mater. Sci. Semicond Process. 108, 104890 (2020)

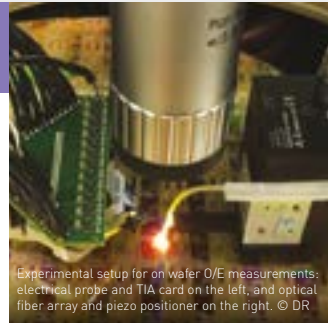


SILICON PHOTONICS TECHNOLOGY FOR 400 GBITS/S APPLICATIONS

To cope with the increasing data traffic of large computing centers, silicon photonics technology has provided a data rate up to 100 Gbit/s per connector for a few years. As a next step, a research team from STMicroelectronics and University di Pavia demonstrated, during the IEEE International Electron Devices Meeting (IEDM, December 2019, USA), a Si-photonics technology suitable for 400 Gbit/s 400G-DR4 standard operations¹. *“Moreover, the extension of our technology towards 400G-FR4*

has been achieved due to the integration of a supplementary SiN waveguide layer that enables wideband optical coupling. This technology also has a strong potential for new devices, not only for actual Si-photonics applications but also for new contexts, such as automotive sensors”, said Frédéric Boeuf (STMicroelectronics), first author of the study carried out as part of Nanoelec.

¹ FR4 and DR4 are standards for data transmission in data centers: DR4 (Direct Reach) involves distances between 500 m and 2 km whereas FR4 (Far Reach) involves distances up to 10 km and stipulates the use of four distinct wavelengths on the same fiber.



→ **F. BOEUF ET AL.**
A Silicon Photonics Technology for 400Gbits/s applications
 2019 IEEE International Electron Devices Meeting (IEDM), paper # 33.1
 DOI: 10.1109/IEDM19573.2019.8993627

LASER INTEGRATION ON A 200-MM FULLY CMOS-COMPATIBLE SILICON PHOTONICS PROCESS

In the Journal of Selected Topics in Quantum Electronics, Bertrand Szlag (CEA-Leti) et al. presented a hybrid III-V/Si photonics process they developed at CEA-Leti, as part of the Nanoelec/Photonics program. Szlag explained that “the overall integration of the hybrid laser is completed in a fully CMOS-compatible process, and leverages the large scale integration capabilities of silicon photonics. *“It is compatible with 200 mm technology and scalable to 300mm wafers*

for low-cost production process in the future”. III-V material is incorporated on top of a mature silicon photonics front-end wafer through direct molecular bonding, which enables the monolithic integration of light sources. Distributed Feedback Laser Diode (DFB) and Distributed Bragg Reflector laser reference designs are used as test vehicles for the process validation. A modular approach is used in order to minimize the impact on the already qualified silicon-based

devices. Collective III-V die bonding is proposed for this technology. *“This new technology offers the opportunity to design photonics circuits with monolithically integrated lasers on large size SOI wafers and provides convergence of silicon-based and InP-based technologies, which offers the advantages of each material. This convergence enables various applications with a unified technology”*, said Szlag.

→ **B. SZLAG ET AL. HYBRID III-V Silicon Technology for Laser Integration on a 200-mm Fully CMOS-Compatible Silicon Photonics Platform**
 IEEE Journal of Selected Topics in Quantum Electronics



Thesis defended in 2019

Integrated photonics circuits in silicon nitride for non-linear optics

Houssein El Dirani's thesis deals with the exponential rise in data traffic linked to developments in online connections between objects and people. This growth in data transmission rates calls for new technologies such as optical frequency combs that have revolutionized the telecommunications sector over the past decade. The concept of optical frequency combs also finds applications in optical detection, chemical detection and optical clocks.

Houssein El Dirani focused on the design, manufacture and characterisation of non-linear silicon nitride photonics circuits without annealing, compatible with CMOS technology, and standard in the electronics industry thereby enabling low cost manufacturing and

co-integration with other optoelectronic devices on the same chip.

"In particular, we developed a production process for Si₃N₄ films with a thickness of 740 nm, without the use of annealing and with good control of the constraints typically associated with this type of material for non-linear optics, explained Houssein El Dirani. This new approach has also allowed us to demonstrate sources of frequency combs incorporated on a chip using silicon nitride resonators coupled by abutment to a III-V DFB laser used as a pump. This proof of concept validates our process for non-linear photonics circuits in Si₃N₄ for ultra-compact and low-consumption optical frequency combs".

HOUSSEIN EL DIRANI

Development of high quality silicon nitride chips for integrated non-linear photonics

Thesis defended on October 7, 2019, at the Ecole Centrale de Lyon in partnership with the Lyon Institute for Nanotechnologies.



Pulse



BRUNO CHARRAT

*Director of the
Nanoelec Pulse program*

Look & outlook

The Pulse Program is working on new applications for the industry of the future, smart cities and silver economy.

These new products must be reliable, secure and resilient in order to find their markets and be embraced by our fellow citizens. Data management must be safe and secure.

Trust is indeed becoming a hot topic in our new hyper-digital society, as shown recently by concerns on health tracking applications or on autonomous vehicles.

It is precisely why Nanoelec Pulse program has been gradually focusing on digital trust since 2016, not only by exploring the field of cybersecurity in itself, but also the issues of operational reliability and ergonomics.

New vulnerabilities are constantly identified and are brought to public attention, creating new fears on digital technologies as medical devices, cars, industrial or urban equipment become massively connected and soon autonomous.

This bad buzz impacts badly industrial players who did not sufficiently protect their products, usually with business losses and sometimes legal consequences.

Designing secure product is not yet a common practice and cybersecurity is often viewed, by product developers, more as a constraint and less important than the overall service provided, the product costs, its performance or its ergonomics. Security is rarely standardized and not a sale argument for most customers.

But due to cybercrime development, legislative framework around cybersecurity is evolving in Europe, paving the way to new cybersecurity techs and tools.

With its partners, Pulse demonstrates the value of solutions powered by new technologies through five major projects. Security-by-design is indeed becoming a new requirement for digital systems.

These projects are on the safety of autonomous vehicles, new security hardware components, and tools for industrial IoT security.

Pulse also works on new tools for a safe and secure aging place for elders.



> IoT and security: Reliable and wireless industrial systems

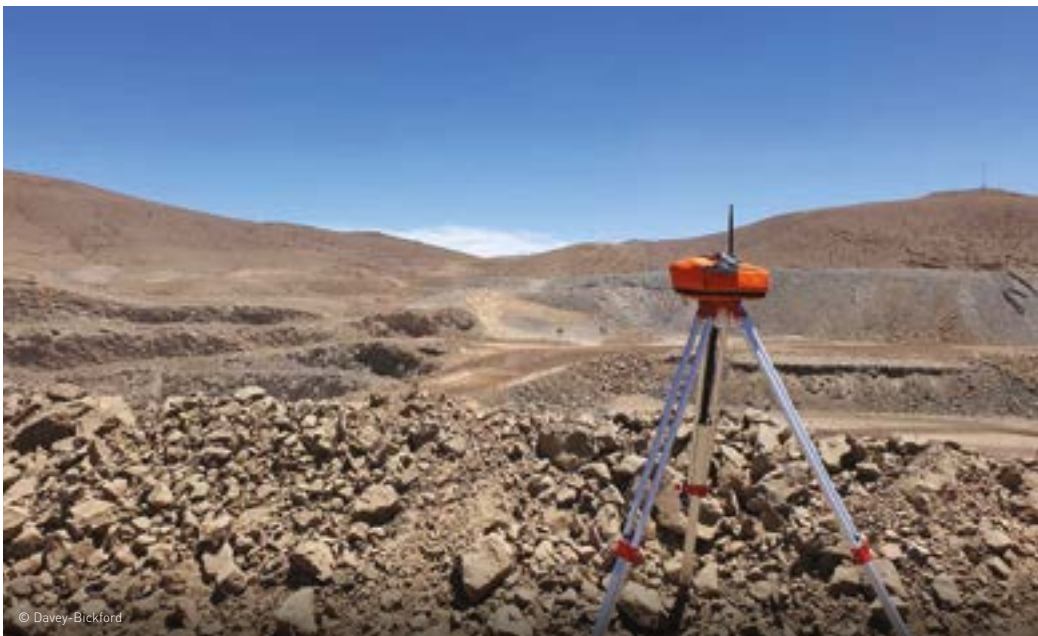
In May 2020, CEA-Leti and Davey Bickford, a French-based company and a world leader in explosion solutions for mining, presented a wireless detonation system designed to increase productivity and safety in open pit mines.

The system, developed as part of Nanoelec, includes electronic detonators with two-way radio modules that can be placed wirelessly on the surface of a mining pit. This wireless network communicates with a digital

blasting system located a few kilometers from the blasting zone and is controlled by a wireless communication protocol specifically developed and optimized to ensure the safe, reliable and synchronized operation of hundreds of detonating elements in open pit mines.

With its main plant located in France (Yonne), Davey Bickford Enaex is the world leader in explosion solutions for mining, quarries, tunnels and construction. "The project that we are carrying out with the CEA

within Nanoelec spans several years. In particular, it aims to improve the connectivity of detonators (increased communication speed, wireless connections, etc.) and we have just crossed an important milestone with the strengthening of our catalog of innovative security products and services that are easier to implement in the field, and in the backdrop of sustainable development", explained Nicolas Besnard, Director of Technology & Systems at Davey Bickford. •



© Davey-Bickford



IoT for inclusive society: Greeting the hearing impaired

Easy to install and to use, Samba is a fast and fluid instant speech transcription system that facilitates the reception of hearing-impaired persons, in particular students at the university.

"Speech is picked up by Samba's microphone and transcribed, in real time, on the screen for the person greeted, a bit like subtitles for a film", explains Nicolas Vuillerme, professor-researcher at Grenoble-Alpes University (UGA), project leader within the framework of Nanoelec.

An initial evaluation of Samba at UGA offices in 2019 made it possible to test its usability in real situations and to collect user feedback. *"A second release, which is more compact,*

portable and more natural to use, is currently being studied with a Design-to-Cost (DTC) management technique. The system can eventually be tested using a wider audience, and be used for other purposes such as real-time translation or transcription of conversations in noisy environments, for example at station counters and in shops, or at business meetings", explained Nicolas Vuillerme.

Jointly designed and funded by the UGA and Nanoelec, Samba is a compact and transportable device made up of a modular subsystems consisting of two displays and a central unit, with a software application. It was designed, developed and implemented by researchers from UGA and CEA. •



The Samba device, designed to facilitate greeting and dialogue with hearing-impaired persons.
© CEA - B. Truong

Cyber-security: Open-source for processors (#Risc-V)

Nearly 120 participants from academia and industry participated in the second Risc-V Meeting, on October 1 and 3, 2019, in Paris, which was organized by Nanoelec.



Risc-V is a 32-, 64- or 128-bit instruction game architecture whose specifications are open-sourced and can be used freely by the education, research and industry communities. *"In a way, it is to the microelectronic components industry what TCP/IP is to networks or Linux is to operating systems", explained Olivier Savry (CEA-Leti), organizer of the event sponsored by Adacore, Rambus and Hensoldt. "Risc-V has distinguished itself in recent years by improving the security of microprocessors against cyber threats. Furthermore, since 2018, Nanoelec has been a member of the Risc-V Foundation with the aim of working on new secure and prototyped hardware architectures on Risc-V processors for connected devices such as the IoT, embedded systems and machine learning implementations". •*

> Cybersecurity: A reference book on the physical security of embedded systems

Developers, digital electronics engineers and students in computer science or digital electronics have a new reference for understanding the physical security of systems, which covers the architecture of processors and demonstrates the requirements of the security objectives of tomorrow.

The book 'Physical security of systems - Vulnerabilities of processors and operating techniques' (Dunod) was written by Olivier Savry, Thomas Hiscock and Mustapha El Majihi (CEA-Leti)

who are involved in the Naoelec/Pulse program. Their book provides a comprehensive overview of the vulnerabilities of devices (in particular processors, but also memories, softwares and peripheral devices) that are contained in the heart of ICT systems, as well as the attacks they may be subjected to and their impact. In November 2019, the book was awarded the prize for the best technical work at European Cyberweek, after selection by a jury made up of experts (AIRBUS Defense & Space, Nokia, Orange Cyberdefense, ESCC, Cybersecurity Centre of Excellence). •



© Dunod

Cybersecurity: Worldwide challenge for cyber hackers

Naoelec has collaborated with the CSAW, the most comprehensive student-run cyber security event in the world.

For the 3rd consecutive edition and in partnership with the New York Tandon School of Engineering, CSAW Europe 2019 was organized by Grenoble INP (November 6-8, 2019, in Valence). After 2,400 contestants from 95 countries participating in the qualification phase, the CSAW finals brought 130 finalists from 11 countries and 30 European universities together in Valence. "The goal is to offer students the

opportunity to compete on ethical cybersecurity challenges", explained David Hely (Grenoble -INP). At the same time, similar competitions were held in USA, India, Mexico, Abu Dhabi and Israel. European students held their own against teams from other continents.

Naoelec experts participated in a panel discussion titled "Women in cybersecurity", also as jury members of the competition. In addition, they had a booth and presented the activities of the Naoelec/Pulse program at the cybersecurity trade forum. •



High school students participating in the digital investigation challenge during Europe CSAW 2019.
© P. Gardin/Grenoble-INP



> Cybersecurity: Standardization of blockchain technology

Nanoelec is involved in the ISO TC307 Blockchain standardization process: Christine Hennebert (CEA-Leti) is a member of the national commission set up by Afnor, which represents France in the International Standards Organisation (ISO) and European (CEN/CENELEC).

"On behalf of Nanoelec, I am contributing to the 'Security, Privacy and Identity' study group, where we are working in particular on the concept of identity with respect to blockchain

technology and the impact on the development of the secure architecture for personal mobile devices or IoT", she explained.

This work aims to protect the identity of citizens on digital systems, especially the internet, from impersonation and tracking. One of the challenges is ensuring people's privacy on the internet. Another challenge is separating the authentication of persons on digital systems from face-to-face identification where a 'pivot' proof of identity can be requested. •



IOT for Smart Living Environments: Recommendations for healthy aging solutions

Experts from STMicroelectronics and CEA (working together under Nanoelec), the Department of Isère and the Alps Health at Home and Autonomous Technology Hub (Tasda) participated in the drafting of a white paper as part of a group of the Alliance for Internet of Things Innovation.

The white paper "IoT for Smart Living Environments: Recommendations for healthy aging solutions", presents recommendations for the deployment of connected objects in the homes of senior citizens. These recommendations cover three challenges to support healthy aging, in particular the cybersecurity aspects of connected objects and services and the privacy aspects of shared personal data. "Pilot use cases, deployed on a

large scale, make it possible to understand and respond to the needs and expectations related to ageing, demonstrating in particular that the use of connected objects, properly adapted, respects security and privacy constraints, and that technology can therefore play a key role in contributing to more active and healthier aging", explained Olivier Horbowy, Strategic Marketing, Advanced Systems at STMicroelectronics, in this white paper. •



> IOT for home safety and autonomy for seniors

Since 2017, the European ActiVage project has aimed to assess the capacity of digital solutions to empower senior citizens in their living environments, to design these digital solutions by uses, and to assess their acceptability and impact on the organization of senior home care. ActiVage includes 12 experimental sites in Europe.



The French site, based in Isère, is managed by Nanoelec and the Department of Isère. The goal of the deployment site in Isère is to study a continuum of care that combines human and technical assistance, bridging the different phases of senior citizens' lives to limit loss of autonomy and avoid unnecessary re-hospitalizations. For this study, the partners of the site implemented a scalable solution that adapts to the three main stages of aging. Three profiles were defined for the experiment: active seniors, frail seniors and hospitalized seniors.

The work was further advanced for various components of the

project in 2019, namely the deployment of the home automation solution and the evaluation of uses, the interoperability of technological solutions as well as the devices security.

In 2019, Nanoelec, through STMicroelectronics and CEA, in particular, actively participated in securing the AIOTES interoperability layer of the ActiVage project, which includes a security and privacy module. The ActiVage solution was installed in an experimental capacity in the homes of 60 seniors living in Isère.

As part of ActiVage, Nanoelec participated in the organization

of a day entitled 'Housing equipment: Health, security, comfort or independence?', November 5, 2019. Over 120 professionals discussed the experiences of various French deployments aimed at equipping housing to support home care for seniors. Fifteen SMEs and start-ups in the field were presented. Two round table discussions (with Intermutuelles Assistance, Korian Solutions, Harmonie Mutuelle, Les Séniories and the Fédération Française de Domotique) were organized around the topics of "Diagnosis, prescription and installation" and "Services in equipped housings". •



Autonomous vehicle security

Faced with the race involving all car manufacturers, autonomous solutions have entered into a strong phase of technological progress.

The goal of the Autonomous Vehicle Security (AVS) project carried out under Nanoelec/Pulse program is to integrate, develop and promote technology building blocks for context capture, for the security of autonomous vehicles.

"In 2019 we developed our perception system, in particular by adding waterway detection modules from neural networks", explained Lukas Rummelhard (Inria), AVS project leader at Nanoelec. "The vehicle's tracking trajectory planning and control systems were also improved. The various technological building blocks developed in the project have been the subject of several demonstrations, in particular of perception on an open road in Rambouillet (France), or on the circuits of IRT Nanoelec and IRT Vedecom, as part of collaborations or international conferences like IEEE IROS2018 or IV2019." •



Cybersecurity: Demonstrator for industry

Nanoelec teams presented developments made as part of the 'Industrial IoT Security' project of the Nanoelec/Pulse program during the International Cybersecurity Forum (January 2020, France).

A platform to raise awareness of vulnerabilities, cyberattack risks and the challenges of cybersecurity for industry has been developed. This allows to demonstrate cybersecurity for industrial and tertiary systems used by stakeholders in the field (energy, essential operators, etc.). Engineers under Nanoelec are able to offer solutions based on technolo-



gical developments in 'security by design'. "Our demonstrator implements a digital protective circuit twin for an electrical transformer. We can also simulate attacks on an industrial network, propose hardware

countermeasures for securing the network and deploy security settings from a connected tablet with an Android operating system", explains Pierre-Henri Thévenon, project manager at CEA-Leti. •

Cyber- security for European companies' digital transition



The availability and rapid upgrading of digital skills in European industry will be essential for the future of the European economy. Without updating their digital skills, European companies will not be able to seize future opportunities resulting from advances in areas such as artificial intelligence, future networks and augmented reality.

Mid-sized companies, SMEs or start-ups interested in developing smart applications in Europe can apply for the calls for the European DigiFed project.

Coordinated by CEA-Leti and involving Nanoelec/Pulse program, DigiFed aims to facilitate the accelerated adoption of cyber-physical systems (CPS) by companies, by providing resources of up to €55,000 as well as technical and commercial support. By opening up cross-border collaboration opportunities in Europe, DigiFed widens the scope of Nanoelec/Easytech program, which is exclusively dedicated to French partners. The first open call for applications for the European DigiFed H2020 project was launched in spring 2020. •



Key communications

CYBERSECURITY: SIDE-CHANNEL BASED DISASSEMBLING

Side-channel based disassembling (SCBD) is a powerful application of side-channel analysis that recovers instructions executed by a processor from its physical leakages, such as the electromagnetic field (EM) emitted by the chip. These attacks directly compromise code confidentiality, but they can also reveal critical information about the system to an adversary.

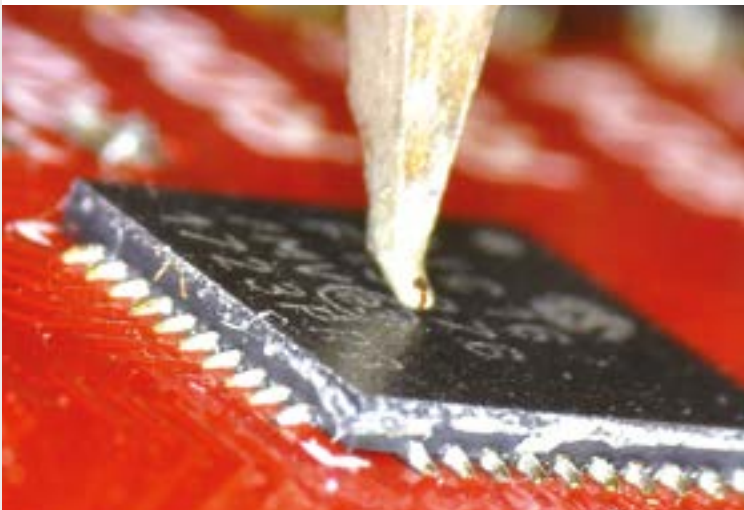
At the 18th Smart Card Research & Advanced Application Conference (Cardis, November 2019, Czech Republic), Valence Cristiani, Maxime Lecomte and Thomas Hiscock (CEA-Leti)

put forward a new approach developed as part of Nanoelec, which is a SCBD that directly focuses the bit encoding of an instruction using local EM leakage.

"We exploit a very precise bit-level leakage model and derive new algorithms from it that aim at recovering the actual bit values", the authors outline. "We also put forward strategies to automate the complex tasks of finding the best EM probe positions and combining them to improve results. On a PIC16 target, our method succeeded in recovering the bits of an instruction with an average rate of 99.41% per bit".

Compared with the state of the art, this disassembler is easier to train, recovers more information on instructions than opcode alone and requires almost no modifications to target other processor architectures.

This work has driven forward state-of-the-art attacks on instructions, and these insights have been used in the design of countermeasures in projects such as Nanotrust (a Nanoelec/Pulse project). Further work on this topic will adapt this new technique for leakage assessments, functionality checking or malware detection in embedded systems.



A microprobe close to the chip in preparation for side-channel based disassembling. Up to now, reverse code based on side channels has only been demonstrated on "simple" processors (single-core smart cards). This new technique opens the way for it to be carried out on more complex processors (for smart phones). © CEA

→ **V. CRISTIANI ET AL.**
A Bit Level Approach To Side Channel Based Disassembling

Cardis, November 2019,
Czech Republic

CYBERSECURITY : SIDE-CHANNEL ATTACKS AND SOFTWARE COUNTERMEASURES



Damien Courousse (CEA-List and Nanoelec) delivering a course at the 2019 Slim Summer school. © C. Maurice/Iriss

Damien Courousse (CEA List) was a lecturer at the SILM summer school organised in Rennes by the research Group (GdR) Sécurité Informatique. Side-Channel Attacks and Fault Injection Attacks are the two sides of the same threat: here the attacker exploits a physical access to the target device. Those attacks are very powerful because they break the standard

assumptions about the security of cryptographic primitives: by exploiting the (very) partial knowledge of the implementation of a secured component, it is possible to “break” the security of this component. In the world of physical attacks, the security assumptions provided by traditional cryptanalysis need to be reconsidered. E.g. the stream cipher AES, otherwise

considered secure, needs to be protected against such attacks. In this tutorial, Damien introduced the working principle of side-channel attacks, and discussed in-depth side-channel attacks based on power and electromagnetic observations. He showed how it is possible to recover a secret cipher key using Correlation Power Analysis and then introduced the principles of the main countermeasures against side-channel attacks. He discussed their impact on the effectiveness of side-channel attacks, and their limits as well as the existing solutions to secure software implementations against side-channel attacks.

→ D. COUROSSE. Side-Channel Attacks and Software Countermeasures

Security of software/hardware interfaces, SLIM summer school, July 8-12, 2019, Rennes, France.



CYBERSECURITY: DETECTING FAULT INJECTION ATTACKS

Fault injections are increasingly used to attack/test secure applications. In their paper presented at the Software Protection Workshop (SPRO, November 2019, UK), Ali Kassem and Yliès Falcone (UGA & Inria) defined formal models of runtime monitors that could detect fault injections that result in test inversion attacks and arbitrary jumps in the control flow. The code implementing a monitor is small relative to the entire application code. “Monitors

have formal semantics; and we have proven that they effectively detect attacks”, explained the authors on their work carried out under Nanoelec. Each monitor is a module dedicated to detecting an attack and can be deployed as required to secure the application. A monitor can run independently from the application or it can be ‘weaved’ inside the application. Our monitors have been validated by detecting simulated attacks on a program verifying a user PIN.

→ A. KASSEM & Y. FALCONE Detecting Fault Injection Attacks with Runtime Verification

SPRO 2019, November 15,
2019, London,
United Kingdom



CYBERSECURITY: PREVENTING COUNTERFEITING & ILLEGAL ACCESS TO INTEGRATED CIRCUITS



Securing integrated circuit life cycles requires authentication mechanisms in order to prevent counterfeiting and illegal access to private assets. Physical unclonable functions (PUFs) are good candidates to provide authentication services using physical signatures on chips or different kind of processors. However, PUFs can be sensi-

tive to noise and environmental conditions, thus inducing reliability issues. Digital PUFs (DPUFs), inherently robust by design, have recently been proposed, in a paper at the IEEE Computer Society Annual Symposium on VLSI (July 2019, USA) by Johan Marconot et al. (UGA/Grenoble INP and CEA-Leti). Under Nanoelec, the authors investigated the utilization, security and efficiency of interrogation circuitries for DPUFs. They proposed a circuit model (SPN-DPUF) with a first security performance trade-off, respec-

ting both security and resource constraints.

"There is an opportunity to design competitive hardware security primitives. In the future, we will focus on analysis of real-data of DPUF random structures, with more accurate performance criteria that results in the most optimized configurations for SPN-DPUF circuits. Furthermore, we should also estimate the resistance of SPN-DPUF circuits against modeling attacks", Johan Marconot explains.

→ J. MARCONOT & AL.

SPN-DPUF: Substitution-Permutation Network based Secure Circuit for Digital PUF
IEEE Computer Society Annual Symposium on VLSI (ISVLSI)

DECISION-MAKING IN AUTONOMOUS DRIVING



Christian Laugier (Inria) gave three invited talks in China last year on motion autonomy and safety issues in autonomous vehicles, based on studies he carried out under the Nanoelec/Pulse program. After a brief history of advances in the initial revolutionary concept of the 'automobile' in the last century, Christian emphasized the exciting new concept of 'automated driving'.

"The issues of autonomous vehicles are strongly dependent upon the capabilities and performance of both embedded perception and decision-making systems. It is possible to address these important issues by mixing Bayesian and machine learning approaches. This is what we developed under Nanoelec", Laugier explains, referring to the 'multi-sensor on-board perception' research carried out as part of the Nanoelec/Pulse project on autonomous vehicle safety. "We developed a new method called 'embedded Bayesian perception' (patented by Inria-IRT

Nanoelec, with licenses sold to Toyota", underlines Laugier, before adding that a technology transfer was carried out in 2019 under Nanoelec, in the context of developing autonomous public transport.

"This method makes it possible to process dynamic scenes, taking into account the uncertainty and predicting future changes in the scene observed within a time frame of 3 to 5 seconds. It makes it possible to assess what the risks of collision are over this time frame at all times".

→ CHRISTIAN LAUGIER, invited talks

IEEE/RSJ International Conference on Intelligent Robots and Systems (IROS 2019, November 2019, China) & World Robot Conference (WRC August 2019, China)



IOT FOR SMART LIVING ENVIRONMENT: REAL-LIFE EXPERIMENTATION OF SYSTEMS COMBINING HUMAN AND TECHNICAL ASSISTANCE FOR HEALTHY AGING

A collaborating team from CEA-Leti and the Alps Health at Home and Autonomous Technology Hub (Tasda) reported on the advancement of two interconnected large-scale trials investigating the interaction between technology and aging population at the IAGG conference. Isèreadom, a French-financed project and the French node of Activage, and the Horizon 2020 program are both implemented in the French department of Isère as part of Nanoelec.

Isèreadom is evaluating an innovative organization of the social care system that combines human and technical assistance based around a care manager and a digital notebook. The Isère deployment site of Activage aims to create a continuum of care, bridging different

moments of a senior person's life to limit losses in autonomy.

"We work on three profiles: active seniors, frail seniors and seniors in short-term hospitalization", Alain Chambron (CEA-Leti), one of the project contributor, explains, after the projet has been presented at the 2019 conference of the International Association of Gerontology & Geriatrics (Taiwan, 2019).

Isèreadom follows 370 users and caregivers (nurses, managers and assistants). With 80 living units already installed, the Isère deployment site is one of nine ongoing Activage sites across Europe, representing 240 users and caregivers.

"For volunteers in each population, we set up a modular and personalized home IoT pack that follows evolving needs¹, detects early signs of loss of autonomy,

thus enhancing safety, comfort, energy saving and social links", Chambron adds.

"Such large-scale deployments show the complexity of commissioning heterogeneous home automation solutions and platforms in a safe and secure way, and that comply with GDPR.

A secure infrastructure to monitor the units and a link to Activage's ecosystem (AIOTES) are key in taking advantage of the information provided by the devices. Isèreadom aims to change public policy, global care organization and digital tools with a step-by-step demonstrator. Users appreciate this opportunity to strengthen the security and quality of life at home", he says.

¹ Seniors' needs evolving with their level of dependence, where it might be advantageous to introduce a population to ITCs early enough to avoid issues in the advanced stages of aging.

→ LOUBIER ET AL. TAIPEI

October 26, 2019 - <https://www.iagg2019.org/>

2019 conference of the International Association of Gerontology & Geriatrics

PowerGan



PHILIPPE PANTIGNY

*Director of the Nanoelec
PowerGan program*

Look & outlook

The development of gallium nitride (GaN)-based semiconductors improves the performance and operational reliability of increasingly compact power converters, be it for power delivery of few watts (laptops or desktops) or for applications requiring few kilowatts (power supply for computer servers or powered mobility).

These gains are essential in meeting the challenges of energy transition. For example, in the “connected devices and small electrical devices” market segment, the International Energy Agency (IEA) forecasts a world electricity demand of approximately 1,000 TWh/year by 2040*. A 1% gain in the energy efficiency of products in this market segment would reduce this demand by 10 TWh, which is equivalent to the annual production of around 20 nuclear power plants.

Given its promising electronic properties for energy conversion, GaN power electronics innovations has been thriving all around the world and it is now a very competitive domain. Teams brought together through the POWERGAN program are contributing to the development of GaN on silicon (GaN/Si) technologies in order to overcome the technical and economic limitations of current power component technologies available in silicon and gallium nitride for the 100-650 V segment.

POWERGAN's aim is to strengthen and structure a national ecosystem of industry and academia in order for stakeholders from French and European industry to gain a foothold in markets in different sectors, ranging from individual electronic equipment to electrification of private and mass transport**.

Launched in 2017, the programme is based on a disruptive technology on 200 mm wafers compatible with mass production. This technology transfer is at the heart of the GaN/Si pilot line that STMicroelectronics is implementing in its factory in Tours France. We are improving the performance and reliability of a first generation of 650 V components and preparing for the next generations. In order to further drive the miniaturization of systems, we are working on the architectures of disruptive converters. We are also developing tools and methods to co-design component and system architectures to accelerate technological adoption, especially for harsh environments such as automotive applications.

These objectives require a multidisciplinary and multi-partner research strategy. Nanoelec is particularly well suited to accelerating the removal the barriers between devices and systems.

The results obtained in mid-2019 for GaN diodes and at the end of 2019 for GaN transistors will enable us to launch new collaborations in 2020. We mainly target collaborations with industry and technological research institutes (IRT) and institutes for energy transition (ITE) in fields such as aeronautics and space, photovoltaics and mobility, and from smartphones to heavy-load transportation.

* Source: <https://www.iea.org/data-and-statistics/charts/>

** The firm Yole estimates in its report “Power GaN 2019: Applications, players, devices, and technologies” that the market for power GaN components will exceed US\$350 million in 2024. Yole plans to enter the market for low-power charger applications, then into the automotive market by 2024, and finally into intensive industrial applications around 2030.



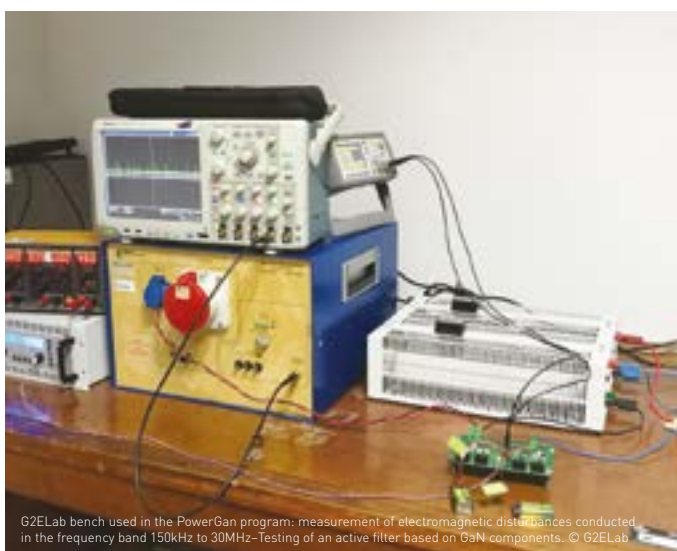
> Controlling electromagnetic interferences

Mentor graphics joins the program

A founding member of the institute since 2012, Mentor Graphics has been particularly involved in the 3D and photonics programs.

In 2020, the company joined the Nanoelec/Powergan program.

"We bring to the program a capacity to build a Digital Twin of GaN power converters, enabling system and technology co-optimization, testing of accuracy against measurements and using it throughout its full life cycle, as well as getting ready to respond to the acceleration of the market", explained Jean-Marc Talbot senior expert at Mentor Graphics. •



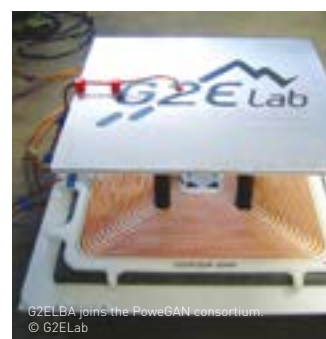
G2ELab bench used in the PowerGan program: measurement of electromagnetic disturbances conducted in the frequency band 150kHz to 30MHz-Testing of an active filter based on GaN components. © G2ELab

In June 2019, the Nanoelec/Powergan program began collaborating with the electrical engineering laboratory G2ELab (CNRS & UGA/Grenoble-INP) on GaN/Si component-based power electronics.

"We bring cutting-edge expertise to the Nanoelec partners in the co-design of innovative power converters: electrical and thermal simulation, electronic design, packaging, and testing", explained Jean-Luc Schanen, co-manager of Power Electronics team from G2ELab.

G2ELab's research will now be able to draw upon the technologies developed through Powergan,

in particular for components, packaging and simulations. *"The first challenge we will face together is the control of the electromagnetic disturbances generated by the rapid switching of GaN/Si components", explained Jean-Luc Schanen. •*



G2ELBA joins the PoweGAN consortium. © G2ELab



> A new context for the Powergan program

STMicroelectronics is participating in the Nanoelec/Powergan program to develop a disruptive 200 mm GaN technology for power applications that will be transferred to its pilot line at its manufacturing site in Tours France.

For this global electronic leader, this is a key building block in its power-switching device ecosystem, along with its recent moves involving TSMC and Exagan. Filippo Di Giovanni, Manager of Strategic Marketing, Innovation, and Key Programs at the Power Transistor Macro-Division of STMicroelectronics provides more information on these activities:

What is STMicroelectronics' position on power switching devices?

We are extremely optimistic regarding the opportunity for growth in both the SiC and GaN wide bandgap power electronics markets and we are investing appropriately to build solid and reliable supply chains to ensure that ST can be a global leader in both. With our tailored initiatives, we are taking steps to address the main application clusters in the power electronics market with appropriate technologies to meet the unique needs of those applications. The power GaN-on-Si technology from ST is ideal in providing high-efficiency

and high-power applications, including automotive on-board chargers and DC-DC converters for hybrid and electric vehicles, wireless charging and servers.

At the beginning of 2020, STMicroelectronics announced an agreement with TSMC, one of the world's largest foundries, and also announced the acquisition of the French innovator Exagan. What is your new roadmap for GaN technologies?

Our goal with GaN is to replicate our success in SiC by quickly establishing a leading position, because we are strongly convinced that this technology will feature heavily within our important strategic pillars, particularly in terms of energy management (industrial and automotive). As a result, we are establishing our

technology platform and formulating our manufacturing strategy.

The collaboration with Nanoelec is key to our 200 mm GaN power technology hub and pilot line in our Tours manufacturing site in France, which will be the backbone in building a comprehensive product lineup.

At the same time, we are also working with TSMC and Exagan to accelerate the large-scale adoption of GaN power technology for fast-growing markets.

The acquisition of the French innovator Exagan provides us with broader expertise in epitaxy, product development and application expertise. Exagan will continue to implement its product roadmap and will now be supported by ST in deploying its products.

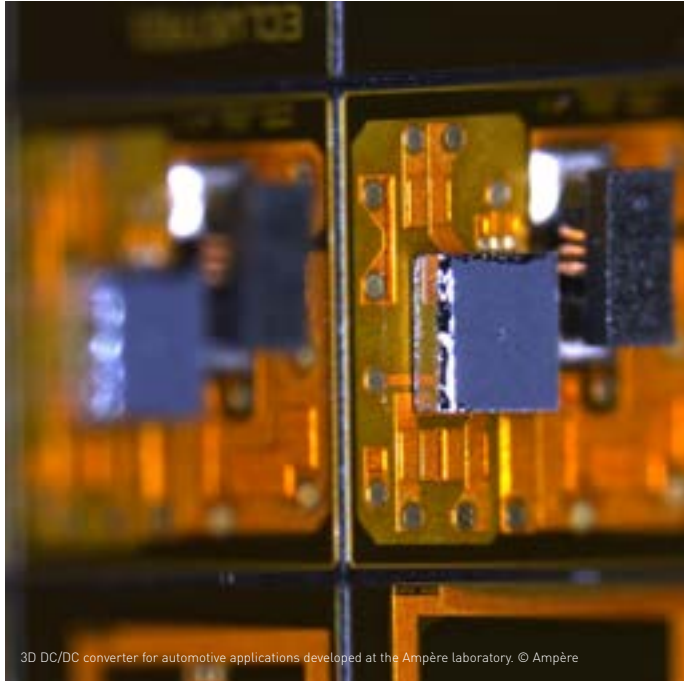


Will these new deals change your roadmap for Power GaN with Nanoelec?

There will absolutely be no changes at all. We are firmly committed to continuing our fruitful collaboration for the development of the next generations of GaN power devices within the IRT Nanoelec /Powergan program.

The ongoing developments of 200 mm wafers of advanced 650 V transistors and Schottky diodes based on the MIS Gate Recess approach look promising. The first trials have confirmed the feasibility of a transfer to our ST Tours GaN pilot line beginning in 2021. We know from our experience in power silicon and silicon carbide that GaN power components will improve significantly in the future.

We therefore strongly support the Powergan roadmap for advanced GaN power components. We do believe that Powergan gathers the multidisciplinary expertise from industry and academia required to start moving GaN devices towards the theoretical limits of the GaN material while, at the same time, devising extra and high value-added “smart” functions for end-users. •



3D DC/DC converter for automotive applications developed at the Ampère laboratory. © Ampère

> Towards ‘smart’ switches in 650 V

The Nanoelec/Powergan program launched a collaboration with the Ampère laboratory (Insa Lyon/CNRS/University Claude Bernard Lyon 1/Ecole centrale de Lyon) in 2019 and focused on power electronics based on gallium nitride components epitaxied on a silicon substrate (GaN/Si).

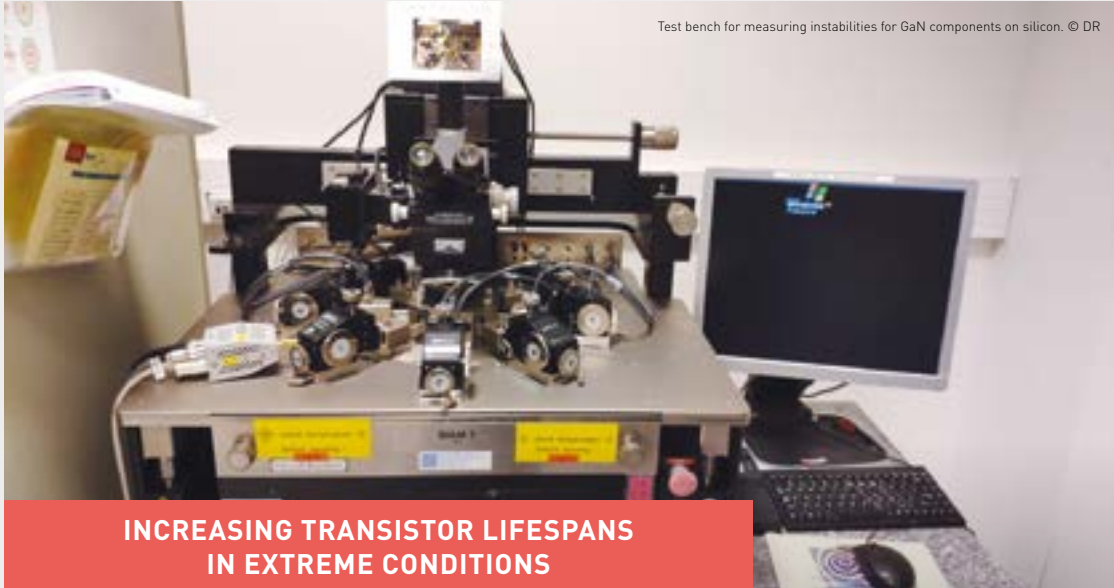
While the program focuses on the development of a first generation of discrete GaN/Si switches

(a transistor or a diode per chip) at 650 volts, the arrival of Ampère at the Nanoelec makes it possible to think ahead.

“For our part, we are helping to prepare a next generation of ‘smarter’ switches, embedding additional control, protection and monitoring functions on the same chip”, explained Bruno Allard, University Professor at Insa Lyon and Director of the Ampère laboratory. •



Key publications



Test bench for measuring instabilities for GaN components on silicon. © DR

INCREASING TRANSISTOR LIFESPANS IN EXTREME CONDITIONS

GaN-on-Si HEMT technology is undoubtedly considered as a major candidate for medium power applications (650 V rated) compared with SiC technologies. It is also considered a strong candidate for multi-MHz moderated power (<2 kW) applications. However, gate reliability and instabilities are critical issues with respect to increasing transistor lifespans, particularly when submitted to high reverse bias stresses and high forward gate voltages.

At the 2019 International Reliability Physics Symposium (IRPS) and at the 2019 International Electron Devices Meeting, Abygaël Viey reported on his research into the reliability of this technology. He is particularly interested in the instabilities of the threshold

voltage, V_{th} . *"We have demonstrated that when we reduce the gate length of the transistor, the V_{th} instabilities decrease and, consequently, the transistor lifespan increases", explains Abygaël. "Furthermore, we have also seen that the instabilities of the V_{th} under negative grid stress voltage (around -5 V) are explained by the presence of carbon atoms in nitrogen sites in the GaN, at varying distances from the grid".*

The study thus demonstrates a strong potential for the electrical characterisation of carbon-doped GaN layers, with doping very often used to increase the breakdown voltage of the transistors.

At present, there are very few means of characterizing these layers of GaN:C.

→ **ABY-GAEL VIEY (CEA-Leti, STMicroelectronics, Imep) ET AL.**

Influence of gate length on pBTI in GaN-on-Si Emode International Reliability Physics Symposium (IRPS)
USA, March 31-April 4, 2019
DOI: 10.1109/IRPS.2019.8720554

→ **ABY-GAEL VIEY (CEA-Leti, STMicroelectronics, Imep) ET AL.**

Investigation of nBTI degradation on GaN-on-Si E-mode MOSc-HEMT International Electron Devices Meeting (IEDM)
USA, December 7-11, 2019
DOI: 10.1109/IEDM19573.2019.8993588



Thesis defended in 2019

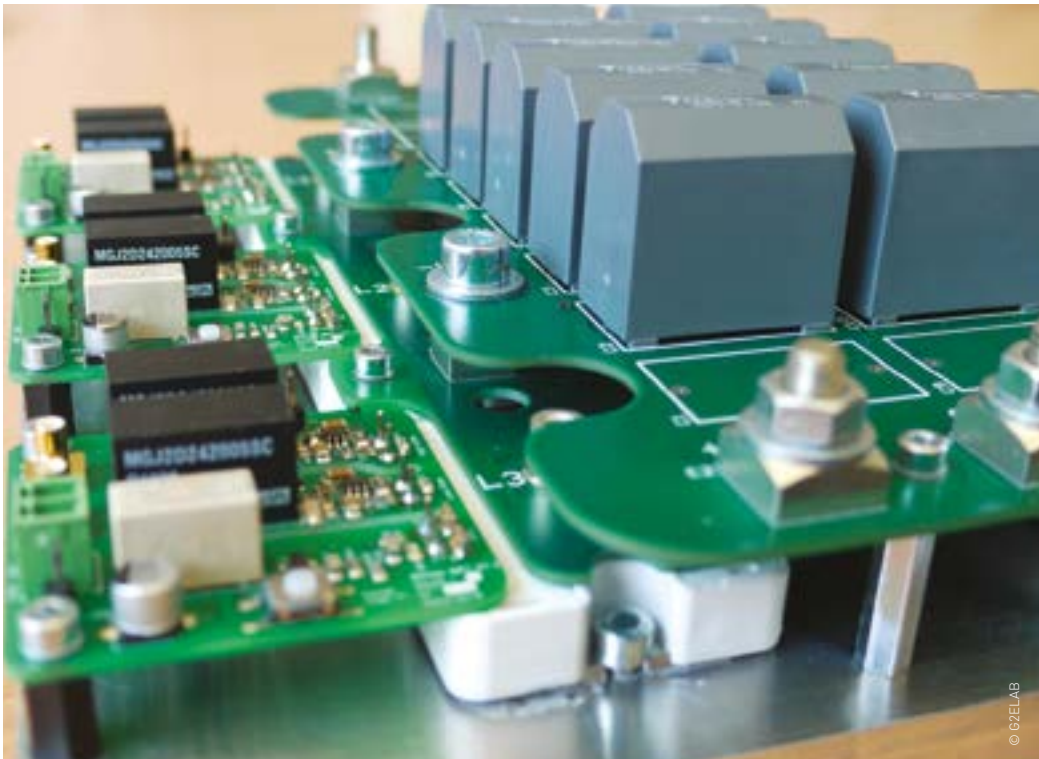
Preventing performance losses of components linked to high voltages

The work presented in this thesis focuses on the study and reduction of degradation phenomena in AlGa_N/Ga_N transistors and diodes epitaxied on a silicon substrate for power applications. The 'current collapse' refers to non-permanent degradations of the component characteristics following a stress related to a high voltage. This work involves identifying the origin and nature of these degradations in the complex structure of Ga_N components.

THOMAS LORIN

Contribution to understanding and reducing the effect of current collapse in HEMT AlGa_N/Ga_N diode structures on a Si substrate for power applications

Thesis defended on September 12, 2019,
at The Université Grenoble Alpes,
in partnership with CEA-Leti.



© C2ELAB

Human capital and education design activities



YOULA MORFOULI AND SYLVIE BLANCO

Co-directors of the Nanoelec Education & Training program

Look & outlook

Grenoble INP and Grenoble Ecole de Management have been collaborating for more than 30 years, creating joint programs and diplomas, in students and professionals education & training. This aims at developing dual engineering-managerial skills. As a result of their local links, particularly with respect to technology and innovation players, the two schools have been stakeholders in Nanoelec since 2012 as co-drivers of its training program. Nanoelec is an ecosystem of innovation and sustainable transitions in itself, based on several pillars, including human capital, which is recognized as a key success factor by the partners.

In this context, both schools have significantly integrated their educational design activities to create and test ecosystem-specific mechanisms for learning and training, in a ambitious, agile and collaborative way. Academia and industry cooperate in a “design thinking” mode through educational design

activities (from an upstream consultation to a transfer down to training operators), addressing all the required skills (from R&D to setting up businesses and disseminating innovation). Sharing their vision as well as learning resources, through demonstrators and labs, they created real universes of experience.

The results are impressive for several reasons: relevance and schools know-how in terms of experiential learning approaches (serious games, simulations, immersive worlds and real collaborative projects); quality and relevance of results achieved through co-development of activities combining academic and industrial partners, initial and continuous training, engineers and managers together; ability of the program to mobilize the ecosystem and react to emerging or difficult-to-address skills requirements (i.e. sustainable electronics or efficient R&D teams); experimenting with different methods of hybridizing skills in a sector shaped by its change dynamics and the diffusing nature of its core technologies.

In addition to this leveraging and accelerating effect, Nanoelec offers an ideal experimental environment for imagining and developing a European benchmark model for developing human capital. This model fits to the era of ecosystems innovation and addresses the challenges of technological and sustainable transitions. Attracting talent and industrial partners will be the major issue over the next five years, while also considering the impact that the COVID-19 crisis will have on the future of education, especially in terms of digitalization.



Interactive module on sustainable electronics

Students of the international master's degree "Micro and Nanotechnologies for Integrated Systems" of Grenoble-INP (UGA), Politechnico of Turin and EPFL Lausanne, used a brand new training module provided in English, during which they had to design a mobile phone incorporating micro-electronic components designed with sustainable development (greenphone) in mind.

This new educational approach was created and facilitated by experts from CEA, STMicroelectronics, Grenoble INP (UGA) and Grenoble Ecole de Management and prototyped as part of Nanoelec.

Forty master's students tested it over one day in January 2020. They worked in teams on different stages of the product life cycle (materials, design, manufacturing, use and end of life). At the end of the module, they presented a set of measures and processes to meet environmental requirements. The result was plenty of creativity and a solid demonstration that respect for the environment, through industry and technology, is crucial for young engineers involved in the sector. •



“We had a whole day in direct contact with practicing professionals. With them, we were able to work on the entire life cycle of electronic devices”, said Sarra Sfar, a student of the master's program. “Without a doubt the greatest contribution of the module was putting us in a position to think “outside the box” in order to identify radically new solutions”. “The day gave us the opportunity to grasp a multidisciplinary tool to innovate in a collaborative and creative way”, added Nazareno Sacchi, also one of the master's students.

“It is important for us to share with the young generations of engineers, in particular those whom we may recruit, our company's commitment to sustainable electronics”, explained Laurent Jamet Director of Innovation & New Ventures, Analog, MEMS & Sensors Group at STMicroelectronics who participated in the day-long event, along with four other experts in the field.



During the test day of the module on sustainable electronics in January 2020. © Grenoble-INP

“As a future engineer, I believe that I have a very important role in today's society and in that of tomorrow. In my future job, I must, of course, be able to meet people's needs with respect to digital systems, but to also respect the environment and preserve our resources such as water, energy and materials”, said Sarra. Nazareno also believes that he will work in the role of “inventor and pioneer” to bring about a “modern and environmentally friendly” society.



Awareness-building module on large instruments for characterisation

In March 2020, a brand new training module, developed under Nanoelec, was held on the EPN campus (ILL-ESRF, Grenoble, France) for 25 students from the doctoral schools of The Université Grenoble Alpes.

Developed by the teams of characterisation and training programs of Nanoelec, the module offers doctoral students an overview of the different analytical techniques by synchrotron radiation and neutron beams applied to nanoelectronics. The program included four lectures in English of three hours each, as well as a visit to the ILL. The ESRF visit was postponed due to the COVID-19 crisis. The students' evaluations of the module

yielded a satisfaction rate of 8.6/10. Six students plan to submit a research proposal to the ILL or ESRF in the near future in order to advance their thesis work. An optional session gave them the opportunity to test the serious game RNDYNEO, which was developed with the help of Nanoelec/Training program. They thus experienced a first entertaining approach to project management in R&D.

The module was also digitally adapted an experimental session in English titled 'Large scale facilities applied for nano-electronics' was offered remotely on May 15, 2020 to the 40 students of Nanotech master's program. Three engineers from ESRF and ILL joined forces

to offer two introductory courses on synchrotrons and neutrons, both on the history and basic principles of synchrotron and neutron radiation, their interactions with matter, but also on certain specific neutron and X-ray techniques for the characterisation of nanoelectronic materials and devices. A few illustrations with case studies carried out by the Nano Electronics Lab on real research subjects were also presented. Four case studies were presented to the students and they worked in groups of four on an experimental design that could solve a specific problem. The results of this study will be summarized in a report to be evaluated by the engineers involved with the module. •



The PhD students at the first module for the introduction to characterisation techniques using large scale instruments at the EPN Campus. © ILL

Serious gaming for Lean Management in industrial R&D

RNDYNEO was developed as part of the Nanoelec/Training program, and is based on a need for STMicroelectronics to train its R&D teams in Lean Management.

Its objective is to increase the performance and efficiency of the teams while making them more agile, innovative and collaborative as they operate in an increasingly complex project-mode environment.

RNDYNEO is an active teaching tool based on the experiences of the teams and combines serious games, real cases, in-situ applications and testimonials.

The project was formalized in 2018 between STMicroelectronics, Grenoble Ecole de Management (GEM) and Grenoble INP (UGA). Test sessions were carried out with ST employees at the end of 2018. *"In 2019, RNDYNEO was incorporated into the group's Lean course and widely deployed to R&D teams on its various sites in France and abroad (India, Italy, etc.)",* explained Thierry Fensch (STMicroelectronics).

RNDYNEO has been adapted into English and provided to international students from Grenoble INP (on international master's programs of Nanotech and Emine), as well as to Indian professors from Amrita Vishwa Vidyapeethal University. It is part of a partnership project aimed at enhancing the attractiveness of Grenoble INP as well as mobility and collaboration with universities in the Indian subcontinent. The latter project is supported by Idex UGA. •



Teachers at the Amrita University in India trying out the serious game RNDYNEO.
© Eric Blanco-Grenoble INP



Students of the Nanotech master's degree course trying out the international adaptation of the serious game RNDYNEO.
© DR



Serious gaming for new products and services

A way to find two thirds of possible innovations in a category of products or services using an entertaining process: this is what two teachers from Grenoble Ecole de Management (GEM) offer with Creanov.

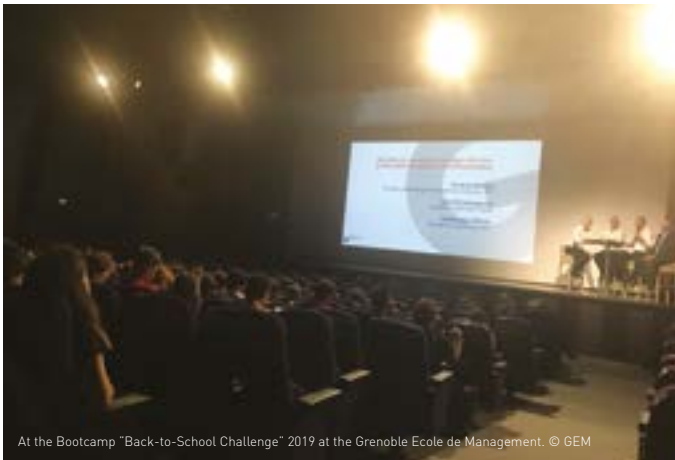
Aimed at innovation and creativity faculties as well as business innovation teams, the game was developed in 2018 with the support of Nanoelec/Training program to implement a scientifically proven method. In order to support the creative process, Créanov uses the fun-

damental framework method. This involves breaking down an existing product or service into two kinds of features (its components and attributes) and then exploring the different possibilities of reconfiguration, creating new links between its features and imagining innovations. •



Bootcamp to think about technological societies

Grenoble Ecole de Management (GEM) organized the "Back-to-School Challenge 2019" with the support of the Nanoelec training program in order to welcome the 700 students from its Grande Ecole program.



At the Bootcamp "Back-to-School Challenge" 2019 at the Grenoble Ecole de Management. © GEM

"Our students worked for 10 days on smart solutions, including their pros and cons, in a course called 'Business Lab for Society'", explained Ivan Laurens, a GEM teacher and co-organizer with Lionel Strub of the Back-to-School Challenge. "To stimulate the students from the start, we simulated a 'Black Mirror' scenario in which each person's journey was determined by their digital footprint, from

their recruitment interviews to the creativity workshops developed specifically for the module". All these elements have supposedly made it possible to determine their cognitive profile as a learner and their associated learning course: leader entrepreneur with an active learning style or introverted analyst with the opposite learning style.

"There is nothing like being personally affected in order to fully appreciate the ethical issues of technology", continued Ivan Laurens, adding that the scenario could also have included a predictive recruitment example by AI in a company or even a tracking application example in the context of a major health crisis.



The students worked on concrete start-up case studies that would use these technologies. They analyzed them based on theoretical and methodological lessons and meetings with professionals from the perspective of sustainable development. They then worked on 18 controversial scenarios relating to major issues in technology management and presented their opinions to an audience of business leaders, managers and teachers. •

International Mistre master's program



The Master's in Integration, Security and Trust in Embedded Systems (MISTRE) opened its doors in 2018.

Nanoelec supported the roll-out of this new course, which is entirely taught in English. Thirteen international students took the master's program in 2018, following a selection of 137 international applications, and 15 students took the program in 2019. The master's program was also awarded the 'Digital Campus' label from the Auvergne

Rhône Alpes region, and it is also co-accredited by Grenoble INP and UGA. It reinforces the initial training offered on the topics of security and trust in embedded systems.

"In a world where smart systems are everywhere (IoT, connected objects, autonomous vehicles, aeronautics, smart housing, etc.), safety and security issues (digital trust) have become major issues", explained Vincent Beroulle, head of the master's degree course. •



Key publications

TEACHING MATERIAL FOR HARDWARE/SOFTWARE CO-DESIGN

Low-consumption embedded systems for real-time image and video processing require incorporating complex algorithms on silicon. Learn-V is a new teaching material that focuses on joint hardware-software development. *“Co-design is one of the most difficult points in microelectronics education for engineering students”*, explained Mounir Benabdenbi (Grenoble Alps University), one of the authors of the project.

“With Learn-V we are renewing existing platforms in the field that were obsolete”.

Learn-V uses the free software platform Rocket Chip (University of California), which is based on the free processor RISC-V (used in industry) in order to teach and practice architecture concepts that integrate hardware and software parameters at the design stage.

Developed by the Tima laboratory teams (Grenoble INP/UGA/CNRS) as part of Nanoelec, it was presented at the RISC-V workshop (Switzerland, June 2019) as well as at the 13th GDR SOC2 National Symposium (Montpellier, France June 19-21, 2019). The results of this research have been directly adapted within the modules intended for Grenoble INP Phelma courses.

→ **N. AIT SAID, M. BENABDENBI**
Teaching Hardware/Software Co-design using Rocket Chip’, Risc-V workshop
Zurich, Switzerland, June 11-12, 2019

TEACHING THE CHARACTERISATION AND IMPLEMENTATION OF HIGH-SPEED POWER DEVICES FOR THE ENGINEERS OF TOMORROW

Power electronics engineers are among the most wanted professionals. However, the field is not well promoted towards the students.

Furthermore, the switching speed of power semiconductor devices-especially wide bandgap devices-is continually increasing, and the knowledge and understanding of switching mechanisms is necessary for designing power converters.

Teams from Grenoble INP (UGA) and G2ELab shared and analyzed the content of a power electronics class at the Master’s Level 2 level, which was adapted in line with the most recent advances in the technology. Five different topics were studied: device characterisation (bare dies), switching waveforms, loss characterisation, thermal design, electromagnetic compatibility and magnetics design.

The study, conducted as part of Nanoelec, was presented at the ECCE conference (USA, Sept. 2019). It led to the implementation of a specific module in English titled ‘Power Electronic Semiconductor Devices-Physical basis, implementation and characterisation’, which was incorporated in the international master’s program ‘Smart Grids and Building’ and the training course ‘Electric Energy Engineering’ (IEE- Grenoble INP - ENSE3).

→ **J-L. SCHANEN & AL.**
Teaching how to characterize and implement high-speed power devices for the engineers of tomorrow
ECCE conference, Baltimore, USA, 09/29/2019-10/03/2019



DESIGNING EXPERIENTIAL TRAINING IN LEAN PRODUCT DEVELOPMENT: AN INDUSTRY AND ACADEMIA COLLABORATION

The design of a training program in lean development was inspired from design thinking principles (related to the serious game, RNDYNEO). Experiential learning through serious games and case studies is the educational foundation of the teaching material. The approach was developed by an interdisciplinary team of researchers from STMicroelectronics, Grenoble Alpes University, Grenoble Ecole de Management and Grenoble

INP, and under Nanoelec.

The paper discusses the design process of the program that led to an innovative co-creation and demonstrates the benefits of interdisciplinary teamwork and relevance of a user-centered approach for lifelong learning training design.

It was presented at the International Conference on Engineering and Product Design Education (UK, September 2019).

→ **E. BLANCO & AL.**
**Designing Experimental Training in Lean Product Development:
A Collaboration between Industry and Academia**
Zurich, Switzerland,
June 11-12, 2019



Educational team of the RNDYNEO project. © Grenoble-INP

Large-scale instruments characterisation



JÉRÔME BEAUCOUR

Director of the Nanoelec Large Scale Instruments Characterisation Program

Look & outlook

Radiations from space are known for many years to impact the behavior and reliability of spacecraft electronics. More recently, the dissemination of sophisticated electronic devices have lead aeronautic and computer data storage industries to take into account the effects of ionizing radiation on systems reliability. Indeed, IC's may be sensitive to the space background radiation even at the ground level. It turns out that automotive industry is also now becoming aware of this new constraint.

Vehicles use more and more electronic parts while complexity of their digital architecture increase dramatically. That goes hand in hand with the increasing reliability constraints.

The ongoing development toward autonomous vehicle strengthen such a trend. Businesses in computer centers, internet of things (IoT) and medical equipment and implants are following the same trend. More

generally, industrial sectors combining advanced electronics, production volumes and reliability requirements will have to consider the radiation sensitivity of components in their new designs.

On the other hand, the increasing complexity of electronic components and technologies, as well as the diversification of materials and manufacturing processes in the More-than-Moore approach requires characterisation that exceeds the performance of standard laboratory equipment. The need to correlate accurately micro- and nano-metric characteristics of materials to macroscopic properties of components translates into a need for gains in spatial resolution, detection capacity and acquisition speed.

To provide an efficient answer to these raising challenges, the Nanoelec characterisation program set unprecedented initiatives linking micro/nanoelectronics R&D with the large scale research infrastructures of the Grenoble ecosystem which are among the best in the world (European neutron source ILL, European synchrotron source ESRF, CNRS-LPSC laboratory).

With unmatched performance in micro/nanoelectronic characterisations, the services developed by the program are now available to industry thanks to the Platform for Advanced Characterisation – Grenoble (PAC-G). To face radiation background challenges for systems safety, the program is initiating a center of excellence in radiation testing which will target a large panel of high-tech industrial sectors.



An international event dedicated to materials characterisation for industry

CARAC is an annual international event dedicated to materials characterisation for industry supported by Nanoelec and the European projects CalipsoPlus, NFFA and SINE2020.

CARAC 2019 (November 2019, Grenoble, France) was the first of its kind offering presentations on industrial cases, tutorials on advanced characterisation techniques and technical visits of characterisation platforms in Grenoble.

It gathered 60 attendees from the European research scene for two days. Participants had also the chance to take a private tour of the leading research facilities of the European Neutrons & Photons Science campus (ESRF & ILL), the UGA-CNRS facilities (Genesis platform at the Laboratory of Subatomic Physics & Cosmology - LPSC and Néel Institute) and the Grenoble-INP Technological Platform for Material Characterisation (CMTC). •



A World-class tomography station

Supported by Nanoelec/Characterisation program and Grenoble-Alps-University (UGA), with the collaboration of the Helmholtz-Zentrum Berlin Laboratory, D50 has been upgraded in 2019. It is now the world most advanced neutron imaging station.

It is equipped with an innovative reflectometry setup, a cutting-edge neutron and X ray tomography station and an irradiation set up, which work alternatively on the beam. D50 delivers a cold neutron flux of 9×10^7 n/s/cm² at its n-tomography station and is capable of achieving impressive 4 μ m of real resolution, the highest in the world.

Private companies and academics have been extensively using the D50 tomography station at the ILL for R&D in hydrogen fuel cells and Li-ion batteries, taking advantage of the unique capability of neutrons to reveal lithium and hydrogen based compounds. •



Nanoelec/ESRF beamline visit by the EC General Manager for Research and Innovation

Jean-Eric Paquet, General Manager for Research and Innovation at the European Commission visited the European Photons and Neutrons Campus on January 2019.

At the ESRF, M. Paquet met the team managing the Nanoelec/Characterisation program. He discovered the beamline BM05, which was partially funded by Nanoelec. The experimental setup includes in a five-circle goniometer, a robot that automatically positions 300 mm and 200 mm wafers for electronics on the diffractometer, a mirror to focus the beam to less than 30 microns, an optical microscope to locate the areas of interest (several micron squares). The large size of one of its detectors (25 cm x 2.5 cm) allows very quick mapping of the

reciprocal space in diffraction patterns. It also allows X-ray reflectometry to characterize the morphological properties (roughness and dimension) of very thin layers (up to 1-2 atomic layers) and topographic analysis to qualify and quantify crystallographic defects of high quality crystallized materials such as diamond or Si wafers. Access to this unique instrument is included in the PAC-G offering for industrial stakeholders. •



Experimental setup inside the irradiation hutch of the beamline BM05 at the ESRF.
© ESRF/P.Jayet



Jean-Eric Paquet, General Manager for Research and Innovation at the European Commission (center) at the ESRF with Francesco Sette, ESRF's director (left) and Helmut Schoeber, ILL's director (right). © ESRF

Ten times more neutrons with Genesis

After an upgrade phase of one year, the Genesis facility (Generator of neutrons for science and irradiations) came back into operation in November 2019 with a flux up to 7.10^9 n/cm²/s 14 MeV neutron.

As a large scale instrument on the cutting-edge at the European level, it is hosted by the Laboratory of Subatomic Physics

& Cosmology (CNRS/UGA). It includes an accelerator-based neutron source which can provide an intense flux of 2.5 MeV or 14 MeV neutrons. This unique accelerator is equipped with an original compact ECR ion source capable of delivering a continuous deuteron beam at 220 keV. The Genesis facility is mainly used for single-event effects testing in microelectronics, diamond or Si wafers.

Access to this unique instrument is included in the PAC-G offering for industrial stakeholders. •



Inside the Genesis platform (Generator of neutrons for science and irradiations).
© S.Maurin 2017CNRS

Serma Technologies joins the PAC-G platform

Serma Technologies contributing to development of the PAC-G offering.
© ILL/S.Claissé

The Nanoelec/Characterisation program and Serma Technologies, a leader in the characterisation market, signed a mutually beneficial partnership agreement in September 2018.



Serma Technologies offers consultancy, expertise, analysis, inspection and testing services for components, circuit boards and full electronic systems. "We accompany our customers throughout the industrial cycle by advising them on the development, durability and reliability of their products," said Pascal Matosevic, Sales and Marketing Director at Serma Technologies.

"With their multisector expertise and our teams of engineers and technicians, it becomes possible to address a wide range of customer issues using state-of-the-art equipment. Thus, it is a natural progression for us to combine our forces to the Nanoelec/Characterisation program for the development of the PAC-G services."

In 2019, this service offering and collaboration with Serma was ramped up with participation in meetings with the Serma sales department, promotion of the PAC-G service offering, and joint participation in trade fairs and events. •

The ESRF Extremely Brilliant Source (EBS) project



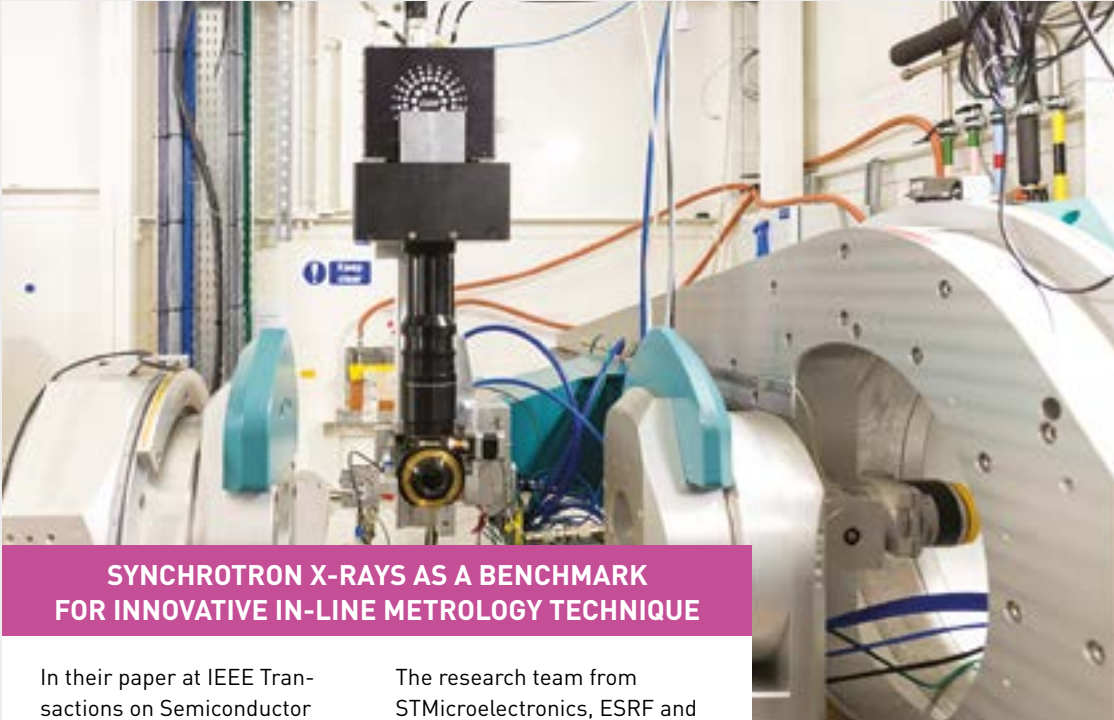
ESRF-EBS (Extremely Brilliant Source) is the ESRF's €150M facility upgrade, over 2015-2022, bringing its scientific users a first-of-a-kind, low-emittance, high-energy synchrotron light source and new, cutting-edge beamlines.

With a revolutionary new storage ring concept that increases the brilliance and coherence of the X-ray beams produced by a factor of 100 compared to present-day light sources, ESRF-EBS represents a new generation of synchrotron and an extraordinary new tool for scientists and industry to study the heart of matter.

With its extremely brilliant X-rays, incredible resolution and range in space and time, ESRF-EBS offers to the electronics industry through Nanoelec's characterisation services, unprecedented tools for the understanding of materials for electronic devices at the nanometre scale. •



Key publications



SYNCHROTRON X-RAYS AS A BENCHMARK FOR INNOVATIVE IN-LINE METROLOGY TECHNIQUE

In their paper at IEEE Transactions on Semiconductor Manufacturing, Romain Duru & al. described the innovative photoluminescence imaging technique for applications to buried defect detection in silicon devices. The validity of this emerging technique is first assessed in comparison with well-established characterisation techniques (defect selective etching of silicon, synchrotron X-Ray diffraction topography, cross-sectional transmission electron microscopy imaging and photoluminescence spectroscopy).

The research team from STMicroelectronics, ESRF and Université de Lyon describes specific applications illustrating the use of the photoluminescence imaging technique for common processes of the CMOS semiconductor industry. They demonstrated benefit of this fast, high resolution and non-destructive technique: this includes industrial use of the technique for production control on product wafers. The beamtime on BM05 and support on the beamline at ESRF for this study were provided under Nanoelec.

Experimental setup inside the irradiation hutch of the beamline BM05 at the ESRF.
© ESRF/P.Jayet

→ **R. DURU ET AL.**
Photoluminescence Imaging for Buried Defects Detection in Silicon: Assessment and Use-Cases

In IEEE Transactions on Semiconductor Manufacturing
Vol. 32, no. 1, pp. 23
30, Feb. 2019

DOI: 10.1109/TSM.2018.2871967

A COMPARISON OF VARIOUS RADIATION TESTING METHODS ON A PHOTODIODE

At the 2019 Radecs conference, a French and German team (Cnes, ESRF, GSI and TRAD Tests & Radiations French ETI) presented a contribution to the use of alternative single-event effects (SEE) test methods. *"We first report collected charge measurements and simulations in a P-i-N photodiode",* the authors said. *"The main purpose was to evaluate*

parameters leading to the correlation between heavy ion broadbeam and microbeam, pulsed synchrotron X-rays and laser pulses".

This study also relies on coupled and analytical simulation to further understand the physical phenomena involved. Single-event latch-up (SEL) current shapes acquired on a ASIC circuit built on CMOS technology

were also analysed and confirm the correlation of these test methods at the temporal scale. These results were then used to study single-event upset (SEU) bursts in an SRAM memory with pulsed X-rays and heavy ions. Scientific assistance prior, during and after the experiment were provided by the ESRF and PAC-G teams under Nanoelec.

→ G. AUGUSTIN ET AL.

Cross-Calibration of Various SEE Test Methods Including Pulsed X-rays and Application to SEL and SEU

2019, September

In Radiation Effects of Components and Systems - RADECS. Montpellier, France.

(Article to be published in IEEE Transactions on NuclearScience in 2020)

NEUTRONS HELP ADVANCE RESEARCH TOWARDS A SENSOR TO DETECT TRANSIENT FAULTS

A study presented at Radecs 2019 conference assesses for the first time a bulk built-in current sensor (BBICS) in a CMOS 65-nm test chip under thermal neutrons, fast-energy neutrons, and laser radiation.

Experimental results suggest that the on-chip current sensor is effective to detect transient faults in different case-study sub-circuits of the chip exposed to accelerated radiation effects, opening prospects for

embedding this type of sensor in reliable, secure, and low-power integrated circuit applications. The beamtime on D50 and support on the beamline at ILL for this study were provided under Nanoelec.

→ R. POSSAMAI BASTOS ET AL.

Assessment of On-Chip Current Sensor for Detection of Thermal-Neutron Induced Transients

2019, September

In Radiation Effects of Components and Systems - RADECS. Montpellier, France.

(Article to be published in IEEE Transactions on Nuclear Science in 2020)



The ILL, international institute for neutron beams, is one of the facilities use in Nanoelec/Caracterisation program. © ILL

Easytech

La Région 
Auvergne-Rhône-Alpes



DAMIEN COHEN

Director of the Nanoelec Easytech program

Look & outlook

Easytech focuses above all on the needs expressed by SMEs and facilitates access for companies to breakthrough innovations generated through Nanoelec technology programs. These companies are the main targets of the program, which was set up to boost their competitiveness within a medium term time frame. SMEs in all sectors can thus access advanced technological building blocks in the field of micro and nano electronics and thereby diversify, improve or enhance their existing products with new functions or new services.

Given the COVID-19 crisis context, we have had to quickly reconsider our working practices and social organizations. The crisis has given rise to new needs and goals; it has also highlighted a number of gaps and significant challenges for our societies in terms of resilience and independence.

Digital technologies can provide solutions in many structural areas including health, working arrangements, social relationships, security and short business cycles. Today, more than ever, the Easytech program is relevant in supporting companies to develop new services and unique products using the expertise of Nanoelec partners.

The program was launched by Nanoelec at the regional level in the French region of Auvergne Rhône-Alpes with the support of Minalogic, which is a global innovation cluster for digital technologies, and with regional facilities also supporting innovation. In recent years, it has gradually spread to cover the whole France territory.

There were 24 projects involving Nanoelec signed in 2019, out of a total of 257 projects since 2012. The projects last between 6 and 18 months, depending on the technological level and the maturity of the technology transferred.

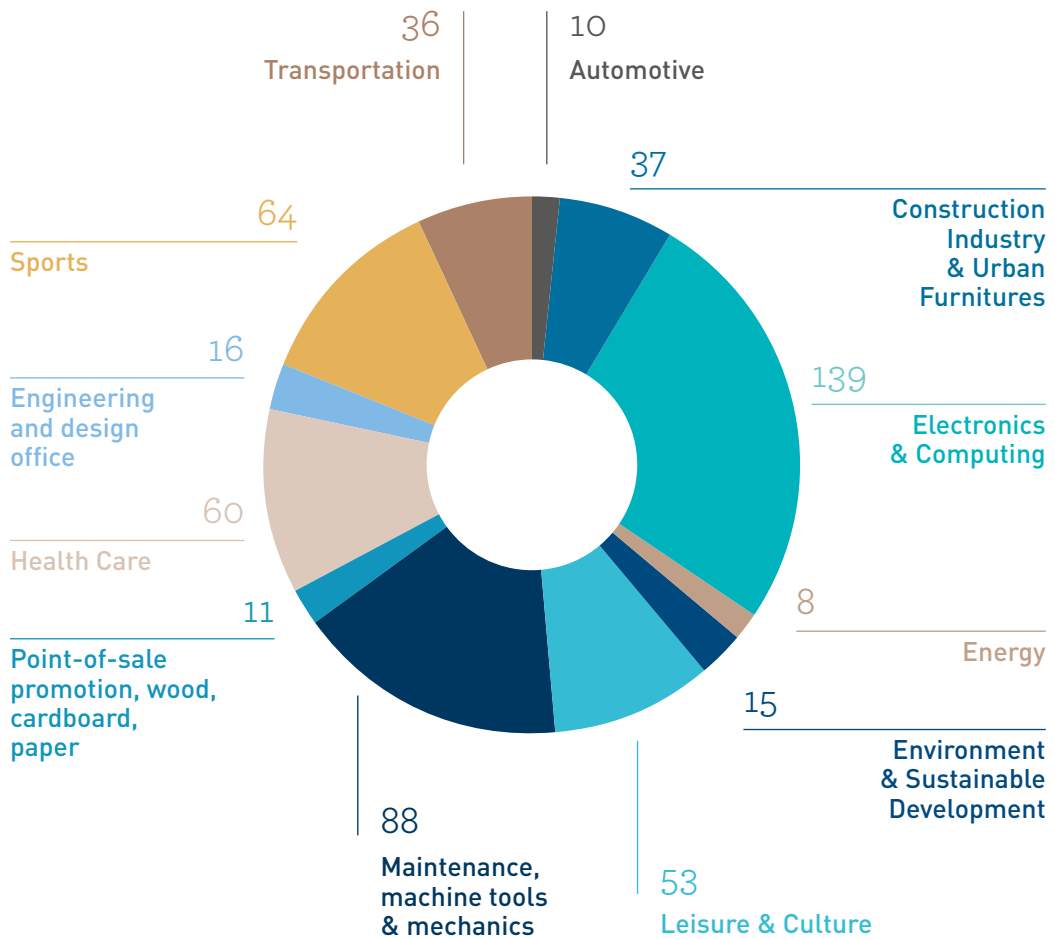
The new products, functions and services are being developed in the hubs and laboratories of two major partners of Nanoelec: CEA and Grenoble INP, and in collaboration with the Jessica association, mainly involved in securing projects before developing product demonstrators. It is a three-phase process offered to companies:

- > The “Explore” service: creativity, consulting and guidance towards the relevant partner.
- > The “Specify/Secure” service: meeting with marketing and technology experts, finalizing the functional specifications, and risk analysis.
- > The “Materialize” service, provision of a product demonstrator.

In a context of economic recovery after the health crisis of 2020, an innovation accelerator like Easytech may prove essential in spreading solutions quicker and more effectively in order to boost the competitiveness and sovereignty of French companies.



Fields of the projects supported by Easytech





Lithium batteries for aeronautics

Limotech is a startup established in 2016 and collocated in Toulouse and Grenoble.

The company is developing the next generation of lithium batteries for the aerospace and defense sectors. The technology will save up to 1 million tons of CO₂ over the next eight years. Limotech batteries replace the current technology that uses nickel cadmium and lead, which are highly toxic substances in very heavy devices. Limotech batteries are three times lighter. Their lifespan is also 2.5 times longer.

Limotech's technological prowess derives primarily from its BMS (Battery Management System), an on-board electronic management system that safeguards the lithium use in harsh environments. The BMS system was developed with the support of CEA and through Nanoelec/Easytech. "At the end of the Easytech project, we had two functional battery packs", explained Florence Robin, co-founder and president of Limotech.

"The electronic management ensures that the internal combustion engines of planes are started

safely without damaging the on-board avionics in the event of a power outage."

Based on an ambitious certification strategy, Limotech will be able to target the OEM and retrofit markets from 2022. The first market segments targeted are general aviation, business and military segments, including aircraft such as the EC 120 from Airbus Helicopters or the Dassault Falcon.

"Thanks to the Nanoelec/Easytech demonstrator, we expect a turnover of €130 million by 2028. Enti-

rely based in France, the company now employs ten people and plans further recruitment to reach a capacity of 30,000 lithium batteries per year by 2028," said Maxime Di Meglio, managing director of Limotech, who aims to ultimately be able to target "48% of the aeronautical market for lithium batteries".

Limotech is currently completing a final stage of a fundraising of around €2 million via BPI, Business Angel and a crowdfunding campaign on the Finple platform. •



Photo showing the pre-series of 12 V batteries, called Sierra. © Limotech

Cybersecurity for reliable timing

Gorgy Timing launches its innovative NTP STS protocol (Secure Time Synchronization), with the assistance from the Nanoelec/Easytech program and the coordination by Minalogic, a partner of the Auvergne-Rhône-Alpes Region for innovation and digital transformation projects.

Gorgy Timing leveraged CEA's cybersecurity expertise available through Nanoelec in analyzing the first secure time protocol on the market, in order to find out whether there were any vulnerabilities, and by conducting a formal verification and analyzing the robustness of its implementation. •



A personal health app

"The WHO estimates that 13 million people die each year due to pollutants in their immediate environment", explained Morane Rey-Huet, president of Meersens, a startup founded in 2017 and that benefited from the support of Nanoelec/Easytech in 2018 to build a pre-production prototype.

Meersens is a DeepTech artificial intelligence company specializing in the aggregation and processing of exposure data in order to help and support health professionals,



The Meersens mBox is a connected device, that will soon become available; it adapts to everyday life and helps people make the best choices for their health and that of their loved ones. © Meersens

businesses, cities and citizens to take into account the impact of the environment on people's medical condition. Through its SaaS solution, mobile application and IoT, Meersens assists public health and is part of a virtuous process for setting up advice, preventative actions and

decision support, with close collaboration with specialists in relevant fields. *"The Easytech project, along with Grenoble-INP, helped us to optimize the electronic card and the connectivity of the biosensors of the mBox, which will be commercialized in 2020",* said Morane Rey-Huet. •



Sport Unlimitech

Discussing the sports of tomorrow is all well and good, but experiencing and trying them out is even better.

The back-to-school season last year has been sportier thanks to Sport Unlimitech, the first trade fair dedicated to sport and innovation.

Taking place in Lyon at the Matmut stadium (2019, September 19-21), the trade fair offered lectures, exhibitions, demonstrations and sports. An initiative of the former rugby player Frédéric Michalak, Sport Unlimitech gave the opportunity, at first hand, to experience the latest innovations that will revolutionize the world of sport.



The Nanoelec/Easytech program, supported by the Auvergne-Rhône-Alpes region, was present with three companies, one of which had benefited from a Cap'Tronics expertise, and two partners from the Grenoble INP and Minalogic program.

These three companies were:

- > Microoled: development and marketing of miniature OLED display for near vision in glasses and other viewing systems.
- > Ido data: use of the Internet of Things and digital technologies to build innovative alarm solutions together with expert partners in their fields, and which aims to prevent risks and enhance security.
- > Up Trainer: a soccer ball launcher that makes the latest technological advances available to coaches and players. •



Internet of Things Trade Fair

Nanoelec, through its Easytech program, was once again present at the Internet of Things trade fair (Sido) in Lyon in April 2019.

For its 5th event, Sido helped break down the barriers between technological worlds by combining IoT, AI & Robotics. From building blocks to solutions, Sido continues to drive innovation by unifying three convergent ecosystems for connected, autonomous and ever smarter projects.

"It was an opportunity to meet the startups and SMEs that will be the stars of tomorrow to offer them our services", says Damien Cohen, Program Director of Easytech.

Located in the Minalogic village, with 16 co-exhibitors, Easytech has once again demonstrated its added value, appeal and strength for companies wishing to innovate.

The Sido trade fair welcomed more than 9,000 visitors. •





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MEMBER

