NANOELEC.

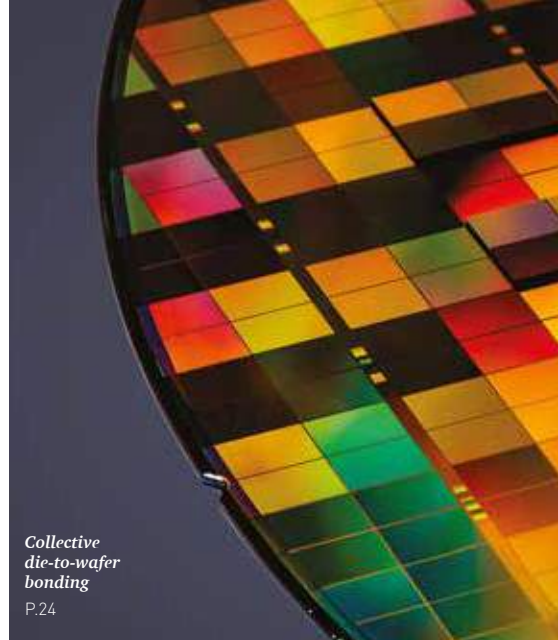# Scientific & technical highlights

Nanoelec/PAC-G, a gateway to large instruments for characterisation
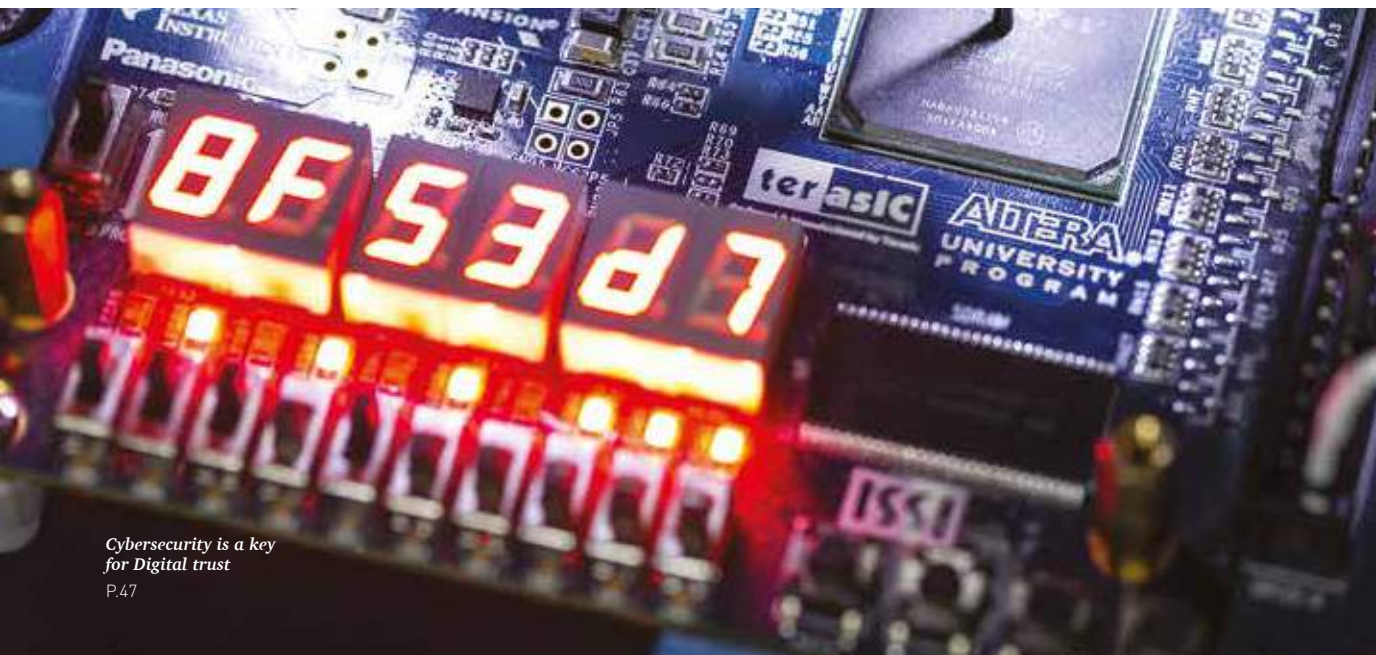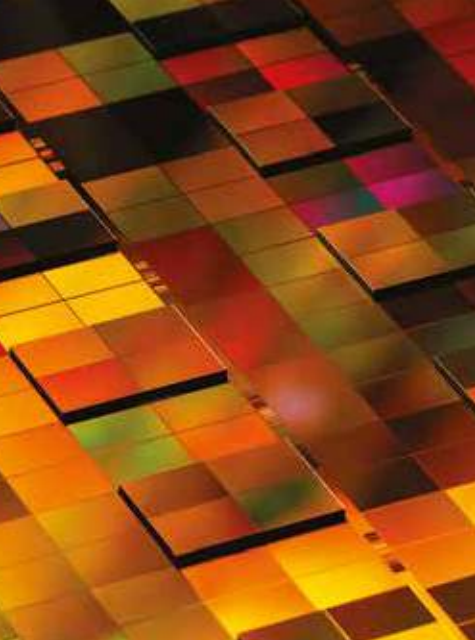P.74

Collective die-to-wafer bonding
P.24

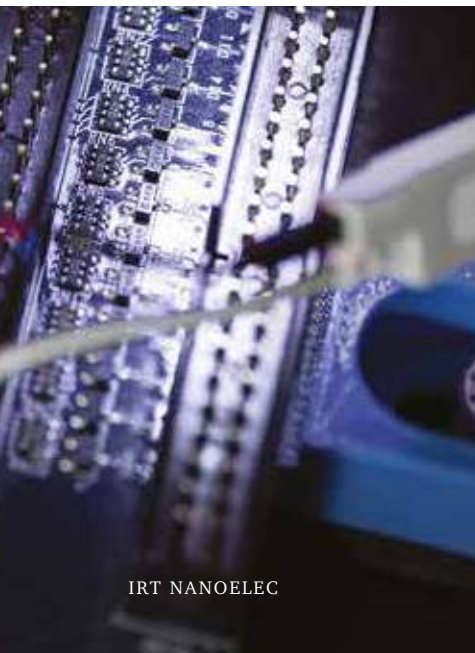*A wireless reliable industrial system*
P.55

Towards display technology leadership in Europe
P.20

Cybersecurity is a key for Digital trust
P.47

Technology dissemination
P.87

Exploring the future of electronics

IRT Nanoelec runs multi-partner technology development and dissemination programs to make the electronics sector more competitive.

> **"Working together to carry out responsible research and development programs to help businesses create value."**

The Nanoelec technological research institute is a consortium of private and public sector players. Our mission is to help companies create value and enable their products to stand out on the digital transition stage.

Nanoelec contributes to the competitiveness of the electronics sector, especially in France. It is based in Grenoble, a world-class hub for research, innovation and production in the field.

Our R&D programs are built jointly by representatives from the academic and industrial worlds. They deal with the design and development of new processes, systems and components in the following fields:
→ photonic sensors, new-generation displays and smart image sensors,
→ technologies for connected objects,
→ energy conversion,
→ characterisation and resistance to radiation of components and systems by means of large instruments.

Nanoelec also runs training design and technological dissemination programs for SMEs. With the support of the Auvergne Rhone-Alpes region, we implement open innovation methods as well as more conventional technological development methods for technology dissemination.

Given the pervasive nature of digital technologies, Nanoelec is in contact with actors from all sectors ranging from goods to services, industry and infrastructures to consumer products, not forgetting transportation, environment and health.

Nanoelec is one of the technological research institutes (IRT) and energy transition institutes (ITE) set up by the French Government and financed by the Investments for the Future program (PIA). These institutes pool academic and industrial players on R&D and their innovation projects aimed at boosting competitiveness of the french economy.

ANTICIPATING FUTURE SKILLS AND TECHNOLOGICAL NEEDS

Microelectronics innovation

→ Carry out world-class collaborative R&D on common roadmaps gathering industrials ans academics

→ Develop and transfer these technologies to create the electronic circuits of the future

→ Give industry players access to development, prototyping and advanced characterization resources

Technology dissemination

→ Help businesses in the field of information and communication technologies meet the challenges of IoT and digital trust and security

→ Provide expertise to help SMEs from various industrial sectors build new products and services with innovative components and embedded software

→ Promote cooperation between SMEs, mid-caps and large companies

→ Collaborative innovation to unveil new applications

Development of human capital

→ Attract young people into jobs in electronics through inclusion, responsability, equality, sustanability

→ Map out needs and assess employment opportunities

→ Design training courses to meet current needs

→ Anticipate future skills required in the sector: sustainability, cross-skills, social and technical communities for innovation

Key figures of the institute

DECEMBER 2020

A consortium of
**public
& private**
members

[21 partners
as of December 2020]

€54M
average
annual
budget

258
associated
partners
including
198 SMEs
since 2012

472
scientific or
technical
publications &
communications
since 2015

199 patents and
43 software filed
since 2012

219
Full Time jobs -
31% in from private companies
in 2020

EASYTECH 3
3D INTEGRATION 5
PHOTONICS 3
POWERGAN 10
PULSE 12
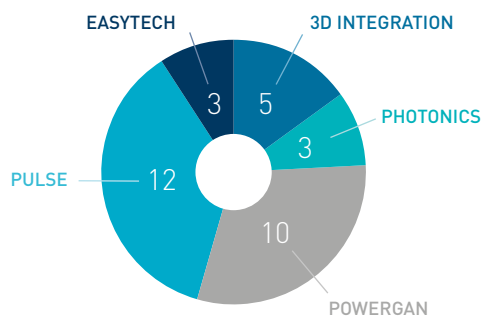
PATENTS & SOFTWARE
FILED 2020

HUMAN CAPITAL & TRAINING DESIGN 13
EASYTECH 10
GESTION 5
3D INTEGRATION 67
PHOTONICS 21
POWERGAN 42
CHARACTERISATION 7
PULSE 54
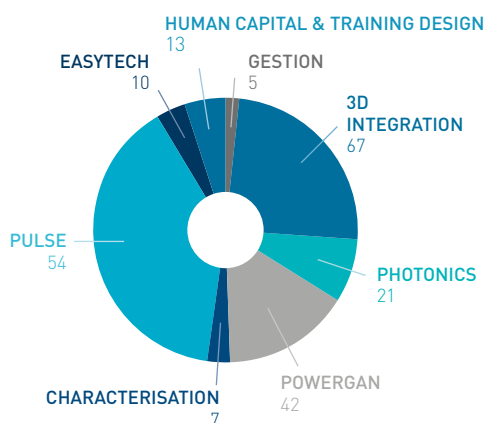
HUMAN RESOURCES
(IN EQUIVALENT FULL-TIME)

Nanoelec benefits from 10 000 m² of world class level clean rooms at CEA-Leti

© Aubert/CEA

A renewed trust from our stakeholders

by Hughes Metras,
Director of the Technological
Research Institute IRT Nanoelec

Equipment EVGroup Gemini.
EVG is a core partner of Nanoelec
© Aubert/CEA

" The Electronics industry is experiencing a period of tension in terms of component availability, the shortage of which is affecting all products: mobile phones, PCs, digital infrastructures, automobiles, etc. As a result, in 2020, the French and European players in the semiconductor sector became acutely aware of the issues of sovereignty and relocation: Owing to their large-scale dissemination, digital systems are at the heart of our economy. This pervasiveness also makes the entire digital sector a prime target for cybersecurity threats: not a week goes by without increasingly sophisticated attacks impacting our public and private economic players.

Following on from the mission entrusted to us by the French Public Authorities in 2012, Nanoelec is addressing some of these challenges, with the aim of successfully completing collectively defined R&D programs. This open collaborative framework is the very DNA of all the IRTs and ITEs under the FIT (French Institutes of Technology) umbrella.

Nanoelec renewed its convention with ANR, the french national research agency. Thanks to this reaffirmed trust and the results obtained over the last nine years in core technologies such as chip stacking, silicon photonics and component security, we set out a range of roadmaps for the period 2021-2025, to target key applications fields for the industrial partners in our consortium.

One of our ambitions is to support our local ecosystem, specialized in the field of imagers, in the move towards smarter sensors and help them identify or anticipate new applications for their components.

Our project in the field of microled displays is a good illustration of how technological innovation can help our industry bring back manufacturing activities that have been abandoned by Europe for a long time. The Smart Pixel concept, which underpins the ambitions of this project in the field of high-end displays, bears witness to the inventiveness of our partners.

Finally, we decided to set digital trust as the core of our developments, in order to address security issues of the IoT, home health care and industrial sectors.

"The IRT renewed its convention with French public authorities."

"The Electronics sector provides the essential industrial base for the design and production of increasingly smart and connected objects in the world around us. The sector thus lies at the heart of the national industrial dynamics and is a powerful force for the development of sectors through innovation and competitiveness."

The diversity of our consortium which, around the Minalogic hub and CEA, gathers local academic teams, key industrial players in the ecosystem including large Groups, midcaps, SMEs and startup, enables us to look to the future with confidence and ambition, while continuing with our technological development, training engineering and dissemination missions.

This latter includes building R&D and scientific services offerings around the advanced physical characterisation skills of our partners operating the Large Instruments in Grenoble, around our silicon technology platforms and our innovative systems integration and testing resources.

Resilience and sustainable development are the facets of the lens through which society (including the end-users of the digital systems) analyzes and questions itself. The younger generations are challenging us on these issues. Evidence of this is the strong commitment of the GEM and Grenoble-INP students who took part in our workshop to design a green phone last February.

In 2021, we are picking up the challenge: we will implement lifecycle analysis tragetting projects at the R&D phase, evaluate environmental diagnosis tools for the Easytech projects and pursue our actions on professional equality in the electronics sector. ■

HUGHES METRAS,
Director of Nanoelec
© P.Jayet/CEA

Highlights

January 2020

Learning communities

→ First **"Sustainable Electronics"** module rolled out with experts from STMicroelectronics, CEA and UGA to 40 master's students.

January 2020

3D Architecture

→ In January 2020, Perceval Coudrain receives a **"Best Paper Award"** for his paper entitled 'Active Interposer Technology for Chiplet-Based Advanced 3D System Architectures' presented at ECTC conference 2019.
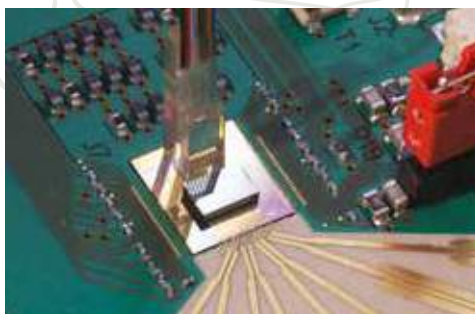
January 2020

Industrial cybersecurity

→ Nanoelec teams present Industrial **IoT Security** developments at the International Cybersecurity Forum (January 2020, France).
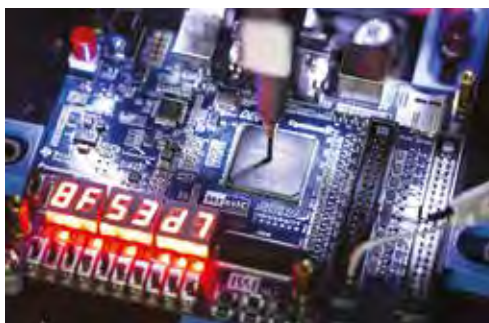
© Moret/CEA

February 2020

Optoelectronics

→ CEA-Leti **silicon photonics platform** developed within Nanoelec is presented at Photonics West international conference.

© ErikaWittlieb / Pixabay

February 2020

Senior Care

→ Launch of **Cocoon Care**. The startup is marketing a solution to detect falls, based on a new generation of detectors and an events management and tracking platform.

March 2020

Power Electronics

→ STMicroelectronics acquires majority stake in **Gallium Nitride innovator** Exagan. It's a new context for Nanoelec/Powergan program.

© P.Jayet/CEA

March 2020

Characterisation

→ 25 PhD students discover characterisation techniques based on neutronic and X-ray synchrotron radiation. The **training module** was adapted to digital format.

March 2020

Batteries

→ Limatech, a startup that has benefited from the support of Nanoelec/EasyTech, raises €2 millions for the development of its **lithium battery systems** for aeronautics.

March 2020

Nanoelec goes online

→ ¨Bridging the gap between semiconductor technologies and architecture design¨ is the title for the very first online webinar at Nanoelec. It is organized for the Date 2020 international conference.
3D Integration, Powergan and Photonics at a glance are covered: **11 key players from our community** -including. CEA, Siemens EDA, STMicroelectronics, Schneider Electric, Prophesee and Polytechnic University of Valencia (Spain)- gave talks during the event.

© CEA

March 2020

Global Shutter Imagers

→ STMicroelectronics is starting to ship high-performance global shutter image sensors. Their unique back-side illuminated global-shutter pixel uses ST **die-stacking technology** that benefits from results of the Nanoelec 3D program.

© P.Jayet/CEA

Highlights

© PJayet/CEA

April 2020

Digital Twin

→ Siemens EDA joins the PowerGan Program to work on **digital twins** for energy converters.

Gerd Altmann/Pixabay

April 2020

Smart cities

→ Kentyou is created. The startup provides open digital solutions, to collect and analyze **urban data** and enable local innovators to build custom solutions that respond to citizens' needs.

May 2020

Infra-red imagers

→ Lynred joins the Nanoelec consortium in May 2020 to accelerate **new imager** developments.

LYNRED
BY SOFRADIR & ULIS

April 2020

Energy Storage

→ Lancey Energy Storage, a startup that has received Nanoelec/EasyTech support, ranks second in the **"Sustainable Society Startup Challenge"** of the MIT Global Startup Workshop 2020.

© Lancey

May 2020

Safety of industrial systems

→ CEA-Leti and Davey Bickford Enaex, collaborating in the frame of Nanoelec, unveil the demonstrator of a new **wireless system** that offers increased safety, flexibility and productivity gains to the blasting market.

August 2020

SMEs go digital

→ 1.1 million€ to support companies in their **digital transition** through the Digifed EU program coordinated by CEA through Nanoelec.

June 2020

Government support

→ Frédérique Vidal, French Minister of Higher Education, Research and Innovation announces **€ 450 million over 5 years** for technological research and energy transition institutes (IRT & ITE), including Nanoelec.

©S.Riondet/CEA

June 2020

Business Meetings for SMEs

→ The Nanoelec/Easytech program take part in online Minalogic **Business Meetings**.

September 2020

General Assembly of the institute

→ Online sharing of achievements and insights on **technological and social issues** such as resilience, sustainable development, gender parity and open innovation.

© Davey-Bickford

July 2020

Webinar on photonics on Si

50 international attendees for Nanoelec speakers (CEA-Leti and CNRS-LTM) share online their latest results & achievements in **integrated photonics** technology.

© P.Jayet/CEA

Highlights

© B.Jayet/CEA

October 2020

IOT Security

→ The Nanoelec/Pulse program and IRT Saint-Exupery take part in a webinar organized by the SCS competitiveness Cluster on the latest updates and user cases in **IOT Security**.

© Nanoelec/CEA

September 2020

X-rays shine

→ ESRF/EBS comes in operation after two years of upgrade. The new machine is the **most brilliant synchrotron in the world.**

SIDO 6th
IoT · AI · ROBOTICS · XR
#SIDO2020 - W 12
SEP. 03-04, 2020
LYON | FRANCE

© Sido

September 2020

Robotics & Digital Fair

→ Nanoelec/Easytech at the Sido fair combining **IoT, AI & Robotics** in Lyon.

September 2020

660 students in a (digital) classroom

→ For the very first time, 660 GEM students come together for an original **digital Back-to-School challenge** designed with Nanoelec.

October 2020

Best paper award for photonics

→ Andrea Quintero, PhD graduate receives a **Best Paper Award** at ECS Prime 2020 for her comprehensive study of the impact of Sn content on the Ni / GeSn phase sequence.

© GEM

© Serma

October 2020

Characterisation for powering GaN technology

→ 219 attendees for a webinar on characterisation techniques for **GaN components & systems** organized by Serma technologies, Nanoelec, Surface Lab and CEA-Tech.

November 2020

French public authorities renewed agreement

→ The contract renewal for IRT Nanoelec is finalized and signed by CEA and the French Research National Agency (ANR): It secures **institute funding** up to June 2023 with an allocation of 43 M €.

© P. Jayet/CEA

November 2020

Characterisation

→ The 7th edition of the Nanoelec/Carac **Symposium** attracts 50 attendees.

© Pixabay

November 2020

Silver Economy

→ Nanoelec experts involved in the Activage EU project participate in a workshop with more than 100 professionals addressing **senior care industry and services** in the Grenoble-Alps area.

© Schneider Electric

November 2020

Smart Building Management

→ STMicroelectronics, Schneider Electric and Lynred present the first integration of Edge AI in a **high-performance people-counting sensor** developed within Nanoelec.

© P. Jayet/CEA

Highlights

© Esisar

November 2020

Cyberweek

→ Esisar, a school of the Grenoble-INP group and a core member of Nanoelec, organizes the European node of CSAW, the most comprehensive **student-run cyber security event** in the world
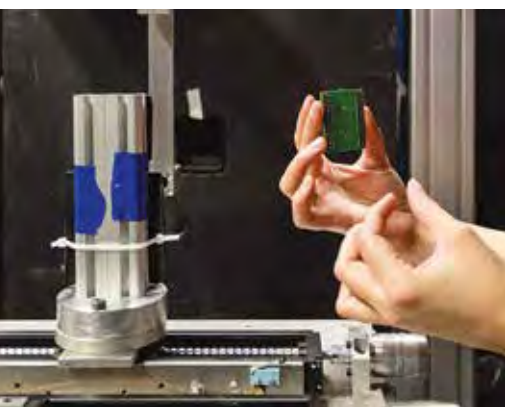
© P.Jayet/CEA

December 2020

Radiation testing of semiconductor devices and systems

→ Nanoelec/G-Rad workshop on current and future needs in **radiation hardness testing** and evaluating the limitations of radiation facilities and developments.

January 2021

Blockchain and digital identification

→ A public **comprehensive talk** by Christine Hennebert (CEA-Leti) associated with the Nanoelec/Pulse program.

December 2020

Open innovation

→ Preconfiguration of Nanoelec/SystemLab initiative, a new way forward for technology dissemination, by identifying **innovative use cases**.

© P.Jayet/CEA

© P.Jayet/CEA

February 2021

Sustainable Electronics

→ 57 students from Grenoble-INP and GEM took part in a **"Sustainable Electronics"** workshop organized as part of the Nanoelec/Human Capital and Training Engineering (Chif) program, with an original serious game "My IOT" created by Nanoelec and Need for IOT (Idex UGA).

© Pixabay

March 2021

Partners confidence renewed

→ Industrial and academic partners of Nanoelec finalize a new version of the **consortium agreement**.

March 2021

Open hardware

→ Nanoelec strongly supports the **Risc-V week** attracting close to 400 scientists from 33 countries.

© CEA

2nd RISC-V Week 2021
March 30th to April 1st

© F.Legrand/CEA

April 2021

Digital training transition

→ Grenoble Ecole de Management (GEM) "Back to school 2020 challenge" is praised for its positive societal impact by AACSB within the framework of the annual challenge **"Innovations that inspire"**.

March 2021

Woman Engineer

→ Severine Cheramy (Product line manager at Aledia) receives the **"Engineer of the year 2021"** award from the 3DinCites professional review dedicated to the international 3D architecture community.

May 2021

Display expertise

→ The **Fellow Award** of the Society For Information Display Fellow Award goes to François Templier, director of the Nanoelec/ Displed program.

© A.Alix/CEA

© P.Jayet/CEA

Highlights

June 2021

IOT security

→ Digifed Generic Experiment Community on **cybersecurity** is kicked-off with sixteen French and European SMEs interested in strengthening the security of their embedded applications for the Internet of Things (IoT).

May 2021

White paper

→ A 100-page report on **blockchain for personal identity privacy** is published by the French Interior Ministry, Thales and Nanoelec, with CEA.

May 2021

SMEs

→ Nanoelec/**Technology dissemination** program takes part in Minalogic Business Meetings 21.

© V. Pochat / CEA

June 2021

Gender matters

→ Nanoelec and Giant Campus organize a special public event on June 23th, the International **Women in Engineering** Day.

3D integration for image

3D integration, which consists in interconnecting electronic chips in 3 dimensions, is a promising solution to address the growing need for functionality, density and performance in future integrated circuits. However, to allow the rapid emergence of this technology in industry, an overall approach is needed, taking account of technological development, new circuits architecture, development of new design tools, testing and reliability technics.

From 2012 to 2020, the academic and industrial teams working under the Nanoelec/3D Integration program focused on developing a comprehensive platform compatible with the full design cycle of new products. They dealt with technology, but also design, electronic design automation tools (EDA), testing and reliability.

As of 2021, this activity is giving way to two new programs focusing on applications: one devoted to image display technologies (Displed) and the other to sensing (Smart Imager).

© B. Truong/CEA

Towards Display Technology Leadership in Europe

François Templier, CEA Research Director and Society For Information Display (SID) France Chapter Director, heads up the brand new Nanoelec/Displed program.

What drives you in the program you're heading up?

I've been managing CEA-Leti's Display Tech program since 2017. Management of the Nanoelec/Displed program allows me to broaden the scope of our cooperation with display manufacturers in a multilateral context. We should be able to accelerate our road map for supporting industry by getting stakeholders from different levels in the value chain around the same table. We intend to develop a radically new microLED-based, high-performance display based on a so-called "Smartpixel" chip, for which we'll expand the application fields and strengthen mass production processes. We'll open up the way to ultra-high resolution video walls, very large flat screens for television or interactive meetings, flexible displays and screens prompting a real feeling of 3-dimensional immersion in a virtual or remote world.

What is the Smartpixel you refer to?

It's a component that integrates a number of red, blue and green microLEDs into a unique control circuit co-assembled on a CMOS standard wafer. Each of these "Smartpixel" units is then transferred to a connecting media that constitutes the screen. This breakthrough approach will nevertheless require new developments, in particular the so-called "mass transfer" step. Ultimately, we'll benefit from higher performance displays enabling new functionalities; this represents a real technological and economic breakthrough. It's exactly this opportunity that we're adressing within the Nanoelec/Displed framework.

Why is it essential to continue developing very high performance image display systems and to be capable of manufacturing them in Europe and France?

By federating key industrial and academic players, our ambition is to rebuild a display industry in France and Europe that can be as strong as the one we had during the time of cathode ray tubes, which were ousted in the 1990s by LCDs of Asian origin.

We live in a society in which images are increasingly present. Why is this? Well, not only because people are staying longer and longer in front of displays, but also because they are seeking systems that are more immersive and free of the constraints such as 3D glasses, for example. New display technologies must ensure not

The Nanoelec/Displed program prepares real breakthroughs in the display industry value chain as well as new image functionalization.

© Pixabay

Displed program
at a glance

👁 **VISION**

A unique opportunity for a French & European ecosystem on large display technologies for immersive applications

📐 **AMBITION**

To design and demonstrate key microLED technologies towards high-end, immersive/interactive displays

🎯 **MISSION**

To develop process flows for microled, Smart-pixel fabrication and mass transfer requirements

👥 **PARTNERS**

Aledia | CEA | EVGroup | Plasmatherm | SET

---

only higher image qualities, but also enhance functionalities (3D Multiview, flexible screen, interactivity). It's legitimate that European and French industries build a solid offering in the microLED market, thereby taking advantage of its very dynamic growth, which should approach 3 billion USD in 2024, especially in relation to television (TrendForce market intelligence provider).

What is your career path?

I've been involved in digital display development for 28 years. I first worked at Thales before joining CEA in 1999. While performing the various functions of researcher, project manager and program manager, I've worked with every type of display (LCD, OLED, microLED, microscreens, flexible screens, TFT active matrices). Finally, my involvement as director of the France Chapter of the Society For Information Display (SID) allows me to continuously consolidate a 360° view of the state of the art in this field. ■

*FRANÇOIS TEMPLIER,
Director of the Nanoelec/
Displed program*
© P. Jayet/CEA

From imaging to vision sensing

The Nanoelec/Smart Imager program is committed to providing relevant and real-time environment analysis by vision. It could be one of the greatest technical challenges at Nanoelec for the coming years. Overview by Eric Ollier, Program Director.

What are the opportunities for smart imagers?

There is a growing number of applications where sensors become a vehicle for decision and action. There are market opportunities for consumers, smart buildings, healthcare, industrial process flows and monitoring, automotive and robotics. Mastering smart imagers industrial process flow would be a competitive advantage for Nanoelec's industrial partners.

Tell us why this program represents a real breakthrough and paradigm shift?

For the development of smart imagers, computing and data storage are the main challenge, in addition to image collection. Several technologies –CMOS image sensors, 3D stacking, AI, Neural Networks– are now mature enough to address new possibilities. A wide range of processing functions is possible, including multi-spectral management and associated data fusion. We have to 'wrap-up' these possibilities to build new functions in multispectral image analysis for example. To do that we must develop and combine the best 3D stacking technologies and also imagine the best architecture and partitioning between functions, including neural networks embedded in the smart sensor.

How does artificial intelligence integrate imagers?

To make the leap from image generation to information extraction, we intend to embed artificial intelligence processing inside the sensor. And this will require a dedicated embedded computing die. So we have to think about a new hardware and software architecture capable of enabling the implementation of a neural network and additional digital processing inside the smart sensor.

What is your strategy?

Our main goal is to evaluate the benefits of 3D-stacking technologies. This encompasses a wide range of inno-

vations in silicon technologies – process and characterization, design, design tools, architectures, software engineering - as well as in the field of software.

What in the Nanoelec background enables it to start such a challenging new program?

The previous "3D integration" program has been very active in terms of technological developments, publications and IP. The partners of the Smart Imager program intend to use this legacy and pursue this policy actively, especially to strengthen the foundations of our stacking technology for new 3D architectures.

Form your personal point of view, what is the most exciting part of the program?

I think what is most exciting is the fact that we have to find practical and industrial solutions based on the

most advanced technologies to embed artificial intelligence in the smart imaging sensor. It is also highly motivating to work in very close collaboration between R&D and industrial partners, working with various teams involved in hardware technologies but also in design, design tools, architecture, AI... Finally, it's very exciting to prepare the next generation of smart imaging sensors! ■

ERIC OLLIER,
Director of
Nanoelec/Smart
Imagers program
© P.Jayet/CEA

Smart Imager program at a glance

👁 VISION

The transition from imagers to vision sensors generates new market opportunities

📐 AMBITION

To provide key harware and software building blocks, to validate them through demonstrations ranging from test vehicles and proofs of concept to the prototyping of a smart, multi-layer imager

🎯 MISSION

• Stacking/3D technologies, embedded AI and data management,
• New architecture

👥 PARTNERS

CEA | Grenoble-INP | Lynred | Prophesee | Siemens EDA | STMicroelectronics |

Mastering smart imagers industrial process flow would be a competitive advantage for Nanoelec's industrial partners.

© Pixabay

COLLECTIVE DIE-TO-WAFER BONDING

EV Group, a core partner of the Nanoelec consortium, successfully demonstrates end-to-end process flow for collective die-to-wafer bonding with sub-two-micron placement accuracy, (see PR in last October). This breakthrough represents an important milestone in accelerating the deployment of heterogeneous integration in next-generation 2.5D and 3D semiconductor packaging. Such technologies are required for leading-edge applications such as artificial intelligence, autonomous driving, augmented/virtual reality and 5G, all of which require the development of high-bandwidth, high-performance and low-power-consumption devices without increasing production cost.

The demonstration was achieved at the EV Group Heterogeneous Integration Competence Center, utilizing existing EVG wafer bonding technology and processes, as well as existing bond interface materials, with substrates provided by Nanoelec and CEA-Leti.

" Markus Wimplinger, Corporate Technology Development & IP Director at EV Group, explains.

For EVG, what are the key benefits of wafer-to-wafer direct hybrid bonding for industry?

In recent years, leading semiconductor companies have stated in public that 3D integration technologies will be part of their next process technology nodes currently under development. This trend has boosted a growth of wafer bonding applications. Wafer bonding was first applied for CMOS image sensor (CIS) manufacturing. Going forward, it is moving to more mainstream applications such as NAND flash memory manufacturing, where hybrid bonding is used at first producers to integrate the cell array with the pe-

riphery circuit. Across all fusion and hybrid bonding applications, EVG provides clear technology to hold a dominant market share.

With the increased momentum for 3D integration for future logic devices, wafer bonding may reach certain limits. What are the key gaps to enlarge the range of applications using 3D integration?

One key gap for stacking technology is that wafer-to-wafer (W2W) bonding technology is not the only solution required for integrating chiplets with one another. There are many scenarios where die-to-wafer (D2W) integration will be required. Several approaches are under development, and have reached varying levels of maturity.

This relates to many of the building blocks involved, such as having a clear consensus on the preferred process flows as well as the pre-

cision and cleanliness of pick and place equipment. While it would be intuitive to favor direct placement/fusion bonding of the dies in the pick and place equipment directly onto the receiving wafer, there is room for alternatives process flows with a collective approach to avoid cleaning and plasma activation of individual dies.

How far are you looking to win new markets or to reinforce your position integrating this new process?

Many people believe that a "collective D2W" bonding flow[1] can be an efficient route toward achieving maturity and high yields for D2W fusion and hybrid bonding. EVG already has installations in the field that support this process flow in high volume manufacturing for non-mainstream semiconductor applications. The work done last year and presented in our press release has resulted in the

[1] Where the dies are placed on a carrier to be cleaned and plasma activated collectively – through wafer level processing – on this carrier.
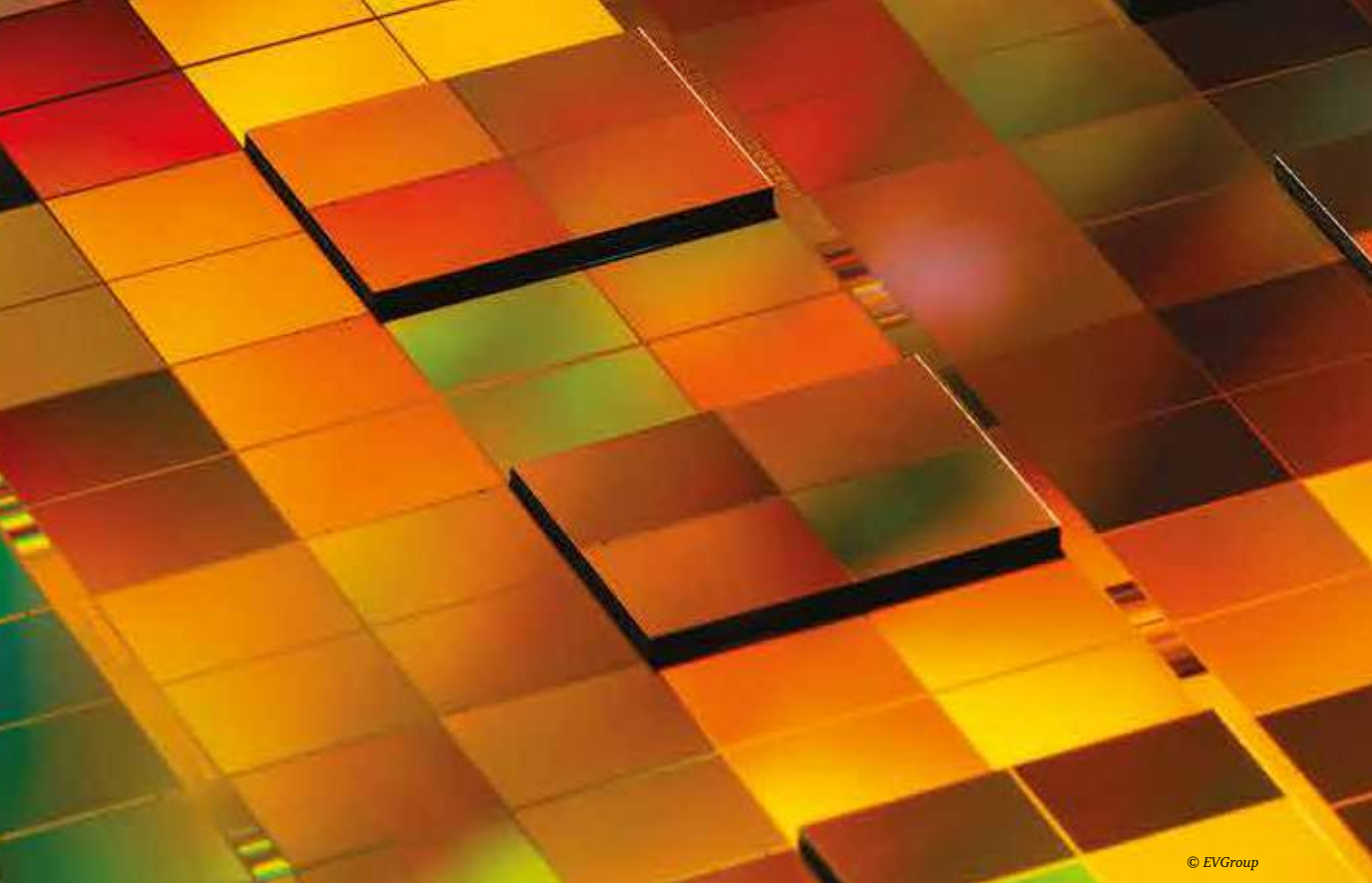
© EVGroup

definition and demonstration of an end-to-end process flow for collective D2W bonding that EVG can now offer to its customers via EVG's Heterogeneous Integration Competence Center.

Through this work, EVG has improved its industrial standard cleaning and surface activation technology. This could set a new standard for how D2W bonding, and in particular cleaning and surface activation, will be done. Therefore, we expect to reinforce EVG's leading position with respect to technology and the market.

What has been the contribution of Nanoelec to the demonstration of the full process?

IRT Nanoelec and CEA-Leti have been providing the wafer material required for this development work. The wafer material was set up to enable hybrid bonding using Cu interconnects. The work would not have been possible without this material. We would like to thank IRT Nanoelec and CEA-Leti for this important contribution.

Will the process be intensively used?

We have clearly seen a huge and growing interest in D2W bonding over the last few years. For this reason, we expect that the process will find significant interest and use in the industry.

How can EVG benefit from collaboration in the French Nanoelec institute?

EVG does not have the capability to prepare adequate test material in-house for such applications. For this reason, the partnership with CEA-Leti within IRT Nanoelec is very important, as it connects EVG with world-leading capabilities from the other partners in this consortium. Moreover, this collaboration gives EVG access to the required materials and technologies and also enables it to perform leading-edge research and development. ■

MARKUS WIMPLINGER,
Corporate Technology Development
& IP Director at EV Group
© EVGroup

The SET company developed its latest electronic components production equipment in collaboration with the IRT Nanoelec.

With more than 350 machines installed in clean rooms around the world, the company from Haute-Savoie, created in 1975, has been a cooperative since 2012, following the buy-out by its employees. The prototype of the NEO HB developed by SET, in partnership with Nanoelec, is being used in the clean rooms at CEA-Leti. The machine enables electronic chips to be produced with extremely high alignment precision.

© *Aubert/CEA*

ACCELERATING 3D INTEGRATION TECHNOLOGY IN INFRARED DETECTORS

Lynred, a global leader in designing and manufacturing high-quality infrared technologies for the aerospace, defense and commercial markets, joined the Nanoelec consortium in May 2020.

> *David Billon-Lanfrey, CSO in charge of Strategy, Corporate Communication and Technology at Lynred, explains some of the advantages that working with IRT Nanoelec will bring.*

Lynred has primarily joined Nanoelec to work on imaging developments. Are the projects you'll be working on specifically about infrared (IR) technology?

We specialize in infrared technology. That encompasses a very broad spectrum of technical solutions and applications designed for a very diverse range of sectors, including space imaging, thermographic imaging, defense systems and driverless vehicles. Lynred's IR sensors are critical components used by many of the major players in the commercial thermal imaging sector in Europe, Asia and North America. While maintaining our positioning in infrared imaging, we are keen to leverage key developments in a much wider market, that of visible-light imaging. This is our aim in working in collaboration with Nanoelec.

What are the challenges and obstacles you are facing in terms of technology and component modeling?

Like many developers in the electronic sector, and especially in the field of imaging, we take the 'More Than Moore' approach. That's the historical trend. Our first goal, therefore, is to reduce pixel pitch on our imagers so that we can achieve higher resolution images. We can use 3D architecture to help us achieve higher resolutions.

This should also enable us to integrate new smart signal processing functions, at pixel level, as well as to produce lighter, more compact imagers. Thanks to 3D stacking architecture, we will be able to diversify the range of applications and markets for our solutions.

CMOS technology cannot be directly transposed for infrared applications, notably because our imagers are cooled, usually to −150°C, and this is not the case for components used in applications that are more conventional. Another major difference compared to visible light imagers is that most electronic components are produced on 300 mm silicon wafers, the most widely-used industry standard, whereas our components are produced on 100 mm or even smaller wafers. As you can see from these examples, we need some R&D to adapt the cutting-edge 3D technology developed at the Nanoelec IRT to our needs.

What attracted you to the multipartner environment at Nanoelec?

We see it as essential to maintain close links with the innovation ecosystem in the field of microelectronics. Nanoelec provides a great environment for pursuing R&D with the different partners working within that ecosystem. Innovation is the key to be able to build and develop new competitive advantages in a market increasingly dominated by players in the USA and Asia.

Is Nanoelec also likely to open up new markets for your products?

By integrating image-processing functions within the sensor, we hope to create imaging solutions with high benefit for our customers in extremely demanding markets in terms of product performance, from military aeronautics to driverless vehicles. For example, for next-generation fighter jets, this would provide longer-range imaging for reconnaissance missions, and improve self-protect and threat-detection systems. For the next generation of vehicles, this will improve safety, even in poor visibility conditions such as darkness and fog. ■

DAVID BILLON-LANFREY,
CSO in charge of Strategy, Corporate Communication and Technology at Lynred
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**Developed by CEA-Leti
and STMicroelectronics
within Nanoelec,**

Intact is an architecture with 96 cores
and 6 micro-chips stacked (FDSOI 28 nm)
in 3D on an active silicon interposer (CMOS
65 nm). The demonstrator has been entirely
processed, packaged and tested.

LEVERAGING IC DESIGN TOOLS AVAILABLE FOR 3D ARCHITECTURE DESIGN

Siemens EDA (ex. Mentor Graphics) is the sole EDA (Electronics Design Automation) partner of Nanoelec. It is providing design & verification tools for the benefit of the Nanoelec research institute's designer community. In addition to providing this valuable support, Mentor also uses the community's feedback to continually improve its design tools within the context of their performance in use on IntAct sophisticated demonstrators.

" *Juan Rey,*
VP Engineering at Siemens EDA Design2Silicon Division, focuses on accurate physical verification of innovative 3D-IC designs.

How has Siemens EDA's Calibre 3DSTACK been an essential tool for the architecture design of Intact, the 3D manycore circuit partitioned using an active interposer presented by Nanoelec last year?
The accurate Physical Verification of such highly complex demonstrators requires efficient and high performance engines made available through a leading edge product suite. A fundamental tool in the signoff verification of 2.5D/3D-IC designs is Calibre 3DSTACK. Calibre 3DSTACK extends Calibre die-level signoff verification to enable complete signoff verification of a wide variety of 2.5D and 3D stacked die assemblies. With Calibre 3DSTACK, designers can perform signoff DRC and LVS checking of complete multi-die systems at any process node without breaking current tool flows or requiring new data formats, significantly reducing time to tapeout.

How does Siemens EDA's Calibre 3DSTACK benefit the Nanoelec IntAct demonstrator?
Calibre 3DSTACK was used extensively during the IntAct demonstrator signoff/final verification (before manufacturing), allowing for the capture of errors that traditional '2D' tools would have missed given the complexity of such design. The consequences of failing to capture these errors during the verification stage could have been substantial, resulting in either a functionality/specification limitation or even worse, a complete chip failure.

Does Siemens EDA also provide innovative tools for reliability and physical stress analysis?
In addition to providing this signoff 'stamp' to IRT Nanoelec demonstrators, Siemens EDA is also proposing innovative prototype tools for IRT Nanoelec partners. Thermal analysis for 2.5D/3D has been one strong research axis over the past years, allowing CEA-Leti to perform architectural studies for their future demonstrators. 2.5D/3D Reliability and physical stress analysis are other topics of interest that Siemens EDA and Nanoelec partners will continue to study over the coming months. ∎

JUAN REY,
VP Engineering at Siemens EDA Design2Silicon Division
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VIPs in Science

SEVERINE CHERAMY

Product line manager at Aledia,
received the "Engineer of the year 2021" award
from the 3DinCites professional review dedicated
to the international 3D architecture community.
Until last February, Séverine was senior business
developer at CEA and director of the former
Nanoelec/3D integration program.

Severine Cheramy (Product line manager at Aledia) received the
"Engineer of the year 2021" award from the 3DinCites review
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FRANÇOIS TEMPLIER

Strategic Marketing manager for displays at CEA and director
of the Nanoelec/Displed program,
received beginning of 2021 the Society For Information Display fellow award
"for his many contributions to the science and technology of thin-film transistors,
flexible displays, OLED microdisplays, and GaN micro-LED displays."

3D DEMONSTRATORS FOR DISPLAYS

Within Nanoelec, Aledia and CEA-Leti are developing their technological know-how
in order to produce new types of displays that are brighter, offer more dynamic contrast
and display speed and are more energy frugal.

"These developments employ all the know-how of the Nanoelec/3D program for match-up, plate to plate assembly and interconnection of a light emitting module (LEM) pixelated wafer with a CMOS wafer. The aim is collective interconnection of hundreds of millions of 3D LEDs with CMOS components, with the LEMs providing brightness in three colors (red-green-blue in a single pixel) while the CMOS wafers house
the pixel control function", says Philippe Gilet, CTO & Co-founder of Aledia.

The various technological building blocks are being studied in parallel by means of demonstrators. In 2020, the proofs of concept were specified and designed, in particular for interconnections between the various layers of 3D pixels. *"The challenge is to succeed in achieving assemblies of plates and not of individual*
pixels", points out Séverine Chéramy, Product Line Manager at Aledia. *"And we are aiming for production in accordance with microelectronics standards (200 or 300 mm on silicon) whereas most of today's practices use more specific substrates with small surface areas. Standardized production will enable us to significantly bring down costs."* ■

Key publications

Embedded ultra-thin silicon vapor chambers for the cooling of microelectronics device hotspots

Thermal management, and more precisely hotspots attenuation, have nowadays become one of the most critical aspect in the design of microelectronic components, especially in the case of compact mobile applications. For his PhD thesis, Quentin Struss studied the design, the fabrication and the characterization of an ultra-thin silicon vapor chamber integrating a micropillars capillary wick. It can be directly embedded on the backside of a CMOS component in order to reduce hotspots intensity.

"A vapor chamber is a passive phase-change cooling device, which evaporation and condensation cycles leads to significantly higher heat transfer performances compared to classical heat spreading solution. A numerical estimation of such device made out of silicon with a total thickness of 600 µm has shown a 1.2 K.W-1 reduction in thermal resistance compared to a classical copper heatspreader with the same dimensions", Struss underlines. *"We combined analytical and numerical models and experiments to demonstrate a microfabrication process flow, compatible with the presence of a CMOS component on the front side. An innovative collective wafer level filling and sealing approach has also been developed and allows, for the first time, the fabrication of a silicon vapor chamber with no filling hole, bringing these devices closer to an industrial production."* Quentin also presented his work in a paper at 2020 Electronic Components and Technology Conference (IEEE 70th ECTC).

QUENTIN STRUSS
Vapor Chambers for high performance two-phase spreading/cooling

Thesis defended on Dec.18, 2020 at Insa Lyon in collaboration with Univ; Sherbrook (Canada), CEA-Leti, STMicroelectronics and Nanoelec

Increasing chip-to-chip bandwidth in an active 3D interposer

Perceval Coudrain (CEA-Leti) who works on 3D integration and advanced packaging as part of the 3D Integration program, received the "Best Paper Award" at the ECTC conference (in May 2019, Las Vegas, USA) for his article titled "Active interposer technology for chiplet-based advanced 3D system architectures". *"An active interposer enables the addition of smart features to the final 3D system, such as advanced network-on-chip (NoC) interconnects, fast I/Os for off-chip communication, embedded power management and system-on-chip (SoC) infrastructure"*, Coudrain said. *"Our paper reported on the first successful technological integration of chiplets on a fully processed, packaged and tested active silicon interposer"*. The prize was officially announced in January 2020.

PERCEVAL COUDRAIN & AL
Active interposer technology for chiplet based advanced 3D system architectures

2019 IEEE 69th Electronic Components and Technology Conference (ECTC)
DOI:10.1109/ECTC.2019.00092

Image sensors require complexes architecture

Introducing his communication at 3D System Semi Summit, François Guyader (STMicroelectronics) underlines the great interest of 3D integration and partitioning for image sensors and the advantage of scalability offered by the hybrid bonding technology. Showing results obtained at CEA-Leti and STMicroelectronics, within the frame of Nanoelec, he demonstrated that parallel hybrid bonding combined with sequential stacking offer scalable solutions to reach more and more complexity in architectures.

FRANÇOIS GUYADER & AL
3D Integrations for Smart Image Sensors
3D System Semi Summit
January 2020

Releasing hpc & big data applications for 3D technology

At the ISSCC 2020 conference, (February 2020, San Francisco, USA), CEA teams reported on a high-performance processor breakthrough achieved as part of the 3D Integration program. They implemented an active interposer as a modular and energy-efficient silicon platform that enables efficient integration of large-scale chiplet-based computing systems for high-performance computing (HPC) and big-data applications.

"This is a breakthrough in terms of system-and-architecture integration, achieved all the way from the architectural design down to a silicon prototype", says Pascal Vivet (CEA-List), the lead author of the paper. *"In addition, 3D technology and associated design techniques are now available for implementing large-scale computing systems, thus offering a chiplet-based 96-core computing architecture for the first time."*

PASCAL VIVET & AL.
A 220GOPS 96-Core Processor with 6 Chiplets 3D-Stacked on an Active Interposer offering 0.6 ns/mm Latency, 3 Tb/s/mm2 Inter-Chiplet Interconnects and 156 mW/mm2 @ 82% Peak-Efficiency DC-DC Converters
ISSCC
February 2020

Through-Silicon-Via for 3D stacking

In a paper published in MRS Communication, a CEA-Leti team acting within Nanoelec, studied the combination of Cu-to-Cu direct hybrid bonding technology with Through-Silicon-Via (TSV) to allow 3D interconnection between pixels and the associated computing and memory structures, with each function being fabricated on a separate wafer. "Process developments are mature and can be reliably used in the fabrication of an electrical test vehicle including vertical interconnects associating multi-wafer stacking with a hybrid bonding process and high-density thin TSV applicable to low pitches (<5 µm)", comments Lucile Arnaud, as first author of the paper.

LUCILE ARNAUD & AL.
Three-dimensional hybrid bonding integration challenges and solutions toward multi-wafer stacking
MRS Communication (Material Research Society),
September 2020

3D-integration technology and architecture breakthrough to power exascale computing

"Profound changes brought about by high performance computing (HPC) applications are based on continuous and exponential increases in computing performance over the past decades", explains Denis Dutoit (CEA-List) who was a guest speaker at IEDM 2020. He underlined the benefit of a cross disciplinary approach in 3D technology and architecture "It enables high-performance processors that will power exascale-level HPC, he says. State-of-the-art 3D toolbox and architecture that we developed within Nanoelec enable higher bandwidth and heterogeneity for processors."

Exascale computing refers to computing systems capable of calculating at least 10^{18}, or one-billion-billion, floating-point operations per second, which would be twice as fast as the fastest computer available today. Efforts to develop exascale computing are driven by highly data-intensive scientific and industrial applications, such as climate research, drug discovery and material design. This level of performance in HPC and Big Data will be achieved with heterogeneous computing nodes composed of generic processor chiplets hosting accelerator chiplets for improved operational intensity.

DENIS DUTOIT & AL.
How 3D integration technologies enable advanced computer node for Exascale-level High Performance Computing
IEEE IEDM
December 2020

Photonic Sensors

Along the optical sensors procurement chain

4 questions to Christophe Kopp, Head of the Nanoelec/Photonic Sensors program
& Head of the Section of New Photonic Applications at CEA-Leti

CHRISTOPHE KOPP (CEA), Director of the Nanoelec Photonic Sensors Program

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What is the potential for optical sensor applications?

In functional terms, optical sensors are well-known for their accuracy, sensitivity, selectivity, versatility and acquisition speed. Thanks to micro-technology integration, their miniaturization is opening up new markets in a wide variety of fields such as environmental monitoring, urban planning, health, industry or energy, but also consumer applications. The digital transformation of our society is leading to the deployment of billions of sensors and sensor networks. They are used across a broad spectrum of applications such as gesture recognition, presence detection, smart heating, etc. The rising adoption of automation in various sectors is speeding up the growth of the market for these sensors.

The global market for optical sensor applications already stands at more than 20 billion dollars, with a target annual growth rate in excess of 10% over the coming decade [1].

[1] Global Market Insights.

© P. Jayet

What innovations will sensors carry in the coming years?

These new sensors must be accurate, be as small as possible and consume very little energy. Moreover, their architecture must be compatible with the means of collective manufacturing. These sensors will be based on the use of photonic chips built on production lines derived from the microelectronics sector. This technology and its industrial ecosystem were initially developed for the high speed optical datalinks market. Today, optical sensors require that the spectral bands that can be addressed be expanded from the visible to the infrared, with functionalization of the detection surfaces.

What technological challenges do you face?

The main technological challenges for these sensors are the accuracy and stability of measurements, miniaturization, data processing and transfer, and compatibility with the constraints of mass production. The unique properties and the performance of integrated photonics are essential in meeting these requirements. We aim at implementing thousands of functions on the same photonic chip. New components and new technological building blocks are required together with the digital tools needed to design these complex photonic circuits, along with automated characterisation techniques.

What are the goals of the program you are running?

Our aim is to speed up innovation and give a technological edge to our industrial partners along the optical sensors procurement chain. In the light of the expected growth mentioned earlier, we ambition to consolidate the technological lead by French players in the field so that they can be on a par with the best in the world. To achieve this, we are pursuing a three-fold goal with them: increasing the maturity of the 200- and 300-mm photonic platforms, developing innovative processes and devices (integration of laser sources in particular) and, finally, implementing application demonstrations. ■

Photonic Sensors program at a glance

◉ VISION

New sensor opportunities based on large scale 300mm silicon photonic technologies

⚒ AMBITION

Enrich our photonic prototyping and industrial platforms with key building blocks enabling new sensors to address Medtech, Environment, Consumers goods, Mobility (Lidars) and Computing

◎ MISSION

- Miniaturize sensors
- Diversify the fields of applications
- Manage the integration of thousands of functions on the same chip
- Increase technology readiness level using CAD tools and enrich our device library including performance corners, fabrication process flow

⚇ PARTNERS

Almae | CEA | CNRS | Siemens EDA (ex. Mentor Graphics) | STMicroelectronics

CONTINUOUSLY IMPROVING DESIGN TOOLS FOR SILICON-BASED PHOTONICS

As a core partner of Nanoelec, Siemens EDA (ex. Mentor Graphics) is providing design & verification tools for the benefit of the Nanoelec designer community. The EDA leader also uses feedback from the community to continually improve its design tools in the context of sophisticated demonstrators and platforms. Tom Daspit, Product Marketing Manager at Siemens EDA focuses on design & verification tools for Photonics-on-Silicon applications.

Why are design tools essential for enabling growth in photonic design?

Photonics-on-Silicon has a wide range of applications in data centers, HPC and telecommunications. The promise of leveraging high-volume, low-cost manufacturing techniques in photonics-on-silicon circuit manufacturing has the potential to extend the range of photonics applications to smart sensors targeting new areas such as autonomous vehicles, autonomous robots, healthcare and more.

Extending and leveraging current silicon design tools in order to seamlessly and productively integrate photonics functions with CMOS-based electronics is a key enabler for high-volume, high-performance photonics circuits.

What are the main methodologies for architecture design in photonics?

Today, there are two main photonic design methodologies: scripted and custom layout. Both are good for creating small designs, but they become inefficient as the design
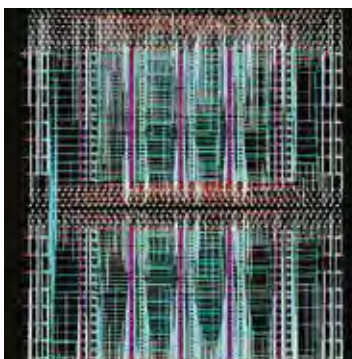
Silicon photonics switch layout based on CEA-Leti/Siemens EDA PDK
© CEA-Siemens EDA

size increases from tens, to hundreds, to over a thousand components in the design.

Photonic design can benefit from the forty-plus years of industry improvements in IC process technology, methodologies and design tools. Ultimately, the availability of more photonic processes should be able to support much larger designs.

IC design sizes have grown from thousands, to millions, to billions of transistors in today's processors. This growth was enabled by automating IC design tasks. Automation is not just tool-centric, it relies on

the underlying design methodology that supports it. An example of digital place and route is LEF/DEF, a standard that abstracts the data to the minimal set that is needed. LEF/DEF is derived from a standard cell design methodology and standard cells are created from individual transistors built up from the data in a Process Design Kit (PDK).

What is the step forward provided by the Siemens EDA LightSuite Photonic Compiler?

Siemens EDA addresses photonics by supporting both automated and custom layout tools. We are focused on driving state of the art layout automation with our LightSuite Photonic Compiler. Considering a 4 by 4 switch, the layout was automatically created in under 5 minutes. Now scale that switch to a 16 by 16. The complexity of such a change requires complex optical and electrical routing. This DRC clean layout is implemented in 85 minutes. Manual layout of a design of this size would take many months to implement. ■

WIDESPREAD USE OF LIDAR SYSTEMS BASED ON INTEGRATED OPTICAL PHASED ARRAYS (OPAS)

Taking a critical step towards developing Lidar systems for widespread commercial applications, teams at Nanoelec have developed generic algorithms to calibrate high-channel-count optical phased arrays (OPAs), as well as an advanced measurement setup enabling wafer-scale OPA characterisation.

OPAs are an emerging technology made of arrays of closely spaced (around 1 µm) optical antennas which radiate coherent light in a broad angular range. The interference pattern produced can be changed by adjusting the relative phase of the light emitted by each antenna. For example, if the phase gradient between the antennas is linear, a directional beam formed. By changing the slope of the linear gradient, the direction of the beam can be controlled, which enables solid-state beam steering.

"The development of a high-performance OPA would pave the way for inexpensive Lidar systems for autonomous vehicles, holographic displays, biomedical imaging and many other applications», says Sylvain Guerber, the lead author of a paper from CEA-Leti and STMicroelectronics at the 21'Photonics West International Conference.

"This can improve performance in scanning speed, power efficiency and resolution compared to the heavy, power-hungry and expensive mechanical beam-steering systems used in current lidars. An additional feature of OPA-based lidar systems is that they have no moving parts, as solid-state beam steering is achieved simply by phase-tuning the antennas, which significantly reduces the size and cost of these systems", he adds.

Lidar, which stands for light detection and ranging, has emerged as a key enabling technology for tomorrow's sensing and vision systems. In addition to automotive and medical uses, they could enable autonomous mobility for drones and robots, as well as industrial automation. Commercial Lidar systems must meet stringent requirements, especially for automotive applications. In particular, a high-power, low-divergence beam is needed to accurately resolve a scene. For example, resolving a 10-cm object at 100 m requires an OPA operating at a wavelength of 1 µm with a circuit consisting of at least 1,000 antennas, each spaced 1 µm apart. Therefore, the development of high-channel-count OPAs is necessary for a commercial OPA-based Lidar system. ■

Sylvain Guerber (CEA-Leti) prepares a series of tests on the new "Lidar bench" set-up installed in 2020. The white fiber is used to inject light into the circuit. The blue sensor electrically controls the phase shifters in the Lidar circuit (steering of the laser beam which exits the chip to scan the visible space, with no moving parts). In red: a camera observes and measures the steering of the beam exiting the Lidar.

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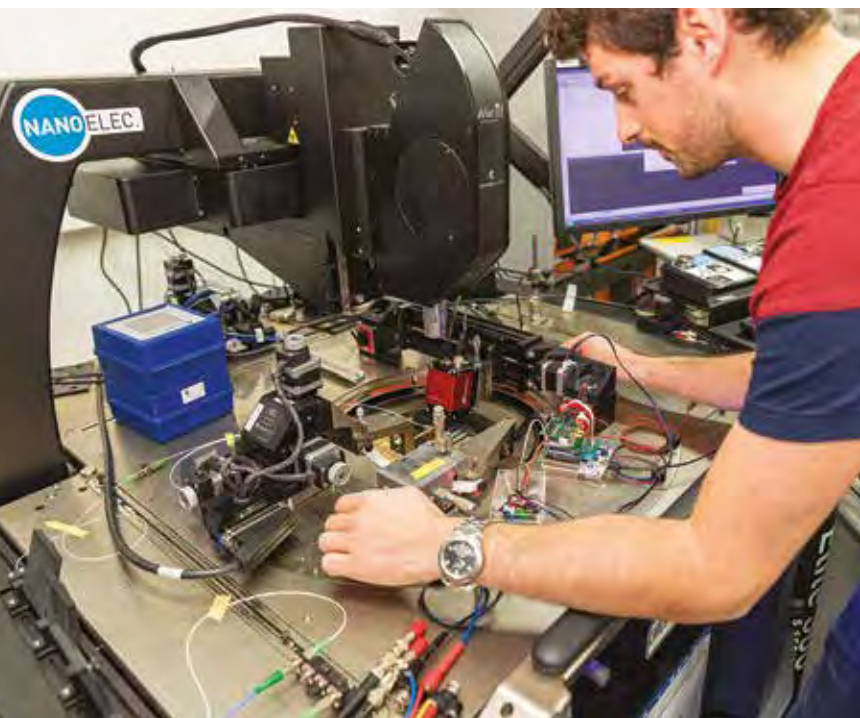
*Nanoelec Double hexapod arms
(2x6 degrees of freedom) used to align
photonics components with a laser source*

© P. Jayet/CEA
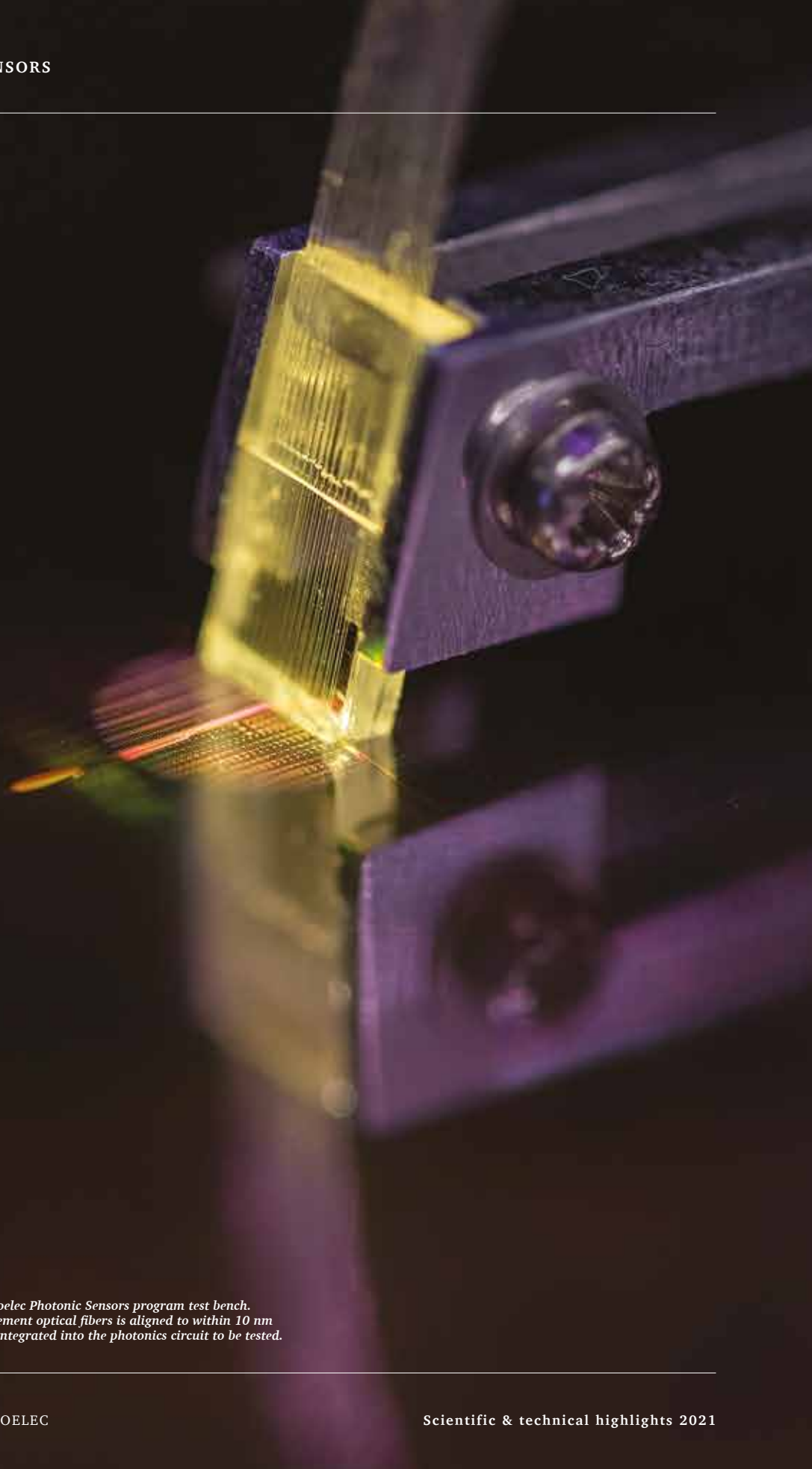
At CEA-Leti, on a Nanoelec Photonic Sensors program test bench.
The bundle of measurement optical fibers is aligned to within 10 nm
on the light channels integrated into the photonics circuit to be tested.
© P. Jayet/CEA

NANOELEC AND SOITEC TO SUPPORT THE STARTUP SCINTIL PHOTONICS

Nanoelec is supporting Scintil Photonics, a startup created in 2018, with the development of III-V/Si integrated circuit demonstrators/prototypes by developing technological building blocks, such as die-to-wafer bonding, manufacturing III-V on silicon parts and supporting design and testing activities.

"Soitec, one of the partners in the Nanoelec consortium, joined our board of directors, in 2020. The company brings us its technological expertise and international market", says Sylvie Menezo, CEO and CTO of Scintil Photonics. *"Also in 2020 we signed our first contract with a leading European telecom equipment supplier."*
"Scintil Photonics offers integrated photonic circuit solutions for high-speed optical communications. These circuits are also very promising for 3D sensing and quantum photonics applications, allowing to tackle dynamic growth markets, respond to new customer needs and significantly enhance our product portfolio," said Thomas Piliszczuk, executive vice president of global strategy at Soitec.

Scintil Photonics aims to develop products for the generation, modulation and photo-detection of very high speed signals (800 Gbps per wavelength) for the data networks market for storage or computing centers (Active Optical Cables, High Speed Short Reach Interconnects). This rapidly expanding market is increasingly turning to integrated photonic solutions, owing to the rise in the transmission rates (electronic-optical integration) and the growth in volumes (the traditional technologies which required manual assembly of parts are no longer sufficient). The III-V on silicon integration developed within Nanoelec constitutes the heart of the Scintil Photonics technology: this integration allows the creation of an externally modulated laser, for which the expected performance is state-of-the-art and the process is compatible with mass production (therefore offering low costs). ■

PDK MAKES PHOTONIC CIRCUIT DESIGN EASIER

An integrated Process Design Kit (PDK) has been included in the Siemens EDA (ex. Mentor Graphics) Tanner design flow and it is now opened up to Nanoelec partners.

"For manufacturing of future circuits on the CEA-Leti 310nm platform, the PDK is a real time-saver. The main target applications are datacoms, telecoms, Lidars, HPC, and neuromorphic chips", Eleonore Hardy, CEA-Leti business developper, underlines.

CEA-Leti and Siemens EDA are collaborating as core partners of the Nanoelec consortium. *"The PDK provides access to a library of proven components and can also be used to design new ones. It is also fully compatible with LightSuite, another Siemens EDA tool that automates the routing of optical and electrical lines and it is also integrated as part of our know-how"*, adds Hardy. ■

© AdobeStock
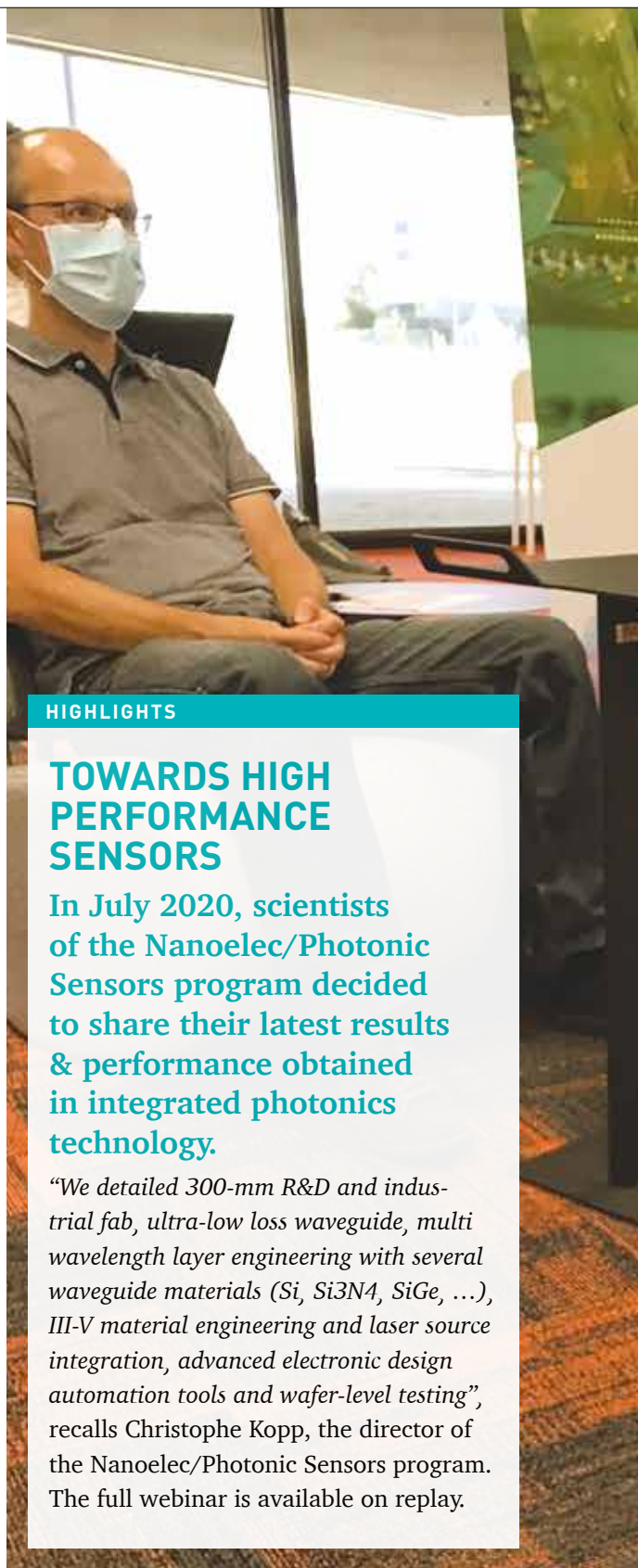
HIGHLIGHTS

TOWARDS HIGH PERFORMANCE SENSORS

In July 2020, scientists of the Nanoelec/Photonic Sensors program decided to share their latest results & performance obtained in integrated photonics technology.

"We detailed 300-mm R&D and industrial fab, ultra-low loss waveguide, multi wavelength layer engineering with several waveguide materials (Si, Si3N4, SiGe, …), III-V material engineering and laser source integration, advanced electronic design automation tools and wafer-level testing", recalls Christophe Kopp, the director of the Nanoelec/Photonic Sensors program. The full webinar is available on replay.

EDUCATION & TRAINING

Teams from the Nanoelec/ Photonic Sensors program disseminate their knowledge and know-how extensively through numerous publications and courses.

For example, in February 2020, Benoit Charbonnier (CEA) was invited to the Thales Research Center in Paris-Saclay within the context of the European Network for High Performance Integrated Microwave Photonics. He gave a short course on silicon photonics for communications and new applications. In November 2020, Quentin Wilmart (CEA) discussed Si capacitive modulator integration in a 300-mm Si photonics platform using different annealing conditions, as part of an intensive short course in silicon nitride integrated photonics by the European Silicon Photonics Alliance.

In 2021, CEA-Leti acquires a rotary bench to test the performance of optical gyroscope prototypes designed and prototyped under the Nanoelec/ Photonic Sensors program.

The turntable can be used for operating rotation speed measurements from 0.001 °/sec to 1,500 °/Sec with a precision of 0.005%. The aim is to eventually develop gyroscopes for mass market applications.

Nanoelec rotary test bench at CEA-Leti
© P.Jayet/CEA

Recording the CEA-Leti digital workshop on emerging photonic and integration technologies for healthcare

© CEA

PHOTONICS FOR HEALTHCARE

On March 2021, CEA-Leti broadcast a digital workshop on emerging photonic and integration technologies for healthcare.

Bertrand Bourlon, Head of the Optical Sensors Lab at CEA-Leti, presented advances powered by Nanoelec on mid-infrared sensors tackling environmental and medical challenges. *"Such sensors enable higher specificity in cost-effective miniaturized sensors & systems",* he underlines, calling up several fields of application like process or air-quality monitoring, cross biochemical and morphological information for health. *"Other fields such as energy and defense might be also addressed by mid-IR imaging integrated photonic sensors",* he adds.

Key publications

New contacts on GeSn alloys for optoelectronic devices

The semiconductor industry is constantly striving to improve various parameters in order to increase the performance and data transfer speed of optoelectronic devices: this includes changing the steps in the production processes, the device architecture or the materials that constitute the devices. In her PhD Thesis, Andrea Quintero worked on the development of contacts on GeSn alloys. *"Germanium-Tin (GeSn), group-IV alloy is an interesting material for integration into electronic or opto-electronic devices and we focused on systematic and comprehensive development and characterisation of Ni/GeSn intermetallics to contact GeSn-based devices",* she explains. Results were obtained at

the CEA-Leti in collaboration with C2N (Univ. Paris Saclay / CNRS), within the framework of Nanoelec. *"They represent a good starting point for producing high-quality, stable and reliable GeSn-based contacts that can be fully integrated into electronic or opto-electronic devices",* adds Quintero. Andrea Quintero has published ten papers on the phenomenon over the past three years, even winning a Best Paper Award at ECS Prime 2020.

ANDREA QUINTERO
Development and characterisation of contacts on GeSn alloys

University Paris-Saclay (U-Psay) thesis defended on october 16th 2020 at CEA-Leti in partnership with C2N (U-Psay & CNRS), Orsay Faculty of science and Nanoelec

Integrating an optical source directly on a silicon chip

In order to meet the nedd for circuits with integrated optical interconnections, Marie-Léonor Touraton's PhD thesis studied the possibility of integrating an optical source directly on a silicon die. "I specifically studied the technological building blocks enabling the integration of light sources, emitting from the red region of the spectrum to the L band, by mean of selective epitaxy of various III-V materials. For various wavelength ranges, we demonstrated the integration of III-V materials stacks in the form of ridges", she says. With support from Nanoelec, a first version of electrically pumped components, like ribbon diodes, on GaAs and silicon substrates was manufactured and characterized.

MARIE-LÉONOR TOURATON
Direct epitaxy of III-V semiconductors on silicon substrate for photonic devices

Thesis defended on June 22nd 2020 at University Grenoble-Alpes (UGA) in collaboration with CEA-Leti, CNRS-LTM, STMicroelectronics and Nanoelec

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Optical switch to replace copper interconnections in ICT components

Silicon photonics look to be a promising solution for replacing copper interconnections for communication requirements that are heavily integrated inside data centers, inter and intra chip links. To achieve high data rates, one can use multiplexing on optical links combined with disaggregated resources. In such architectures, an optical switch being able to cope with high size and data rate is a core element to be designed. During his PhD, Nicolas Michit focused on intrachip interconnections on a photonic interposer, based on wavelength multiplexed links around the 1310-nm communication channel. *"We were interested in optical switching,* Michit says. *At first, the decision to use ring resonators based links was justified in terms of compactness, network flexibility and low optical losses. These structures are however very sensitive to the environment and to geometry fluctuations: it is important to understand clearly the physical effects involved. We described different ring resonance models to create a model that is both analytical and accurate enough to describe the peak shifts observed experimentally. This work gave us a better understanding of the ring parameters in order to minimize its impact on a wavelength-division multiplexing (WDM) link."*

NICOLAS MICHIT
Optical switch for the design of fast wavelength-division multiplexing (WDM) links in silicon photonics

Thesis defended at Lyon University in collaboration with Insa-Lyon, INL, STMicroelectronics (CIFRE contract) and Nanoelec

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A CMOS-compatible laser

For her PhD, Flore Boyer worked on optimizing performance of optoelectronic circuits for high-density data transmission. An innovative integration scheme has been developed in collaboration with STMicroelectronics and CEA-Leti. It consists in the full integration of the III-V emitter, which is a III-V/Si hybrid laser, on a silicon wafer in a 300 mm CMOS-compatible clean room. *"We focused on the components required for such integration, in particular CMOS-compatible contact layers of the laser, necessary for the generation and amplification of the optical signal,* Boyer reports. *We then demonstrated promising and reliable metallization for the full integration of III-V/Si hybrid laser onto a 300-mm Si fab-line."*

FLORE BOYER
Integration of CMOS-compatible contacts on III-V materials for photonic devices on silicon using the 300-mm platform

Thesis defended at Université Grenoble-Alpes in collaboration with CEA-Leti, STMicroelectronics and Nanoelec

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Best Paper award

Andrea Quintero received a Best Paper Award at ECS Prime 2020 for her comprehensive study of the impact of Sn content on the Ni/GeSn phase sequence. *"We performed morphological and electrical properties characterisation during the solid-state reaction",* reports Quintero. *"Sn segregation around grain boundaries hampers atom diffusion, delaying the growth of the Ni(GeSn) phase. In addition, we observed a correlation between the Sn content and degradation of the morphological and electrical properties. This prize rewards Andrea's amazing efforts and work during the 3 years of her PhD Thesis",* underlines Philippe Rodriguez, Head of the Advanced Materials Deposition Laboratory at CEA-Leti.

ANDREA QUINTERO & AL.
Analysis of Sn Behavior During Ni/GeSn Solid-State Reaction by Correlated X-ray Diffraction, Atomic Force Microscopy, and Ex-situ/In-situ Transmission Electron Microscopy

ECS Prime October 2020

CMOS-compatible contact technology on III–V materials

S. Bensalem et al. recently published their "study of the Ti/InGaAs solid-state reactions: Phase formation sequence and diffusion schemes" in Materials Science in Semiconductor Processing. The development of CMOS-compatible contact technology on III–V materials based on Ti for electronics or photonics applications has been carried out at Nanoelec by scientists from CEA-Leti, STMicroelectronics and the Hungarian Academy of Science Center for Energy Research. *"We studied solid-state reactions between Ti thin films (20 nm) and InGaAs layers grown on InP substrates from the as-deposited state up to 550°C using a combination of advanced X-ray diffraction (in-plane reciprocal space mapping), Auger electron spectroscopy and transmission electron microscopy analyses"* underlines Philippe Rodriguez, as corresponding author for this paper. *"The complete knowledge of the phases present and their spatial localization is essential in order to understand and tailor the electrical properties of the Ti-based contacts on InGaAs. It is also important to anticipate and control the impact of the integration scheme in terms of additional thermal budget for instance."*

Electro-refractive modulators to reduce energy needs

Silicon photonic modulators are a key component for electro-optic transmitters in data centers. Electro-refractive modulators relying on free carrier plasma dispersion in a Mach-Zehnder interferometer have become the most popular solution. Accumulation–based capacitive modulators are an efficient approach, which can reduce modulation power consumption. Preparing his PhD thesis with the support of core partners of Nanoelec (CEA-Leti, CNRS & STMicroelectronics), Ismael Charlet studied the behavior of capacitive modulators with polycrystalline silicon to form the capacitance. *"The modulators are made within the standard fabrication flow with only a few add-ons. We demonstrated that furnace annealing conditions and excimer laser annealing conditions during polycrystalline silicon formation enhance the modulator bandwidths"*, he says. The results were reported at the 21'Photonics West International Conference.

Designing a photonic process flow for hybrid lasers

Ar and He plasma might be used to pre-clean InP prior to nickel contact deposition. The integration of III-V/Si hybrid lasers on a 300-mm platform for photonic applications requires the development of dedicated CMOS-compatible contacts, for which those based on nickel are very good candidates. A team from STMicroelectronics, CEA-Leti and Grenoble-INP, working together on this subject within Nanoelec, compared the impact of in situ pre-clean based on argon (Ar) or helium (He) plasma on the surface integrity of InP prior to nickel (Ni) contact deposition. The results were presented in the Journal of Vacuum Science & Technology B. *"We observed that Ar pre-clean significantly damages the InP surface by generating high roughness and creating indium (In) dots on the top surface"*, Flore Boyer, as main author, says. *"However, helium pre-clean seems to induce less damage and no indium dots. We suggest that the difference in electrical behavior obtained between Ar and He pre-cleaned Ni/n-InP contacts is due to differences in the surface state and morphology."*

Digital Trust (Pulse)

Context and outlook

With the advent of the Internet of Things (IoT), new services based on data management are multiplying. The increase in the number of cyber-attacks is raising awareness among the public and institutions of the risks associated with a toot rapid and poorly controlled digital transition.

New vulnerabilities are being identified and revealed to the general public at a time when medical devices, automobiles, industrial and urban equipment are becoming increasingly connected and autonomous. These vulnerabilities and the attacks that exploit them are undermining the trust of the users in connected services and goods. Consequently, these attacks have an impact not only on the image of the companies, but also on the society's economy. They even sometimes compromise the legal and social liability of the public or private players who have inadequately protected their products.

However, when designing digital products, cybersecurity is often seen as a constraint which should not weigh too heavily on the primary function (health care, mobility, manufacturing, etc.), whether in terms of cost, performance, or ergonomics.

The challenge of the Nanoelec/Pulse program is thus to identify how electronic technologies can participate in the emergence of new products and services capable of increasing operating safety, protect the confidentiality, authenticity and integrity of digital data, guarantee protection of privacy, while simplifying the deployment of cybersecurity strategies. Our work focuses on three application areas: the security of industrial systems, that of robots and self-driving vehicles, and the Silver economy.

In its own way, the Pulse program aims to help meet the vital need from institutions, solutions suppliers and users, to live in a trusted digital world. ■

VINCENT CACHARD,
Director of the Pulse program and Manager of the Hardware security research department at CEA-Leti
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Pulse at a glance

👁 VISION

Due to the rise in cyber-crime, cybersecurity of the Internet of things (IoT) is a major challenge for digital trust. Strengthening and hardening critical embedded, increasingly interconnected and smarter systems is now vital.

⚒ AMBITION

New smart and intrinsically secure nanocomponents to reinforce systems resistance against future cyberattacks + Improved security of smart embedded systems throughout their life cycle (including AI algorithms) + Safer deployment environment through digital ID, data sovereignty and secure interactions between smart systems.

🎯 MISSION

Develop and test new security features for components and systems in three fields of application: Industry 4.0, Homecare and Robotics.

👥 PARTNERS

Akeoplus | CEA | Grenoble-INP | Inria | Schneider Electric | STMicroelectronics | UGA

HOMECARE CYBERSECURITY

Demonstrator for a first integration of Edge AI in a high-performance people-counting sensor

© Schneider Electric

Accurate occupancy data for smart building management

In November 2020, STMicroelectronics, Schneider Electric and Lynred presented the first integration of Edge AI in a high-performance people-counting sensor developed within Nanoelec.

While monitoring occupancy in large spaces with multiple entrances and exits is a significant challenge in any closed environment, it potentially offers significant value for hotels, offices, retail businesses and building managers. Three core partners of Nanoelec – STMicroelectronics, Schneider Electric, and Lynred – recently demonstrated a prototype of a high-performance people-counting sensor that overcomes the related challenges. This sensor provides the opportunity to use the data to optimize room occupancy, anticipate energy consumption, reduce waiting and queuing time, manage social distancing more efficiently, and more.

Since 2015, the Nanoelec/Pulse program partners have been working on attendance monitoring in public areas using digital devices. The 2020 demonstrator is the first device developed with Artificial Intelligence (AI) at the Edge. In the Nanoelec collaborative environment, STMicroelectronics, Schneider Electric and Lynred, with scientific and technological input from CEA, Inria and UGA, achieved a strong mix of hardware and software options coping with cybersecurity, reliability, and energy specifications. At the same time, Pulse/Nanoelec provided the technological platform to set up and test the different configurations of devices and algorithms to explore a range of suitable innovative solutions. ■

Open Innovation for smart cities and smart mobility

The startup Kentyou partnered with the Nanoelec/Pulse program to enhance its own development to provide a strong capacity to connect sensors, merge and mine data for smart cities.

"Given that sensor technologies are now affordable and widespread, city and building operators have to cope with the problem of extracting intelligent information from the deluge of data. They encounter difficulties with connecting sensors and merging data", explains Levent Gürgen. Levent Gürgen was a researcher at CEA and president of the Urban Technology Alliance (UTA)[1] before creating his own startup, Kentyou, in April 2020. *"Kentyou helps ci-ties and innovators exploit digital technologies and build smarter and more sustainable urban environments"*, adds Levent. Last year, the company partnered with the Nanoelec/Pulse program to enhance its own development to offer its customers the ability to connect sensors, and merge and mine data.

"Through Nanoelec, we had access to CEA's software platforms and skills, in order to implement the open source Sensinact[2] technology", adds Levent Gürgen. *"In addition, we recently benefited from the stimulating environment of the H2020 Large-Scale Pilot Activage project and took part in the experiments in its French node driven by Nanoelec/Pulse and also in 9 other European collaborative projects"*. As an IoT interoperability platform, Sensinact adopts a standard service-oriented approach to provide loose coupling between the physical and the virtual worlds, which brings the necessary flexibility for dealing with the dynamic and heterogeneous real world.

In 2020, the company has already hired 5 employees and has obtained a 400 k€ budget from the EU's H2020 program. Kentyou focuses on smart city services, although connected agriculture and Senior Care have been also investigated as market targets. *"As an example, we have started work with Chamrousse, a mountain resort in France, to provide optimization of skier flow and localization. We are also working with Santander, the well-known Spanish seaside resort & harbour. The idea is to enrich the tourist experience, manage car park capacity and provide the public with optimized advice for multimodal public transportation"*, adds Levent Gürgen. *"Our ambition is to reach 75 cities (of different sizes, French, European and beyond) that would use our platform within 5 years."* ■

[1] The Urban Technology Alliance (UTA) is a global non-profit organization providing city-scale testbeds from all around the world, to deploy, test and validate the latest smart city innovations – http://www.urbantechnologyalliance.org/
[2] https://projects.eclipse.org/proposals/eclipse-sensinact

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Facilitating the reception of deaf and hearing-impaired students

UGA and CEA-Leti, working together within Nanoelec, develop a tabletop interface to enhance and facilitate the reception of deaf and hearing-impaired persons.

Samba is a hardware and software device providing a real-time speech-to-text solution to improve the quality of services to deaf and hearing-impaired persons. Developed by Université Grenoble-Alpes (UGA) and CEA-Leti under the Nanoelec/Pulse program, with a grant from the UGA Idex, Samba was recently improved based on feedback from field-testing with end-users: with its two 10-inch back–to-back displays, the tabletop system is more compact. It now "speaks" five languages and offers new functionalities, like verbatim mailing, to address a wider audience.

At the UGA reception office for disabled students, the hardware and software solution helps staff better serve deaf and hearing-impaired persons: a real-time speech-to-text solution enabling the students to interact via the desktop interface with the impression that they are simply reading subtitles.

The beta version of the solution consisted of a modular unit that housed two displays and a computer. After two rounds of field-testing at the university's disability services, several improvements were made in particular with the expertise of the AGEIS laboratory.

Specifically, feedback from end-users (hosts and disabled students) indicated that the system would better meet their needs if it was smaller. In research conducted under the Nanoelec/Pulse program, the joint AGEIS (UGA) and Y.Spot (CEA Tech) teams used an iterative and incremental development approach to come up with a direction-adjustable unit that houses two 10-inch horizontal displays mounted back-to-back instead of the 15-inch vertical displays used in the first prototype. When placed between the student and the university staff member, the new, more compact desktop version does not prevent the student from going back and forth between the text on the screen and the speaker's face.

A design-to-cost approach has been used to reduce the number of components and simplify the assembly process for future commercialization. In addition to making the final product more affordable, this should also facilitate assembly by disabled workers, another of the project's goals as part of an inclusive approach. The new prototype has a strong visual identity, with an easy-to-identify logo and original surface texturing. The software and interface were also improved based on feedback from the first round of user testing. Ultimately, real-time machine translation will be added to the system, potentially broadening Samba's target market. ■

The new Samba compact solution for deaf and hearing-impaired persons is developed at CEA and UGA under the Nanoelec/Pulse program

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Nanoelec's Products & Technologies Living-lab at CEA-Leti.

This R&D platform helps pioneer new technologies with applications in connected mobility, in-home healthcare and other home services. The goal is to support companies in their development of innovative and secure products and services.

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Are you washing your hands the right way?

Nanoelec is participating in improving SureWash, a device to monitor the quality of handwashing in hospitals, schools, public restrooms and restaurant kitchens.

The SureWash device is the very first system capable of monitoring both the quality and the frequency of hand hygiene in real-time. It has been improved by CEA-Leti, within Nanoelec. SureWash is the very first system capable of monitoring both the quality and frequency of hand hygiene in real-time. Providing special training to improve hygiene practices, the product is designed for installation above sinks (hospitals, schools, public restrooms, restaurant kitchens, etc.).

Under the European FED4SAE program, Glanta, an Irish Company, asked Nanoelec and CEA-Leti to help

them improve SureWash from a design-to-cost perspective. CEA-Leti's researchers successfully achieved both software and hardware integration, leveraging Nanoelec's Products & Technologies Living-lab. Based in Grenoble, France, and operated by Nanoelec, this R&D platform helps pioneer new technologies with applications in connected mobility, in-home healthcare and other home services. The goal is to support companies in their development of innovative and secure products and services.

Various functional tests of SureWash have been conducted, namely (i) installation of the hardware device on-site, (ii) recognition of hand gestures in accordance with the United Nations World Health Organization (WHO) recommendations, (iii) feedback from monitoring provided to the users, (iv) cybersecurity aspects. SureWash units use cutting-edge computer vision technology to build hand hygiene muscle memory by giving real-time

feedback to learners. The latest version of the device performs automatic video auditing (AVA) of hand hygiene. AVA is placed over sinks and measures and quantifies the level of hand hygiene. In the event of poor washing practices, SureWash provides real-time training on the spot.

"The video images never leave the device making them GDPR compliant. The devices were used in a clinical trial in the UK's National Health Service (NHS) and it increased the quality of hand hygiene by 197% and the number of hand wash events by 147%", said Gerard Lacey, CTO and cofounder of Glanta, who published these results in the American Journal of Infection Control in February 2020.

Founded in 2011, Glanta has been pioneering new techniques in gesture recognition and augmented reality since its inception. Above all, Glanta's mission is to deliver working applications for camera-based algorithms. ■

Data to preserve the autonomy of seniors

Since 2015, the startup Cocoon Care has been carrying out research work under Nanoelec's Pulse program. This work has led to the marketing of a fall detection system (made of new-generation sensors and a monitoring platform). This is only the first step in the implementation of a broader prevention and prediction system for connected health, which aims to help elderly people who stay home, as well as support caregivers.

In both Europe and France, seniors nowadays account for a fifth of the population[1]. Moreover, the proportion of the elderly is tending to grow worldwide[2], along with the need for more assistance and skilled people to maximize autonomy and ensure the best quality of life for everyone. Therefore, in France, 15,000 workers and 3.9 million relatives are mobilized to help elderly and dependent people[3].

To meet these needs, Valentino Marra and Laurent Adde co-founded Cocoon Care on February 28, 2020. The startup has already hired six employees and raised funds from a major player on the CAC40 index. Based on results from research work that Nanoelec partners have been carrying out since 2015, Cocoon Care plans to consolidate its smart home offering adapted to elderly people losing their autonomy. It aims to protect their safety, reinforce their autonomy, improve their comfort and support & ease the workload on relatives and caregivers.

The startup benefits from the professional and technical expertise of UGA and CEA researchers as well as access to Nanoelec's experimentation platform to evaluate and validate its solutions in realistic conditions – before a first field deployment and market launch – but also to develop its ability to innovate. *"The technology that Cocoon Care has industrialized was evaluated several times in 2020 through Nanoelec's Products & Technologies Living-lab (PTL) following strict and proven scientific protocols. This platform reproduces the living conditions of elderly people in a realistic environment, especially through a full-scale instrumented replica of a nursing home/hospital room. Functional integration tests have demonstrated the compatibility between Cocoon Care's solution and the Schneider Electric building management system"*, underlines Christophe Villemazet (CEA), De-

[1] Eurostat & Insee

[2] In 2020, the world has nearly one billion people aged 60 and over. During the first half of the 21st century, the aging of the population will continue gradually, and the number of those aged 60 or over is expected to reach 2 billion by 2050. (Global AgeWatch 2018: http://globalagewatch.org/reports/global- agewatch-insights-2018-report-summary-and-country-profiles /)

[3] Source: DREES, Capacités, Aides et Ressources des seniors (CARE) -Ménages 2015 and CARE-Institutions 2016 surveys

To consolidate its home automation offering dedicated to elderly people with loss of autonomy, Cocoon Care uses the Nanoelec Products & Technologies Living-lab (PTL). The startup can thus test the implementation of its solutions and test their reliability and security in realistic conditions of use. Here, mounting of a bed presence detection device on the "testbed" placed in an instrumented replica of a nursing home room.

© P. Jayet/CEA

puty Director of the Nanoelec/Pulse program.

Cocoon Care intends to stand out through the reliability and performance of its sensors, and by hosting data on HDS[4] servers: the Silver Economy technology market is *"tired of low value-added solutions, or even gadgets, with little value or low reliability,* according to Laurent Adde, the company's Managing Director. *However, thanks to the technological readiness level, along with human assistance provided by the caregivers, it is possible to concre-* tely safeguard and improve the autonomy and quality of life of elderly people, as well as of their families and caregivers."

"We are starting to market an offering for the B2B market based on fall detection, which accounts for 9,000 deaths every year in France[5]", adds Valentino Marra, CEO of Cocoon Care. There is an urgent need as current devices detect 30% to 50% of the falls in the best case, and the human and economic stakes are significant. The startup's first targets are the health and me- dico-social sector stakeholders such as nursing homes, hospitals, senior residences/villages, as well as telecare providers.

"As early as next year, we will also be addressing the consumer (B2C market) directly with an adapted offering. Our market expectations are significant as we will face a 55% growth in the senior population worldwide in the next ten years, reaching 1.5 billion people in 2050[6]", Valentino Marra adds. ■

[4] Computer services specifically officially approved for the storage of health data

[5] According to the WHO, more than 37 million serious falls require medical care, and 646,000 people die, including more than 9,000 in France, (Public Health France)

[6] World population aging 2019. Highlights. New York, United Nations, Department of Economic and Social Affairs, 2019 (ST / ESA / SER.A / 430) (https://www.un.org/en/development/desa/population/publications/pdf/ aging / WorldPopulationAgeing2019-Highlights.pdf)

CYBERSECURITY OF INDUSTRIAL SYSTEMS

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Hardware-in-the-loop platform for cybersecurity

"The WonderICS platform was installed within Nanoelec at CEA at the end of 2020. This hardware-software co-simulation environment aims to alert the public and professionals to the cybersecurity threat of industrial control systems and experiment with innovative security solutions. In WonderICS, we have integrated simulators to emulate physical processes for different use cases such as hazardous gas management or hydroelectric power plants." explains Pierre-Henri Thevenon, cybersecurity engineer at CEA who coordinated the design of WonderICS. *"A set of tools can be used to attack industrial control systems in different ways (phishing mails, corrupted USB key, hardware trojan, etc.). Fortunately, we also demonstrate organizational and technical solutions that would have prevented this type of attack"*, he adds. ◼

SAFETY OF INDUSTRIAL SYSTEMS

IoT and security: Reliable, wireless industrial systems

CEA-Leti and Davey Bickford Enaex, collaborating within Nanoelec, unveiled in May 2020, the demonstrator of a new wireless system, that offers increased safety, flexibility and productivity gains to the blasting market.
In November 2020, the two partners extended their joint laboratory for three years to continue the development of innovative radio-frequency communication systems that remotely control networks of high-tech wireless electronic detonators. The joint lab will build on the partners' recent success in developing an electronic initiation system without using surface wire. Like the previous partnership, the ongoing work will take place within Nanoelec. ■

© Davey-Bickford

Open hardware for innovation in electronics

At the end of March 2021, France organized the third international meeting for the Risc-V worldwide community. Some of the teams contributing to the Nanoelec programs are increasingly involved in worldwide collaborations on open standards for processor innovations. Nanoelec provided extensive support for the "Risc-V week" workshop and CEA, member of the Risc-V International Association, joined the Open Hardware Group in 2021.

> ❝ *4 questions to Fabien Clermidy, Head of the Computing Department at CEA List & CEA representative in the OpenHW Group.*

What is Nanoelec's interest in focusing on open hardware and software for innovative architecture?

Innovation is required to maintain the environmental sustainability of digitalization and the trend towards electronic devices everywhere. The challenge to be met is to enable the design of specialized integrated devices and embedded systems that are energy-frugal while keeping control of development costs and time.

Open Hardware enabled by Risc-V ISA and Open Software such as Linux are creating common homegrounds and strong references for a number of dedicated markets, facilitating collaborations through which real innovations can be developed and accurately evaluated. They are powerful enablers for Nanoelec.

Risc-V is presented as "paving the way for the next 50 years of computing design and innovation". What are the expected breakthroughs?

One of the breakthroughs enabled by Risc-V Open ISA and Open Hardware as a whole is the ability to design specialized High Performance Computing Sytems on Chip (SoCs) that are "Correct by construction", "Secure by design" and/or "trustworthy".

Risc-V facilitates more transverse innovation at the SoC or platform level. This will have a strong impact on low-power consumption and the quest for security for instance, two areas that essentially require cross-disciplinary approaches (analog design, digital design, software). Open-source hardware and especially Risc-V opens up a whole field of innovation: e.g. computing cores, micro-architecture, integration with caches and memory hierarchy, and accelerators.

Despite the end of Moore's Law, computing power increase can be achieved through accelerators co-designed to serve the requirements of a given business software stack. Finally, it will lead to de-facto standards that will facilitate implementations by various players who

Risc-V week

Held on-line by Nanoelec, Inria and CEA, the "Risc-V week" (Mar. 30 to Ap. 1, 2021) underlined the benefits of hardware and software co-design and open source collaboration.

In addition to 20 technical presentations, the event received significant contributions from prominent personalities of our community, such as Prof. Gernot Heiser (UNSW Sidney), Prof. Luca Benini (ETHZ & Univ. Bologna), PhD Rishiyur S. Nikhil (Bluespec), PhD Gabriel L. Somlo (CERT/SEI, CMU) and Dominic Rizzo (Google). Close to 400 scientists from 33 countries (mainly Europe, India and Brazil) attended the various sessions.

have their independence of action at heart.

This will have a strong impact on computing and embedded systems where specialization is paramount, such as embedded perception, AI for autonomous vehicles, cloud computing, and HPC.

Will participating in Open Hardware Group task forces also increase Nanoelec's capacity and skills for designing new kinds of processors, systems and tools?

In 2020, CEA, within IRT Nanoelec, renewed its membership of Risc-V International, a Zürich-based foundation that drives collaboration around Risc-V ISA (Instruction Set Architectures) specifications. Joining the OpenHW Group, a forum dedicated to cooperation on the development of open-source cores, tools and software, allows us to go forward and collaborate on actual implementations.

The challenges of hardware design include the costs and time required for the last stages of IP verification. It is important to catch bugs ear-ly on to reduce verification costs, and improve time-to-market. The openness of Risc-V ISA allows collaboration on verification tools, e.g. for ISA implementations. Open collaboration, massive reuse and sharing will quickly improve the maturity of these IPs and tools.

The same kind of virtuous circle will come for other SoC technologies that will be open sourced, e.g. NoC, cache coherency, virtual memory, vector processing, or specialized processors based on Risc-V ISA extensions and accelerators.

The OpenHW Group, as a not-for-profit global organization, is also a tremendous opportunity to present our contributions to potential partners on the global market.

At the end of March 2021, France organized the third international meeting for the Risc-V worldwide community. What was the purpose of the meeting?

The proprietary nature of previous ISA left few, if any possibilities for collaboration between hardware and software research communi-ties. With the advent of Risc-V and open source hardware, it is important to bring these two communities together in order to co-optimize at the system level and fully realize the benefits of open source hardware and software. We can see the benefits of this approach in our own developments for security for IoT and variable precision floating-point in numerical computing. ◼

FABIEN CLERMIDY,
Head of the Computing Department
at CEA List & CEA representative
in the OpenHW Group
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White Book

With IRT Nanoelec and Thales, the French Ministry for the Interior publishes a white paper on the contribution of Blockchain technology to the deployment, increased reliability and protection of digital identity.

Digital identity lies at the heart of the challenges of the digital economy: storing, processing and using users' personal data is one of the bases of the business model of the digital giants. However, for the time being, the existing identity ecosystems are relatively incompatible with new challenges such as privacy protection (GDPR), compliance with new anti-fraud regulations, or identity theft prevention.

The concept of Self Sovereign Identity (SSI) is one possible avenue for addressing these challenges. "Supported by an intrinsically secure Blockchain, it allows people to own and control the digitization of their identity without intervention of a centralizing organization", state the authors of a white paper entitled "Blockchain and digital identification", published by the Ministry for the Interior, with IRT Nanoelec and Thales in May 2020. ■

The Inria-Chroma instrumented car dedicated, within Nanoelec, to collision risk developments in autonomous driving
© P.Jayet/CEA

Autonomous vehicle security

In the race engaged by all car manufacturers, autonomous solutions have entered an acute phase of technological progress. The goal of the Autonomous Vehicle Security (AVS) project carried out under Nanoelec/Pulse program is to develop, integrate and promote core technologies for context capture in order to enhance the vehicles security. *"Based on Bayesian fusion and filtering technologies, these bricks allow the vehicles to move safely by providing an enriched representation useful for the autonomy functions"*, as explains Lukas Rummelhard (Inria), AVS project leader at Nanoelec. *"In 2020, the quality and scope of the demonstrations of autonomous driving functionalities were enhanced. The work mainly focused on vehicle localization, path planning and following systems, and on the development of a path-planning method specifically adapted to Bayesian occupancy grids."*

All these developments were the core subject of a test campaign, unprecedented for the team, on a dedicated circuit (Transpolis). Hundreds of tests on the perception systems and low-level control mechanisms were performed and large volumes of data collected during this four-day experimental session. Another focus of the work has been on the embedding of the developed technologies. Context capture technologies must be able to operate with low cost and low power sensors whether it is for automation of light vehicles or integration of perception capabilities on infrastructures. Systems have to be compatible with an integration on small, lightweight, low-power computing devices.

As part of Nanoelec, Inria is also working on the validation of artificial intelligence (AI) systems for mobility. The question of the evaluation and validation of the effectiveness of these technologies remains one of the key issues preventing the deployment of embedded context capture technologies and therefore a major challenge for autonomous vehicle projects. ■

WORKSHOPS & CONFERENCES

CYBERSECURITY AWARENESS WEEK

Nanoelec supported the 17th Cybersecurity awareness week sponsored in Europe by the Grenoble-INP/Esisar engineer school.

Almost a thousand users have registered on the on-line conferencing website of CSAW 2020 in Europe. CSAW is the most comprehensive student-run cyber-security event in the world, featuring 10 hacking competitions, workshops, and industry events. Final events are hosted by six global academic centers, including, in Europe, Grenoble-INP/Esisar, a core partner of Nanoelec. The world finals brought together 377 participants - 100 of them coming from Europe for 3 challenges: applied research, embedded security challenge & capture the flag). *"Interest in cybersecurity is not waning*, David Hely (Grenoble-INP/Esisar) comments. *Students are very sensitive to cybersecurity issues and they are going down this route in increasing numbers."*

CYBERSECURITY: DEMONSTRATOR FOR INDUSTRY AWARENESS

Nanoelec teams presented their latest developments in industrial IoT Security at the International Cybersecurity Forum (January 2020, France).

A platform has been developed to raise awareness of vulnerabilities, cyberattack risks and the challenges of cybersecurity for industry. It can be used to demonstrate cybersecurity for industrial and tertiary systems used by stakeholders in the field (energy, essential operators, etc.).

Engineers at Nanoelec are able to offer solutions based on technological developments in 'security by design'. *"Our demonstrator implements the digital twin of an electrical transformer. We can also simulate attacks on an industrial network, propose hardware countermeasures for securing the network and deploy security settings from a connected tablet"*, explains Pierre-Henri Thevenon, project manager at CEA-Leti.

International Cybersecurity Forum (January 2020, France)
©DR

REGIONAL ECOSYSTEM FOR ACTIVE AND HEALTHY AGEING

The Nanoelec experts involved in the European Activage project,

took part in a seminar on November 5, 2020 intended for senior care professionals in the Grenoble-Alpes municipality. It was entitled "From product to ecosystem: Round-up & prospects regarding innovations for ageing well." This third annual event was an opportunity to review projects, offerings and services. The next edition will take place in November 2021 addressing the themes of artificial intelligence and cybersecurity for the home care service for the elderly.

Key publications

Preventing Collision Risk in Autonomous Driving

A crucial aspect that automotive systems need to face before being used in everyday life is the validation of their components. To this end, standard exhaustive methods are inappropriate for validating the probabilistic algorithms widely used in this field and new solutions must be adopted. In a paper at IV2020, scientists from Inria-Chroma, participating in Nanoelec, and Louvain Catholic University, presented an approach based on Statistical Model Checking (SMC) to validate the collision risk assessment generated by a probabilistic perception system. Exhaustive verification and evaluation were carried out on a large number of simulated scenarios. The simulation results were compared to real-life experiments using Nanoelec/Inria's autonomous car by reproducing a scenario

in which the car collides with a pedestrian (dummy) crossing the street.

ANSHUL PAIGWAR & AL.
Probabilistic Collision Risk Estimation for Autonomous Driving: Validation via Statistical Model Checking
Presented at IV 2020
31st IEEE Intelligent Vehicles Symposium

Deception strategy for cybersecurity

A joint team from CEA and Mines Saint-Etienne is paving the way for a new approach to defend a distant system against malicious attacks, in which

traps are set for the attacker. *"We explain the basics of our defense by the principle of the luring effect, inspired by the notion of robust and non-robust features, and experimentally justify its validity"*, Rémi Bernhard says, as first author of the review paper accepted at the IJCNN 21 conference. *"We propose a new approach to improve the robustness of a distant model against malicious attacks, inspired by the notion of robust and non-robust features. Our method is conceptually innovative as it exploits a new way of defending a distant system: presenting the adversary with various features that are less robust than those of the target model. Technically, it requires no retraining of the model, nor makes assumptions about the way malicious attacks are designed, nor relies on expensive test-time inference procedures."*

RÉMI BERNHARD & AL.
Luring Transferable Adversarial Perturbations for Deep Neural Networks

IJCNN 2021 (International Joint Conference on Neural Networks 2021)
http://arxiv.org/abs/2004.04919

A scalable deep learning toolkit for medical imaging segmentation

Deep learning has gained significant popularity in recent years thanks to its tremendous success across a wide range of relevant fields of applications, including medical image analysis in particular. Although convolutional neural network (CNN) based medical applications have been providing powerful solutions and revolutionizing medicine, efficiently training CNN models is a time-consuming and challenging task. It is a computationally intensive process taking a long time and occupying scarce system resources, which represents a significant obstacle to the progress of scientific research. To address this challenge, Soulaimane Guedria and colleagues (Université Grenoble Alpes, AGEIS & LIG, within Nanoelec) report in an original paper on a scalable intuitive deep learning toolkit for medical imaging semantic segmentation. *"R2D2 not only offers empirical evidence and in-depth investigation of the latest published works but it also facilitates and significantly reduces the effort required by researchers to quickly prototype and easily discover cutting-edge CNN configurations and architectures"*, comments Soulai-

mane Guedria as first author of the paper.

SOULAIMANE GUEDRIA & AL.
(Université Grenoble Alpes, AGEIS & LIG)
R2D2: A scalable deep learning toolkit for medical imaging segmentation
Journal of software: Practice and Experience
doi.org/10.1002/spe.2878

Protecting code and data in embedded processors

A study on protection against attacks to keep user data secret and safe. "Computing devices have become a part of our daily *world. Being physically accessible, they are exposed to a very wide range of physical attacks, which most of the time are underestimated"*, says Olivier Savry (CEA-Leti). These systems must include protection against these attacks in order to keep user data secret and safe. In a paper presented at the DSD Conference 2020, Olivier Savry and two of his colleagues working within Nanoelec, propose a new, efficient and flexible memory encryption & authentication mechanism that can protect code and data in embedded processors. "This new countermeasure is developed on a modified *Riscy Risc-V core and its performance is evaluated on an FPGA target"*, states Olivier Savry. "Thus, we showed a new way to deal with the stack of *countermeasures thanks to authenticated encryption of both code and data to guarantee confidentiality and integrity at runtime, protection against code reuse attacks and stack overflows."*

OLIVIER SAVRY & AL.
Confidaent: Control FLow protection with Instruction and Data Authenticated Encryption

2020 23rd Euromicro Conference on Digital System Design (DSD)
10.1109/DSD51259.2020.00048

Is the blockchain a relevant technology for industry 4.0?

For Industry 4.0 use-cases, involving several stakeholders of a value chain around connected and autonomous smart robots, the Ethereum

Blockchain appears to be a technology with high potential. However, the use of digital certificates from a public key infrastructure (PKI) also requires compatibility with a more mature technology. Christine Hennebert and Florian Barrois, cyber experts at CEA-Leti, explore the advantages of each of these technologies and show that they could complement each other advantageously. *"Blockchain strengthens trust between independent actors, around cybersecure embedded smart robots distributed in a factory, enabling business development and transparent traceability of activities"*, concludes Christine Hennebert in the paper presented at Brains'20 last September.

CHRISTINE HENNEBERT & AL.

Is the blockchain a relevant technology for industry 4.0?

2nd conference on Blockchain Research & Applications for Innovative Networks and Services, BRAINS 2020

Security for connected objects throughout their lifecycle

For his doctoral thesis at CEA-Leti within Nanoelec, Johan Marconot looked at the design of solutions to provide security for and guarantee the operational integrity of connected objects throughout their lifecycle.

"The greater diversity of IoT technologies and players limits generic security solutions. The protection systems should not be a burden on the resources and the ease of use of the devices. Moreover, during their lifecycle, IoT objects have specific security needs", he explains in the introduction to his thesis. His research has made two contributions: formalization of the security requirements for the lifecycle of cyber-physical systems and the proposal of a new extraction model for PUF (Physical Unclonable Functions), for which the logical principle is based on Substitution-Permutation-Networks (SPN).

JOHAN MARCONOT

Physical Unclonable Functions for Security of lifecycle of a cyber-physical object

Thesis defended on July, 9th, 2020 at Grenoble-Alpes University in collaboration with CEA-Leti and Nanoelec

A deep learning parallelism platform for medical imaging applications

Deep neural networks (DNNs) and in particular convolutional neural networks (CNNs) trained on large datasets are achieving considerable success across a wide range of paramount applications. They have brought powerful solutions and revolutionized medicine, particularly in the medical imaging analysis field. *"However, deep learning implies multiple challenges"*, says Soulaimane Guedria, in his PhD thesis prepared within Nanoelec. *The CNN training phase is a computationally intensive and time-consuming task. Furthermore, introducing parallelism to CNN is a tedious, repetitive and error-prone process. In addition, there is currently no broad study of the generalizability and reproducibility of the CNN parallelism techniques in concrete medical imaging segmentation applications."* Within this context, Soulaimane Guedria reports on the design, implementation and validation of an all-in-one scalable and component-based deep learning parallelism platform for medical imaging segmentation.

SOULAIMANE GUEDRIA

A scalable and component-based deep learning parallelism platform: application to convolutional neural networks for medical imaging segmentation.

Thesis defended on July 8th, 2020 at the University Grenoble-Alpes in collaboration with LIG and Nanoelec

Energy Conversion (PowerGan)

Context and outlook

From smartphones to kitchen appliances and e-vehicles, electric current and voltage must both be processed and controlled with the help of a converter to supply the optimal energy required by each specific device. Power conversion, however, leads to energy loss. Gallium nitride (GaN) and other wide-bandgap materials can substantially reduce this loss. Until recently, these technologies were too costly to use in power conversion applications. But driven by the aeronautics and automotive industries in their quest for highly compact and efficient power converters at low cost, R&D centers are now pioneering new GaN techniques.

The aim of the Nanoelec/Powergan program is to strengthen and structure a national industrial and academic ecosystem to help stakeholders from French and European industry gain a foothold in a variety of sectors, ranging from personal electronic equipment to electrification of private and mass transport. Teams brought together through the program are contributing to the development of GaN-on-silicon (GaN/Si) technologies in order to overcome the technical and economic limitations of current power-component technologies available in silicon and gallium nitride for the 100-650 V segment. Launched in 2017 and directed by Philippe Pantigny until November 2020, the program is based on a disruptive technology using 200 mm wafers compatible with mass production. This technology transfer is at the heart of the GaN/Si pilot line that STMicroelectronics is implementing in its factory in Tours, France. We are improving the performance and reliability of a first generation of 650 V components and preparing for the next generations. In order to further drive the miniaturization of systems, we are working on the architectures of disruptive converters. We are also developing tools and methods to co-design component and system architectures to accelerate technological adoption, especially for harsh environments such as automotive applications.

GaN power devices may be just around the corner. However this achievement requires more R&D efforts. Each architecture has its own potential, depending on the application targeted. Academic and industrial teams brought together within Nanoelec continue to explore various architectures in order to address the great need for efficiency at low cost, and, perhaps more importantly, the need for greener power electronics. ■

RAPHAEL SALOT,
Nanoelec/Powergan
Director & Key Account
Manager at CEA
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PowerGan
at a glance

👁 VISION

Support and accelerate the development of a new generation of power components to address digital and energy transition challenges.

📐 AMBITION

Contribute to the structuring of the national GaN value chain with a research strategy based on disruptive GaN/Si power devices using 200 mm technology and GaN enabled power converters co-design tools and techniques.

🎯 MISSION

Prepare 650 V transistor technology transfer to STMicroelectronics and establish proof of concept for a PowerGan Digital Twin.

👥 PARTNERS

CEA | Grenoble-INP | Schneider Electric | Siemens EDA | STMicroelectronics

TOWARDS
A DIGITAL TWIN

One of the scientific and technological challenges of the Nanoelec/PowerGan program is centered on the modelling of power components (via the 650V transistor compact model study).

The digital twin concept consists in replicating a physical system in a digital model operating *in silico*. This type of approach is developed by Nanoelec for GaN power components and it allows co-optimization of the system and the technology and drive them to the performance limits.

As a founding member of the institute since 2012, Siemens EDA (ex. Mentor Graphics) has been closely involved in the 3D and photonics programs. In 2020, the company joined the Nanoelec/Powergan program.

"We bring to the program the capacity to build a Digital Twin of GaN power converters, enabling system and technology co-optimization, testing of accuracy against measurements and using it throughout its full life cycle, as well as getting ready to respond to the acceleration of the market", explained Jean-Marc Talbot, Senior Director Solutions & Strategic Partnerships at Siemens EDA. ■

POWER SWITCHES

As part of Nanoelec, the CEA is jointly developing atomic scale resolution plasma etch processes for GaN and related materials with Lam Research, a leading US supplier of semiconductor processing equipment.

These solutions are a key building block in the fabrication of GaN based power devices. *"In 2020, studies were carried out on the characterization of Lam's ALE (atomic layer etching) process recipes as well as on the interaction of these steps with other processes in the device fabrication flow. A reduction in the defects associated with etching and a positive impact on ohmic resistance were observed. This ultimately benefits device performance for advanced power management applications. This critical work carried out by Nanoelec has made a significant contribution to our understanding and capabilities in this important area of power electronics"*, explains Dr David Haynes, Head of Specialty Technologies Strategy at Lam Research. ■

CONTRIBUTION TO STANDARDS

The community of GaN power electronics development players considers that the technologies are now mature enough to standardize components characterisation techniques used to edit the product technical data sheets.

In response to this need, a working group of the JEDEC[1], including Nanoelec contributors, published standard JEDEC JEP180 in 2020: It is a "Guideline for Switching Reliability Evaluation Procedures for Gallium Nitride Power Conversion Devices" providing all players along the value chain with a qualification reference baseline appropriate to the physics of GaN components, thus overcoming the limitations of GaN technology qualification using standards based on the physics of silicon components. ■

[1] JEDEC is the global leader in developing open standards for the microelectronics industry, with more than 3,000 volunteers representing over 300 member companies.

At G2ELab, Pawel Derkacz, PhD student (UGA and Gdansk University, Poland) developed an electromagnetic interference measurement bench for Nanoelec/Powergan power boards

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Key publications

High performance transistors

Currently, GaN devices typically use a hetero-structure, with an AlGaN barrier layer grown on the top of GaN buffer layers. However, due to the difference in lattice parameter between these two materials, the device performance and reliability can be limited. *"In order to further improve the devices, in terms of performance and reliability, CEA teams have started to develop new barrier materials based on InAlN, which has the same lattice parameter as GaN when grown with 18% of In",* says Mrad Mrad, introducing his PhD thesis. *"My work is a continuation of these initial developments, with the intention of adapting and developing these layers for specific applications, including the growth of quaternary films composed of InGaAlN."*

MRAD MRAD
Epitaxy of quaternary InGaAlN layers for high performance transistors

Thesis defended on July 7th 2020 at Grenoble-Alpes University in collaboration with CEA-Leti.

Towards the 2nd generation of GaN power diodes

In lateral power diodes, the conductivity modulation mechanism can pave the way for the demonstration of surge current capability. In a Hybrid Anode Diode concept with a p-GaN layer, an anode contact on p-GaN layer can be a source of hole injection that increases the electron density at the AlGaN/GaN interface. In a paper presented at the International Conference on Simulation of Semiconductor Processes and Devices (SISPAD2020, digital), CEA-Leti authors presented the study they ran within Nanoelec.

"The role of the p-GaN layer on the surge current capability explains the role of hole barrier tunneling at the anode metal/p-GaN interface. We demonstrated that use of high Mg concentrations in the p-GaN layer for HADs provides lower turn-on voltage owing to conductivity modulation. The findings obtained in our work can

pave the way for the use of conductivity modulation to obtain surge current capability in lateral power diodes", states Marie-Anne Jaud (CEA-Leti) as a corresponding author of the paper.

GÖKHAN ATMACA & AL.
Surge Current Capability in lateral AlGaN/GaN Hybrid Anode Diodes with p-GaN/Schottky Anode

2020 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)

Advanced GaN devices embedding a MOS gate

In papers presented at IEDM 2020, scientists from Université Grenoble-Alpes, CEA-Leti and STMicroelectronics gathered in the Nanoelec/Powergan program and colleagues of University of Padova (Italy) recounted experiments with variations of high-electron-mobility transistors (HEMT) based on gallium nitride-on-silicon. GaN-based semiconductors improve both performance and reliability of increasingly compact power converters compared to silicon, and AlGaN/GaN HEMTs have shown potential to replace power-conversion solutions based on Si or SiC for high-frequency applications with high power and low noise. This technology is therefore expected to be a cost-effective, power-conversion solution for many end-user applications, ranging from smartphones to kitchen appliances and e-vehicles and from battery loaders to DC/DC or AC/DC converters.

Considered together, the two papers provide a novel understanding of the gate stack of the GaN MOS-c HEMT developed at CEA-Leti in the IRT Nanoelec framework. They demonstrate the complexity of GaN MOS stack characterization as well as the requirement for deep expertise to report and analyze reliable parameter values. The work presented in these papers will also help to solve detrimental effects occurring in GaN devices to improve reliability.

"We showed that the instabilities of voltage threshold (Vth) under positive gate stress were caused by two populations of traps," said Aby-Gaël Viey, an author of

the papers. "In addition, our more recent work demonstrated that it is possible to accurately model and predict these threshold voltage instabilities with great precision. Indeed, the known model of capture emission time (CET) maps were used to confirm the presence of the two populations of traps and predict pBTI degradation (Vth shift) under a certain gate/temperature stress condition."

ABYGAËL VIEY & AL.
Carbon-related pBTI degradation mechanisms in GaN-on-Si E-mode MOSc-HEMT

WILLIAM VANDENDAELE & AL.
Novel Insight on Interface Traps Density (Dit) Extraction in GaN-on-Si MOS-c HEMTs

IEDM 2020 Conference

A model for calculating switching and conduction losses

Gallium nitride (GaN) transistors have demonstrated their potential as a high switching frequency, high power density, and high-efficiency power device. Substantial research has been undertaken on the switching and conduction losses calculation, using an analytical approach. A team from G2Elab (UGA, France) and Sharif Univ. of Technology (Iran) presented an interpolation-based method to calculate switching and conduction losses at the IECON 20 conference.

"This interpolation method employs a combination of the GaN transistor and driving parameters such as parasitic capacitances, parasitic inductances, gate resistors, drain-to-source voltage, instantaneous current, and temperature. A value for switching loss is considered as a base value and the different combinations of circuits will be reached by using interpolated equations", explains Moshen Rezayati, PhD student at Sharif University and G2ELab.

The study also investigates the temperature-dependency of the ON state resistance and finally, the accuracy of the proposed model is validated by using a number of scenarios on LTSPICE simulations. *"The proposed model enables simple, rapid, and remarkably accurate estimation of switching losses and conduction losses and can be used in the optimization process wi-*

thout any time domain simulation for switching and conduction losses", Rezayati adds.

MOHSEN REZAYATI & AL.
Interpolation-Based Switching and Conduction Losses Model of GaN Transistors

IECON 2020, the 46th Annual Conference of the IEEE Industrial Electronics Society

High-speed switch

The 22nd European Conference on Power Electronics and Applications was held in digital format in September 2020. Thilini Wickramasinghe (Lyon University) presented a paper on the electrical property variability of GaN transistors in parallel and their impact on fast switching operations. Sponsored by Laboratoire Ampere (Insa Lyon) and CEA-Leti, the study aims to identify the acceptable dispersion range of the electrical properties of transistors in parallel in order to obtain a stress-free switching operation targeting medium power (1-3 kW) applications. In this study, both board parasitics and device electrical parameter discrepancies were investigated.

"We used 650 V GaN devices with two different gate types (p-gate and MIS-recess gate) in different packagings for the experimental study. It was found that the variation of the threshold voltage can make a high current imbalance during on-transitions while the on-resistance in steady-state has less impact. However, the routing parasitic components in a very high-frequency range have a significant influence on current unbalances among the devices as compared with the device parameter discrepancy range in the sample. This again proved that the GaN transistor-based designs are appropriate for circuit integrations", Wickramasinghe says.

THILINI WICKRAMASINGHE & AL.
Electrical property variability of GaN transistors in parallel and their impact on fast switching operations

EPE'20 ECCE Europe,
22nd European Conference on Power Electronics and Applications

3D architecture for power electronics

At EPE'20, authors from CNRS, Grenoble-INP (UGA), G2ELab, ENS Cachan and Gdansk University (Poland) presented a paper on the adaptation of a 3D integration concept, previously used with vertical devices, to lateral GaN devices.

"This 3D integration reduces loop inductance, to ensure a more symmetrical design with significantly reduced Common Mode emission, thanks to low middle point stray capacitance. This reduction has been achieved both by working on the power layout and by including a specific shield between the devices and the heatsink", underlines Pawel Derkacz, first author of the paper. *"Superior performance of the 3D layout is expected when looking at the simulation results"*, says Derkacz, PhD student at G2ELab (Grenoble-INP) and Gdansk University.

PAWEL DERKACZ & AL.
**3D PCB package for GaN inverter leg
with low EMC feature**

EPE'20 ECCE Europe,
22nd European Conference on Power Electronics
and Applications

Full 3D advanced packaging

The results of the Nanoelec/PowerGan program were presented by G2ELab, as part of a summary of 3D integration in power electronics, during an "Industrial Applications" session organized by PSMA (Power Sources Manufacturers Association), during APEC 2020.

The audience consisted of academic and industrial researchers. Apec is the largest international power electronics conference. PSMA selected this G2ELab presentation for adaptation as an expanded webinar version, to present the power electronics technology roadmap. More than 250 people attended the session.

JEAN-LUC SCHANEN & AL.
**Full 3D advanced packaging concepts
for Wide Bandgap based power electronics**

APEC – Applied Power Electronics Conference 2020

Large scale instruments for characterisation

Context and outlook

Large instruments are offering unparalleled performance for advanced characterisation of electronic objects. However, access to these instruments was designed for expert users, which is frequently the case among academic researchers, but less so among industrial users. Ennio Capria, Director of Nanoelec/Carac program, sheds light on the issue.

ENNIO CAPRIA, Deputy Head of Business Development at ESRF and Director of Nanoelec/Carac program

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What do the large instruments contribute to electronics R&D?

Firstly, we can explore the topography, morphology, physical properties and composition of components with extreme precision and very high resolution. Thanks to the very high penetrating power of neutrons and X-rays, it is possible to do this non-destructively, without opening them or destroying them. This is a major advantage when checking the quality of manufacturing processes, as of the R&D stage.

The second area of work is to study the effects of ionizing radiation on the components and systems. We are receiving a growing number of requests in this field.

Large scale instruments for characterisation program at a glance

👁 VISION

The unmatched performance of large-scale instruments to perform advanced characterisations of electronic components and devices has to be made known to industrial users.

⚗ AMBITION

Develop a competence center for testing radiation hardness of electronic components.

🎯 MISSION

Continue to make unique scientific instruments & methodologies available to serve the new challenges of the electronics industry

👥 PARTNERS

CEA | CNRS/LPSC | ESRF | ILL | Schneider Electric | Soitec | STMicroelectronics

What is the advantage of the Grenoble ecosystem in this area?

In Grenoble, we benefit from the presence of extremely powerful and totally unique European research infrastructures, in particular the ILL neutron source and the ESRF synchrotron. We also have the CNRS/LPSC whose accelerator outputs high-energy neutrons.

Admittedly, in 2020, the availability of the infrastructures was limited. On the one hand, the health crisis complicated access to the experiments and, on the other, our instruments underwent a large number of upgrades requiring temporary shutdowns. But, thanks to its new EBS source, the brightness of the ESRF has increased by two orders of magnitude and it now stands as the world's most intense synchrotron source. We have installed a new instrument alongside the ILL reactor, devoted to irradiation testing, called Tenis. Finally, the Genesis source at the CNRS which produces neutrons of 2.5 and 14 MeV has enjoyed a major flux gain.

Why develop a center of expertise for radiation testing?

We are looking in particular to examine the emerging

problem of loss of reliability which parallels ultimate miniaturization and complex packagings of electronic devices. The cause is the atmospheric radiation background noise present both at altitude and on the ground. The aim is to give our industry a competitive edge in the reliability sector. The large instruments are a very powerful means for measuring the sensitivity of new electronic technologies to ionizing radiation and neutrons, notably the atmospheric radiation background.

What problems are you studying?

For example, could artificial intelligence carried on board an aircraft fail when its computer is subjected to more intense radiation at high altitude than on the ground? How long can inexpensive memory chips withstand ambient radiation in a locomotive, a radio set, or even in our pockets? This is the type of question that we can explore with our partners and users.

As the same time, you are continuing with projects underway for several years?

The program is supporting technological develop-ments at Nanoelec, in photonics, power electronics, smart imagers and displays. Thanks to the collaborative structure of Nanoelec, the academic and industrial research teams in the consortium have access to the characterisation capabilities of the large instruments to develop new and wide-ranging methodologies.

And, for a broader community of users, the Advanced Characterisation Platform in Grenoble (PAC-G) is helping to maximize the value of this work by making it accessible to the national and European industrial ecosystem.

What do you feel is the most motivating aspect of the program for an industrial player?

We offer a range of services, from consultancy work to executing sample characterisation experiments and analyzing data. Through us, industry can access cutting-edge characterisation tools in service mode and in complete confidentiality. We also offer access to some of the world's most knowledgeable experts in the field of material characterisation. ■

AWARENESS TRAINING ON LARGE INSTRUMENTS FOR CHARACTERISATION

An original training module as an introduction to characterisation through large-scale instruments is provided by Nanoelec in English for international Master & PhD level students, for the second year.

The training module on characterisation was designed by two Nanoelec programs (Characterisation and Human capital & Training Design) in 2020. It was tested in person in March 2020 for 25 doctoral students from the University of Grenoble Alpes. It was then adapted to digital format and offered in May 2020 and January 2021. 25 students of the Doctoral School of Electronics, Electrical Energy, Automatic Control, Signal Processing at Grenoble-Alpes University attended the 2021 session.

"Our training program offers 8 courses including introductory and specific sessions on X-ray synchrotron and neutron radiations selected for their relevance to microelectronics applications", Manon Letiche says. She is one of the three engineers at ESRF and ILL heavily involved in the training session. *"In the same spirit, a one-day module on large scale facilities was set for master Nanotech students where we presented some illustrations with case studies carried out by nano electronics lab, on real research subjects. The students had to work on four case studies in order to develop their scientific reasoning elaborating an experimental plan including large scale facilities that could solve a specific problem"*, she adds. ∎


Picture taken in March 2020 during the very first course on the Awareness-building module on large instruments for characterisation: 25 students from Université Grenoble-Alpes attended the session. The students' evaluations of the module yielded a satisfaction rate of 8.6/10. Six students planned to submit a research proposal to the ILL or ESRF as part of their thesis.

© DR

Manon Letiche positioning a sample for irradiation experiments at the Nanoelec neutron beamline called Tenis at the ILL. As a physicist, she runs most of the Nanoelec experiments on the ILL facility. She is also heavily involved in training courses for PhD students at Grenoble-Alpes University.

P. Jayet/CEA
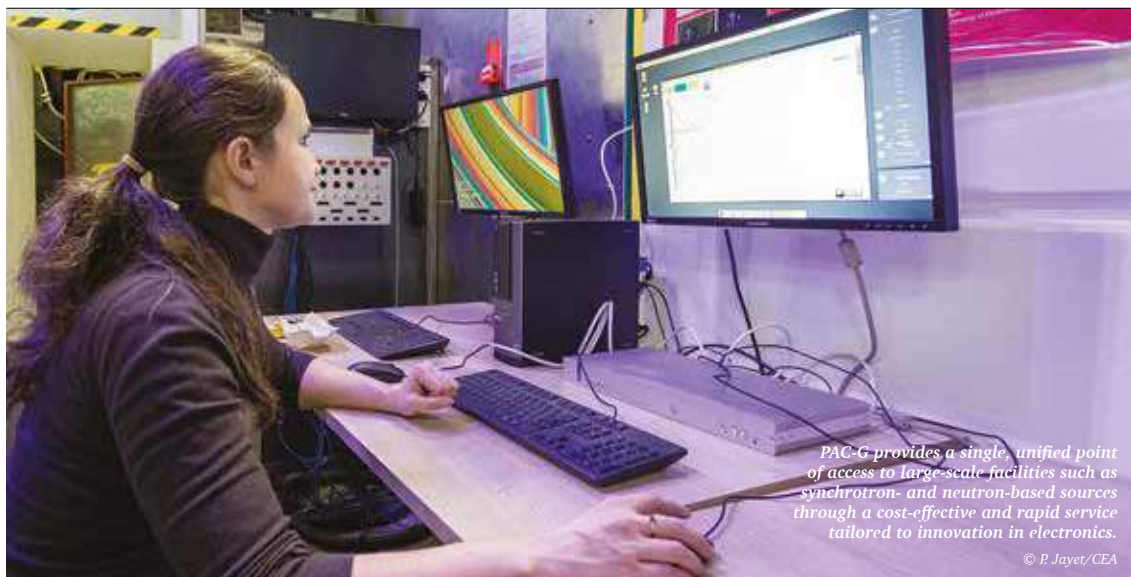
PAC-G provides a single, unified point of access to large-scale facilities such as synchrotron- and neutron-based sources through a cost-effective and rapid service tailored to innovation in electronics.

© P. Jayet/CEA

A GATEWAY TO LARGE-SCALE INSTRUMENTS DEDICATED TO ELECTRONICS INDUSTRY NEEDS

PAC-G is a dedicated gateway giving the electronics industry quick and easy access to some of the world's most advanced characterisation facilities.

As ESRF/BM05 beamline responsible, Phil Cook is checking an X-ray mirror focusing the synchrotron beam on the sample to be irradiated. The beamline is a key component of the Nanoelec/ Carac program. It has been entirely redesigned during the ESRF / EBS upgrade in 2018 2020. An instrument developed with CEA-Leti is dedicated to thin film characterization techniques for electronics. In addition, a robot ensures the automation of X-ray topography tests, one of the key techniques of the PAC-G.

P. Jayet/CEA

PAC-G also provides an extremely broad portfolio of individual but complementary characterisation techniques. *"We are unique, offering a single, unified point of access to large-scale facilities such as synchrotron- and neutron-based sources through a cost-effective and rapid service tailored to innovation in electronics"*, says Caroline Boudou (ILL), senior scientist in charge of Nanoelec projects at ILL. In 2020, outside the confinement period, the occupancy rate of the PAC-G instruments was high (1,108 hours of beam time for users), mostly for manufacturers linked to the field of microelectronics (around 70%). Thus, 412 hours of commercial access were provided by industrial customers via Nanoelec. ∎

THE BEST SOURCES FOR IRRADIATION

After an upgrade phase of one year, the Genesis facility (Generator of Neutrons for Science and Irradiations) came back in operation for both academic and industrial users with a flux up to 7.109 n/cm²/s of 14 MeV neutron.

This instrument hosted by the Laboratory of Subatomic Physics & Cosmology (CNRS/UGA) is on the cutting-edge at the European level. It operates an accelerator-based neutron source which can provide an intense neutronic flux either at 2.5 MeV or at 14 MeV. This unique accelerator is equipped with an original compact ECR ion source capable of delivering a continuous deuteron beam at 220 keV in the mA range.

The Genesis facility is mainly used for single-event effects testing in microelectronics. It is alos used to test detectors (diamond, Si) wafers.

Access to this instrument unique in France is included in the PAC-G offering for industrial stakeholders. The ESRF came back in operation in September 2020, being now the most brilliant synchrotron source in the world. *"At the same time, the BM05 beamline dedicated to Nanoelec/Carac has been entirely refurbished"*, says Phil Cook in charge of BM05. *"An instrument developed with CEA-Leti is dedicated to thin film characterisation techniques for electronics. In addition, a robot improves the level of automation for X-ray topography measurements, one of the key techniques of the* PAC-G." ESRF–EBS (Extremely Brilliant Source) is the ESRF's €150M facility upgrade, over 2015-2022, bringing its scientific users a first-of-a-kind, low-emittance, high-energy synchrotron light source and new, cutting-edge beamlines. *"With its extremely brilliant X-rays, the ESRF-EBS offers incredible resolution in space and time. This enables unprecedented tools for understanding the materials in electronic devices at the nanometer scale; we offer these tools to the electronics industry through Nanoelec's characterisation services"*, underlines Cook. ∎

Luca Capasso is positioning a wafer on the Nanoelec giant goniometer on the ESRF/BM05 beamline. Radiative particles may cause major disruption of computing capacities in critical applications. To cope with the unprecedented generalization of digital devices, Nanoelec set up a center of competence for the effects of radiation on ICT components.

P. Jayet/CEA

WORKSHOPS & CONFERENCES

CARAC'20

Characterisation of new electronic components is essential to their design and ultimately to ensuring their reliability.

The 7th edition of the Carac Symposium took place on a Nanoelec webinar platform attracting 50 attendees online. This edition focused on the performance gains of the very large equipment available at the ESRF, ILL and CNRS/LPSC under the Nanoelec/Carac program. Carac is a unique event dedicated to materials characterisation for the electronics industry. Before a live online visit of the ESRF and ILL facilities, attendees had the benefit of contributions from the Grenoble-INP, CEA-Leti, Néel and Irig institutes, CNRS-LPSC, ESRF/EBS and ILL.

RADIATION TESTING

Radiation effects in semiconductor devices is one of the major reliability concerns in today's electronics.

Continuous scaling and the ubiquitous presence of sensors and components in our day-to-day life now means that these effects play a major role in the performance of electronic systems. Moreover, several reliability questions arise from new applications (such as self-driving cars, nanosatellites, medical implants…). As the demand for radiation hardness testing is on the rise, the availability of radiation facilities providing industrial access to these tests seems to be decreasing. Traditional testing methodologies also seem to be limited in the face of new semiconductor technologies.

In December 2020, the very first edition of Nanoelec/G-RAD workshop brought together testing facilities and radiation experts and stakeholders from industry and academia to stimulate discussion on current and future needs in radiation hardness testing and evaluate the limitations of available radiation facilities and possible developments.

CHARACTERISATION FOR GAN RAMPING UP TECHNOLOGIES (WITH SERMA)

Gallium Nitride technologies are gaining ground and are the focus of investment efforts by the largest players in the RF and Power electronics markets.

To confirm its performance, this technology requires advanced means of characterisation. In October 2020, Serma Technologies, Science & Surface, Nanoelec and CEA Tech presented different techniques for characterising both the manufacturing quality and the dynamic functioning of GaN components. This original webinar attracted 160 attendees (220 signed up), mostly from industry. Serma Industries contributes to PAC-G as a characterisation service provider.

Key publications

DRAM under thermal neutron irradiation

At DTIS 2020: EEE 15th International Conference on Design & Technology of Integrated Systems in Nanoscale Era, a European team reported on static and dynamic test methods used to define the response of a self-refresh DRAM under thermal neutron irradiation. Neutron-induced failures were investigated and characterised by event cross-sections, soft-error rate and bitmap evaluations, leading to an identification of permanent and temporarily stuck cells, block errors, and single-bit upsets. *"Estimations of cross-section for the different kinds of failures show that the memory is not very sensitive to thermal neutrons. However, the effects of the neutrons may be critical in some specific applications: block errors were observed in four different patterns, with intermittent word errors in vertical and horizontal sequential logical addresses, and also presenting divided vertical lines with all bits of a word with errors, and a sequential error with dependency in the addressing order"*, said Manon Letiche, in charge of irradiation measurements at the D50 Nanoelec beamline at ILL.

A 28-nm SRAM-Based FPGA subjected to 14-MeV neutrons

An international team including scientists from Université Grenoble-Alpes and CNRS involved in Nanoelec conducted a characterisation of the sensitivity of a Xilinx Artix-7 field programmable gate array (FPGA) to 14.2-MeV neutrons. Irradiation experiments were performed at the Genesis CNRS facility. The content of the internal static random access memories (SRAMs) and flip-flops was downloaded to a PC and compared with a golden version of it.

Synchrotron tomography on hybrid bonding-based test structures of back-side illuminated CMOS image sensors

As part of the development of back-side illuminated CMOS image sensors, high-resolution synchrotron tomography has demonstrated proportionality between electromigration-induced void volumes and time-to-failure in hybrid bonding-based test structures. *"Our new sample preparation workflow is compatible with synchrotron-based tomography for statistical studies. We aim to make it a tool for routine measurements"*, comments Stéphane Moreau (CEA-Leti), first author of the study. *"We observed a conventional failure by voiding in long feed lines of the BEoL. Process-induced bonding voids do not affect the reliability of the analyzed samples. Due to non-uniform distribution of the electric current in the region attached to the via matrix, the failure time is sensitive to the exact location and shape of the electromigration-induced void. This gives key information for understanding the role of via redundancy, which is provided by using via matrices, in increasing the electromigration robustness of interconnects"*, adds Moreau.

The high-resolution synchrotron tomography experiments were performed on the ID16A beamline at the ESRF using samples prepared by STMicroelectronics under the Nanoelec/Carac program.

Assessment of On-Chip Current Sensor

For the very first time, a body/bulk built-in current sensor (BBICS) in a CMOS 65-nm test chip has been assessed under thermal neutron, high-energy neutron and laser radiation. *"The kind of sensor we studied is useful for embedding in electronic computing systems requiring high reliability and also security and low-power specifications, such as in the aerospace, industrial automation, and automotive fields. These on-chip sensors operate as an online testing mechanism able to set a flag when radiation-induced transient faults perturb a chip sub-circuit"*, explains Rodrigo Possamai Bastos, associate professor of computer engineering at Grenoble-Alpes University and Tima Laboratory. As a first author, he signed the study published in the IEEE Transactions on Nuclear Science Review. This study includes contributions from scientists associated with Nanoelec. Thermal and fast neutron irradiations were performed at ILL and CNRS/LPSC, on experimental setups operated under Nanoelec.

"Experimental results suggest that the on-chip current sensor is effective in detecting transient faults in different case-study sub-circuits of the chip exposed to accelerated radiation effects, opening up prospects for embedding this type of sensor in reliable, secure, and low-power integrated circuit applications", Dr. Bastos adds.

RODRIGO POSSAMAI BASTOS
(UNIVERSITÉ GRENOBLE-ALPES)
& AL.
Assessment of On-Chip Current Sensor for Detection of Thermal-Neutron-Induced Transients

How machine learning may be affected in aircraft at altitude

Hardware-implemented machine learning algorithms are finding their way into various fields, including safety-critical applications. This requires that these algorithms perform correctly even in harsh environmental conditions, such as in avionics at altitude. Support Vector Machine (SVM) is an important Machine Learning method that has been the target of hardware implementation in recent years. Matheus Garay Trindade and his colleagues from UGA, ILL and Universidade Federal do Rio Grande do Sul (Brazil) published the first work to assess both Binary and Multiclass SVMs under thermal neutron radiation. "Thermal neutrons are noticeably present at high altitudes", Garay underlines. *"That's why we performed a fault injection campaign along with a radiation test with the D50 thermal neutron source, operated through Nanoelec at the Institut Laue-Langevin. Our results show high intrinsic fault tolerance for both varieties of the SVM algorithm, especially for the Multiclass SVM. In the future, we intend to evaluate different datasets for both the Binary and Multiclass SVMs. We also plan to conduct more fine-grained fault injection campaigns , e.g., injecting faults in each individual SV or in specific regions of the circuit, with multiple datasets, in order to try to generate a reliability model that we could potentially extrapolate to other datasets. Furthermore, we plan to test different architectures for the algorithm"*, he adds.

MATHEUS GARAY TRINDADE
(UNIVERSITÉ GRENOBLE-ALPES)
& AL.
Effects of thermal neutron radiation on a hardware-implemented machine learning algorithm

Human Capital & Training Design

Sustainability as a driver of innovation

Micro-nanoelectronics is an area of particular technological intensity, facing major national and european challenges in terms of sovereignty and corporate competitiveness. For the microelectronics industry, the ecosystem goals were set out when the sector's Strategic Committee contract was signed with public authorities on 15 March 2019:

→ Maintain technological excellence by ramping up research, development and innovation efforts, above all in the digital field;

→ Adapt skills and training by anticipating changing requirements and support recovery so that supply matches demand;

→ Boost the attractiveness of a career in the microelectronics industry and of a competitive technology.

These issues entail challenges and specific needs, in terms of skills development, which is one of the reasons for the IRT Nanoelec training program: speed with which skills change; appearance of new professions that are rapidly under pressure (rapid change in markets); need for a broader vision incorporating the ability to interface with applications sectors such as energy, health or mobility.

In this context, this program is specifically positioned to meet the needs of the electronics sector in line with the demand for academic excellence and technological progress driven by scientific laboratories and training organizations of the Nanoelec consortium. A second characteristic of this program is its transverse nature, covering all skills requirements, from technology to its distribution on the markets and, increasingly, sustainable development.

Like most of the major universities (such as Stanford, Georgia Tech, Aalto, NUS, KIT...), the Human Capital and Training Design program at Nanoelec has opted to develop experience-based teaching, involving the students in the projects and experiments of the consortium, using demonstrators, prototypes and Labs facilities. ■

SYLVIE BLANCO, Professor and Executive Director of Innovation at Grenoble Ecole de Management and PANAGIOTA MORFOULI, Professor at Grenoble-INP (Grenoble Institut d'Ingénierie et de Management)/UGA, are co-diretors of the the Nanoelec/Human Capital & Training Design Program

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Market 2

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Chif
program
at a glance

👁 VISION

The attractiveness and competitiveness of the electronics sector are tied into the development of interdisciplinary, agile collaboration capacities.

📐 AMBITION

Design and experiment with an integrative and customized learning and training system that strengthens the human capital and the dynamic innovation capabilities of the institute and its academic and industry partners.

🎯 MISSION

Design and develop-new training module contents and formats. They are organized around three areas: fundamental skills (science and technologies, management, innovation), experience-based learning (demonstrators and labs), learning communities to tackle emerging challenges (new roles of teachers, new learning practices vs energy, environment, digital transitions).

👥 PARTNERS

Grenoble-INP |
Grenoble Ecole de
Management (GEM) |
STMicroelectronics

SCIENTIFIC AND
TECHNICAL SKILLS

© Grenoble-INP

Hardware cybersecurity

"Owing to the lack of appropriate equipment, practical teaching in the field of hardware security on the Grenoble University site was hitherto mainly theoretical and based on computer simulations", explains Paolo Maistri, CNRS researcher and training instructor at Grenoble-INP. *"Within Nanoelec, we therefore developed the equipment needed for this practical teaching on real targets: hardware setup and algo-*rithms supporting different types of attacks."*

The module was also suitable for remote digital teaching. *"It is essential to consolidate the skills of our students in the field of hardware security, a major challenge for the electronics sector and, more particularly, the partners of IRT Nanoelec"*, recalls Paolo Maistri, who also says that *"the large number of students on the cybersecurity course forced us to take a fresh look and modify the practical work (choice of hardware, type of exercises, etc.) and how it was carried out (remote/face-to-face) in the context of the pandemic."* ∎

The students work on electricity consumption data for a classroom in the Predis MHI, a 600 m² living lab type experimental platform inside the GreEn-ER low-consumption building.

© Denis Morel/G2Elab/CNRS Photothèque

Power electronics

Within Nanoelec, Grenoble-INP coordinated the design of modular teaching building blocks in the field of power electronics. *"Our goal is to provide the students working on their projects in the Fablab with rapid, robust, secure and instrumented prototyping resources"*, explains Jean-Luc Schanen, professor at Grenoble-INP and head of the Power Electronics group at G2ELab, which is also associated with the Nanoelec/Powergan program. ◼

Artificial intelligence for energy in buildings

The Predis MHI [1] platform at Grenoble-INP is working on experimenting with innovative technical and social solutions. The "ICT4 People into everyday energy" module in English prefers "learning by doing" type teaching: the students work on the interfaces between humans and the cyber-physical systems around them, on the basis of occupancy data for an experimental Green-ER building (via Predis MHI). *"One of the things* we have developed is a smartphone application to present energy and comfort data to the building's occupants"*, explains Benoit Delinchant, Professor at Grenoble-INP. *"It is made available to the students and aims to make complex data comprehensible and create a trust-based link between the automated energy system and the building users. With regard to the data themselves, we have also made Open Source developments to make the data accessible via artificial intelligence embedded by web solutions."* Teachers use these data as application support in the form of case studies, notably for neural network automatic learning. ◼

[1] Predis MHI is a 600 m² "living lab" type experimental platform inside the GreEn-ER low-consumption building.
It is dedicated to studying energy usages inside buildings, in interaction with the occupants and the energy networks.

MARKETS, INNOVATION AND ENTREPRENEURSHIP

660 students in a digital classroom

Grenoble Ecole de Management (GEM) defied Covid: for the very first time, 660 first year students of the Grande Ecole Program (PGE) came together on September 14th, 2020 in the large auditorium. Masks and sanitizer gel were not mandatory because the auditorium was located on GEM's new remote digital campus. The meeting was to launch the 2020 Back-to-School challenge on six issues combining technology and society, in addition to a reflection on the impacts of image portrayals through a digital avatar.

To do this, GEM, within Nanoelec, has designed an escape game which takes place within the digital campus co-developed with Virbela – Laval Virtual. The students' mission was to propose a "New Deal to think and impact the world" project. They had to consider the six societal challenges identified during the health crisis and the priorities of the local territorial ecosystem: health, energy, education, city (mobility), work and food. *"Our new students had ten days to prepare to pitch their "new deal" project to a jury in an exhibition comprising 144 virtual stands"*, comments Sylvie Blanco (GEM).

AACSB [1] rewarded the GEM digital back-to-school challenge in its annual 'Innovations that inspire' awards. *"Grenoble Ecole de Management has embraced the call to create positive societal impact"*, underlines Caryn L. Beck-Dudley, AACSB president and CEO. The challenge also received a Digital Learning Trophy [2]. ∎

[1] AACSB International (AACSB), a global nonprofit association, connects educators, students, and business to achieve a common goal: to create the next generation of great leaders. Synonymous with the highest standards of excellence since 1916, AACSB provides quality assurance, business education intelligence, and learning and development services to over 1,700 member organizations and more than 840 accredited business schools worldwide.

[2] Initiative of Féfaur, European leader in independent consulting in Digital Learning strategy and training evaluation.

The digital animation team during the GEM 2020 Back-to-school challenge, designed with Nanoelec
© GEM

In 2019, during a face-to-face session, the board version of the Créanov serious game created in 2017 with Nanoelec. The digital version, which can be played remotely, was prototyped and published online at the end of 2020.

© GEM

Open mind role-play for innovators

By means of a statistical game, finding two thirds of the possible innovations in a category of products or services: this is what GEM proposes with Creanov. This game is intended for innovation and creativity teachers as well as corporate innovation teams. It was developed to implement a scientifically proven method. It was prototyped and published within Nanoelec for the face-to-face sessions in 2017 and adapted to digital format for the remote sessions in 2020. *"The validated methodology of the basic structure demonstrated its pertinence in supporting the innovation process at a number of companies. It is based on analytical and systematic approaches and is particularly relevant for engineering environments.*

It consists in breaking down an existing product into characteristics of two types – its components and its attributes – before then exploring their various configuration possibilities. This is extremely effective for product digitization issues", recalls David Gotteland, professor at GEM and one of the two designers of the game with Aurélie Merle.

Creanov is targeting two audiences: students and managers in charge of innovation: product managers, R&D managers. More than 1,100 students and 110 persons in executive training programs have already used the board game version of Créanov. *"On 4 January 2021, 750 GEM students used the digital game. Twenty teachers had been trained to coordinate the remote sessions on-line"*, explains Isabelle Patroix, Playground Manager at GEM, who was responsible for digitization.* ∎

Sensor-based customer experience with embedded artificial intelligence

Within Nanoelec, the GEM teams have designed and developed the mock-up of an experiential module on customer meetings. Its purpose is to develop new knowledge of marketing and innovation management as related to the possibility of using data from real site, in real time. Three use cases of applications are targeted: shopping process and image sensors with embedded AI; air quality and data appropriation; smart experimentation zones for consumer experience in mass retail or medical care.
"With these new knowledge, our students will develop marketing and sales skills and practices →

aligned with the digital ramp-up", explains Christian Rivet, professor of marketing at GEM. *"They will work on smart offers that can give rise to personalized services for the emerging user. This can be, for example, an alert on the management of queues in stores or the optimization of the organization of purchases in a shopping center according to attendance"*.

This module contribute to the development of entrepreneurial postures making possible to think and appropriate new technologies (such as sensors and associated AI, for example) as levers of value creation for the customer. Rivet recalls that *"for the customer, the experience begins before the purchase and ends with the recycling of used or obsolete products"*. ■

At GEM, use of facial recognition functions with Nanoelec, for the development of an experience-based module on digital integration into the customer experience.
© GEM

TRANSVERSAL SKILLS

A very first participatory module on sustainable electronics

Students of the international master's degree "Micro and Nanotechnologies for Integrated Systems" of Grenoble -INP (UGA), Politechnico of Turin and EPFL Lausanne, used a brand new training module provided in English, during which they had to design a mobile phone incorporating micro-electronic components designed with sustainable development (greenphone) in mind. This new educational approach was created and facilitated by experts from CEA, STMicroelectronics, Grenoble INP (UGA) and Grenoble Ecole de Management and prototyped as part of Nanoelec.

Forty master's students tested it over one day in January 2020. They worked in teams on different stages of the product life cycle (materials, design, manufacturing, use and end of life). At the end of the module, they presented a set of measures and processes to meet environmental requirements. The result was plenty of creativity and a solid demonstration that respect for the environment, through in-

dustry and technology, is crucial for young engineers involved in the sector.

"We had a whole day in direct contact with practicing professionals. With them, we were able to work on the entire life cycle of electronic devices", says Sarra Sfar, a student of the master's program. *"Without a doubt the greatest contribution of the module was putting us in a position to think 'outside the box' in order to identify radically new solutions. The day gave us the opportunity to grasp a multidisciplinary tool to innovate in a collaborative and creative way"*, added Nazareno Sacchi, also one of the master's students.

→

"It is important for us to share with the young generations of engineers, in particular those whom we may recruit, our company's commitment to sustainable electronics", explains Laurent Jamet, Director of Innovation & New Ventures, Analog, MEMS & Sensors Group at STMicroelectronics who participated in the day-long event, along with four other experts in the field.

"As a future engineer, I believe that I have a very important role in today's society and in that of tomorrow. In my future job, I must, of course, be able to meet people's needs with respect to digital systems, but to also respect the environment and preserve our resources such as water, energy and materials", adds Sarra. Nazareno also believes that he will work in the role of 'inventor and pioneer' to bring about a 'modern and environmentally friendly' society. ∎

During a workshop based on 'my IOT', a serious gam created by Nanoelec and Université Grenoble Alpes Idex Cross Disciplinary Program "Need for IOT"

@ P. Jayet/CEA

Designing a sustainable phone through a serious game approach

57 students from Grenoble-INP/ Phelma and Grenoble Ecole de management (GEM) took part in a "Sustainable Electronics" workshop organized on February 5 and 12, 2021 by the Nanoelec/Human Capital and Training Design (Chif) program.

"During the two sessions, the students worked in small groups →

with the aim of conducting an in-depth analysis, with the experts, of the design of a smartphone incorporating micro-electronic components designed in a spirit of sustainable development (greenphone)", explains Panagiota Morfouli (Grenoble-INP).

Like last year, the educational approach was devised and led by experts from CEA, STMicroelectronics, Grenoble INP (UGA), Time for the Planet and Grenoble Ecole de management and prototyped within Nanoelec. At the beginning of the workshop, the students worked on the societal challenges of sustainable development from an industrial viewpoint, with STMicroelectronics, and from a legal and ethical viewpoint, with GEM.

This year they had a brand new tool called "My IoT" designed and produced by the Need For IoT (Cross disciplinary program at Idex UGA) along with Nanoelec. "This serious game complements existing offers", explains Laetitia Thomas, pedagogical engineer at UGA and designer of the tool. "After having been made aware of the various impacts of the IoT supply chain, participants together create possible solutions in line with circular economy goals".

This collaborative game aims to raise awareness and initiate a change in mentalities and behaviors regarding the impacts of the globalized micro and nanotechnology industry in an accessible, innovative and engaging way. ∎

Supply chain for innovation

The RnDyneo module developed in 2018-2019 by the partners of the Nanoelec/Human Capital and Training Design program, deals with the agile behavior of R&D teams at STMicroelectronics involved in transverse projects, following on from the action taken by the company with its Manufacturing teams. "The positive impact of this training led STMicroelectronics to re-quest an extension of this module intended for the buying and Supply Chain teams", explains Pierre Chevrier, associate professor of R&D management at Grenoble-INP. "In 2020, we therefore designed a new module with the aim of stimulating good customer-supplier practices in favor of collaboration and innovation."

Building on a new serious game, the SupplyChain module is intended for continuing professional training of industry personnel as well as initial training of engineers and international masters. ∎

Workshop based on the SupplyChain serious game created by the Nanoelec/Human capital & Training Design program
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A playground connected shop at GEMLabs
© GEM

Technology dissemination

Promoting the adoption of emerging technologies in new applications fields

The economically tense conditions created by the Covid-19 pandemic reveal more than ever the need to help companies become more competitive. As far as the digital transition is concerned, technologies and components are focused on a few mass markets and companies sometimes lack the information and the in-house skills to integrate new technologies. Yet, these technologies are indeed opportunities to expand their offering and strengthen their commercial position.

With the Technological Dissemination program, the partners in Nanoelec are promoting and accelerating the dissemination of emerging contents in a variety of application fields; they are drawing more particularly on R&D skills in imaging, artificial intelligence, embedded software and electronic systems design.

The program comprises two initiatives:

→ The aim of the System Lab initiative is to exploit components developed by the main partners involved in R&D programs at Nanoelec, primarily in the field of imagers. New applications are being explored.

→ In the Easytech initiative, we make advanced electronic building blocks accessible to very small, small and medium and mid-cap business, including those whose core business is anything but digital. The aim is to enable them to take the digital transition on board, to increase the added value of their products or improve their manufacturing processes. ■

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Easytech: growing success with SMEs, mid-caps and startups

Established in 2012, the Nanoelec/Easytech initiative provides global support for SMEs and mid-caps in their innovation process (creativity, expertise, R&D project). It is run by Minalogic, a competitive cluster for digital technologies, supported by the Auvergne-Rhône-Alpes Region and local authorities. Elvir Mujic (Minalogic) is co-director of the technology Dissemination program, in charge of the Easytech initiative.

You are taking charge of the program in 2021. What has Easytech achieved so far?

Under the leadership of Damien Cohen between 2014 and 2021, Easytech attracted an increasing number of companies. It offers a simple and easy fast-track to innovation projects. It is seen as such by the managers of small companies, as well as startups, who do not necessarily have large R&D departments to assess the pertinence of what is available. 281 Easytech projects have been sponsored with more than 200 companies since 2012.

What are the profiles of the companies you target?

We deal primarily with SMEs, a few mid-caps and a few large companies. Most of these companies are in the Auvergne-Rhône-Alpes region. Their core business is usually electronics but also sometimes maintenance and mechanics, instrumentation, materials, or other fields.

Their applications markets are highly diversified, ranging from space to health, to new modes of mobility, construction, sport and the agriculture+food industry.

What motivates you in working with SMEs?

Being able to help SMEs carry out their innovative project is highly stimulating! The diversity of subjects, topics and technologies used is impressive and intellectually energizing. Moreover, without this support, many projects would not see the light of day, or would not have gone so fast or so far. Feeling useful day after day, that's motivating!

What is the contribution of local authorities?

Like all IRTs, Nanoelec's mainfocus is not solely thematic, but also regional. This is why the local authorities top up funding for the Easytech projects. This helps bring down the financial risk for the local companies that innovate with us. First of all, the Auvergne-Rhône-Alpes region contributes at a level of 20% to the labelled projects. Moreover, local authorities (mainly cities and urban areas) can add 10% for projects for SMEs based in their district. This is the case with Grenoble Alpes Métropole, Valence Romans Agglomération, Saint Etienne Métropole, Thonon Agglomération, La communauté du Pays Voironnais, Annemasse Agglomération, Clermont Auvergne Métropole. More than one quarter of our projects are also carried out with companies in other regions of France. ■

ELVIR MUJIC,
Minalogic Director at St-Etienne
& co-director of the Technology
dissemination program
at Nanoelec, in charge of
the Easytech initiative
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SystemLab: time for new usages

Experimented in 2020, SystemLab was established as part of the Nanoelec Dissemination program in 2021. Y.Spot, the open innovation center at CEA, runs the initiative. Sandra Tochon (CEA-Y.Spot), co-director of the Technology dissemination program, in charge of SystemLab, explains.

Where did the idea of creating SystemLab come from?
Together with our main industrial partners, we felt that it would be interesting to enhance Nanoelec's technological dissemination offering, by organizing a stronger and more direct link with the R&D programs. In the SystemLab initiative, we work with the component manufacturers looking to explore new application fields.

What is the concept?
We are exploring application of new components based on the synergies between building blocks provided by various partners and on approaches closely linked to the potential users. In the medium or long term, we will use the results of this process to expand or enrich the characteristics of our partners components and generate opportunities for new technological routes.

So what is the approach?
The SystemLab partners share , an open technical mock-up and marketing platforms, methodologies to support open innovation processes

SANDRA TOCHON, co-director of the Technology Dissemination program at Nanoelec, in charge of the SystemLab initiative.
© P. Jayet/CEA

combining creativity skills, exploitation of usage scenarios, value analysis and eco-design. Wecreated an open platform for use case exploration and evaluation based on merging optical sensors data flows. The components are supplied byour partners for which we carry out time and space interfacing.

What fields are concerned?
We work first of all on the functions and services that can be introduced by multispectral image sensors. We aim to seek out what has not yet been explored. This means that we have to take account of many additional technical aspects, such as AI, data security, and data communication.

What is the driving force behind your coordination of the initiative?
SystemLab is a new way of exploiting the technology that we, engineers, hold so dear. It enables a link between the largest possible number of players, from widely differing backgrounds and sectors. which means meeting committed and fascinating men and women, virtually every day.

We benefit from pathways already opened up by our colleagues in the open innovation team at CEA-Y. Spot. Their methods for leading workgroups and generating new designs are absolutely amazing. It's now up to me to organize and coordinate that for our partners!

What fields are concerned?
The developments designed in SystemLab can concern component architectures, but also new functions (security, signal processing) or manufacturing processes needed for implementation of these innovations on the products. We work first of all on the functions and services that can be introduced by multispectral image sensors. ■
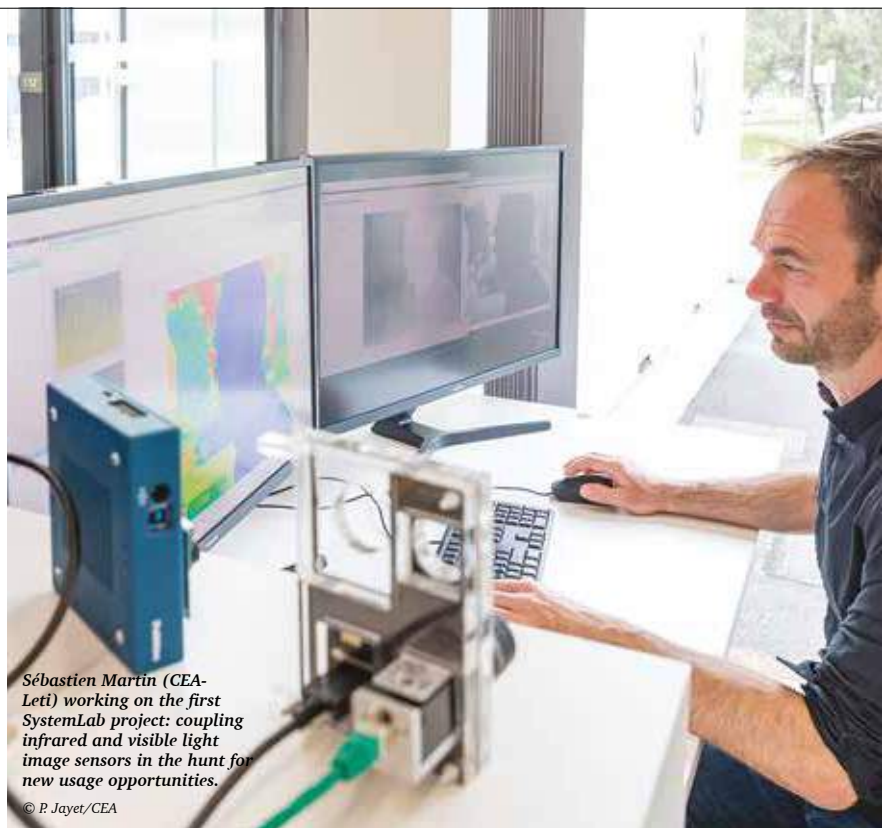
Sébastien Martin (CEA-Leti) working on the first SystemLab project: coupling infrared and visible light image sensors in the hunt for new usage opportunities.
© P. Jayet/CEA

Sébastien Martin (CEA-Leti) and Gaël Parent (Y.Spot) test an unprecedented imaging system developed by SystemLab, for a sports application.
© P. Jayet/CEA

ELECTRIC AIRCRAFT

Aviathor is offering light aircraft owners a chance to replace their internal combustion engine with an economical and silent electric motor.

The startup was created in 2019 and has signed a number of pre orders with several aero clubs in the Auvergne-Rhône-Alpes region. It ran an Easytech project with Grenoble-INP in 2020.
"Thanks to the students at Esisar, we were able to develop a hardware and software solution for the transmission of commands between the flight controls and the aircraft's electric motor", explains Benoît Cocheteux, founder of Aviathor. *"The PCB we developed ensure quadruple redundancy to make the flight control more reliable. We are now in the industrialization phase."* ■

CONNECTED HEATER

Lancey Energy Storage is developing solutions to optimize self-consumption and heating systems, combining battery storage of electricity and heating management in the home or other buildings.

By incorporating storage capacity and an EMS (Energy Management System) in its heater system, Lancey enables its customers to achieve up to 100% photovoltaic self-consumption, increase thermal comfort and drastically reduce energy consumption in the building. Lancey heaters can communicate with their server and their environment to "learn" the habits of the users, react to the grid and provide feed back information to the building managers (predictive and remedial maintenance). In 2020, under an Easytech project carried out at Grenoble-INP, Lancey was able to incorporate a new communication protocol (Thread) to improve the reliability, security and interoperability of its digital connections. ■

© Lancey Energy Storage
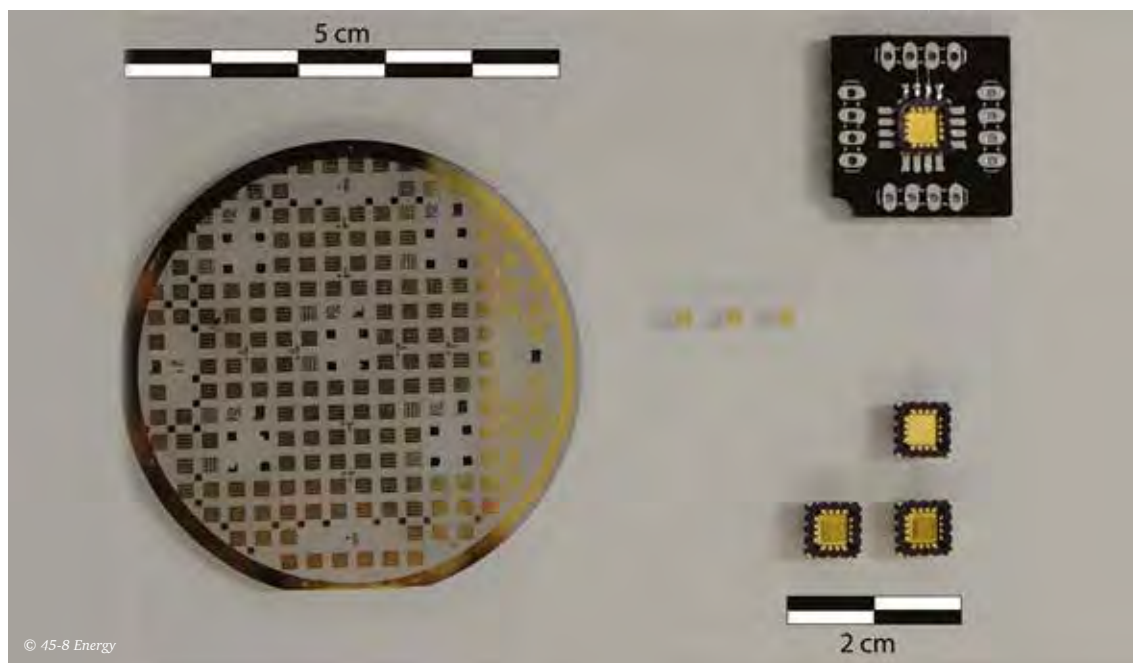
© 45-8 Energy

UTILIZING NATIVE HELIUM AND HYDROGEN

Because helium and hydrogen are present in native state in the Earth's crust, the 45-8 Energy startup intends to achieve exploitation of these two gases, which are both environmentally friendly and vital in many applications.

Under a Nanoelec/Easytech project headed by Captronic, it is examining the feasibility of a sensor intended for in-situ monitoring, which would function independently for a minimum of 12 months. *"Our device would be buried at shallow depth and be capable of wireless transmission of the data acquired, at least once a day"*, says Nicolas Pelissier, founder of 45-8 Energy, the aim of which is to explore and produce these gases in France and in Western Europe, for the European market. Finally, building on the development of a proof-of-concept compact sensor with 16 transistors, the company grew from 4 to 12 employees and raised 1.3 million euros in 2020. ∎

PLASTRONICS

MCVE Technologie is a startup created in 2019, which is developing an additive manufacturing technology for functionalizing plastic materials and composites.

It is working in the field of plastronics and will rapidly be offering solutions for adding electronic functions to plastic parts or print circuits on flexible items.

"The Easytech project that we ran in 2020 under the supervision of Captronic/Jessica France was able to evaluate the additive technology and its compatibility with industrial electronic component assembly processes", explains Christian Weisse, founder and CEO of MCVE Technologie. *"Building on the commitment of our first commercial contacts, we are preparing to hire our first business development manager"*. ∎

"MEASURING" ODORS

In July 2020, Aryballe Technologies raised 7 million euros to industrialize its artificial nose. The Grenoble startup, founded in 2014, develops, manufactures and markets a completely new sensor that provides rapid identification of odors.

> " *Thierry Livache, CSO at Aryballe, looks back at the two projects he ran with CEA under the Easytech program, in 2015 and 2020.*

What was your project in 2015?
We built a functional demonstrator of an odor detector based on surface plasmon resonance. We already had a prototype but were able to integrate an airflow circuit sampling air via a fan, a compact optical module with a LED source, a glass prism and a CMOS 2D monochrome sensor with a lens and its PCB.
With this relatively large functional demonstrator, we were able to attract enough investment to rapidly grow from 1 to 10 engineers.

In 2020, you integrated a completely new technology. What is it?
A new photonics on silicon approach was developed by Aryballe and CEA-Leti. This project succeeded in establishing a chip production flow and carry out technology transfer to a components fabrication plant/manufacturer specifically for our needs. Our strategy is now mainly focused on marketing an odor sensor using this technology.

Which companies are supporting you?
In 2020, Samsung and the SEB group joined the company's original investors (Asahi Kasei, Hyundai and International Flavors & Fragrance). ■


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AIR QUALITY MONITORING

eLichens was created in 2014 in Grenoble and provides information about the quality of the air we breathe.

Using miniaturized, connected and ultra-low consumption sensors, hyper-focal air quality monitoring is possible in a professional environment (industrial sites, offices, public spaces) or in the home. The company ran two Easytech projects with CEA, in 2019 and 2020.

"In 2019, we explored a pyroelectric membrane type technology to detect and measure carbon dioxide and methane, explains Pierre Jallon, CTO of eLichens. *Last year, we turned to a completely different subject: detecting pollen in air, as this causes allergies for many people every spring."*

The company raised 6 million euros in 2020. *"These funds will help us with mass production of gas sensors and gas leak detectors, but also with deploying air quality monitoring stations"*, says Pierre Jallon. ■
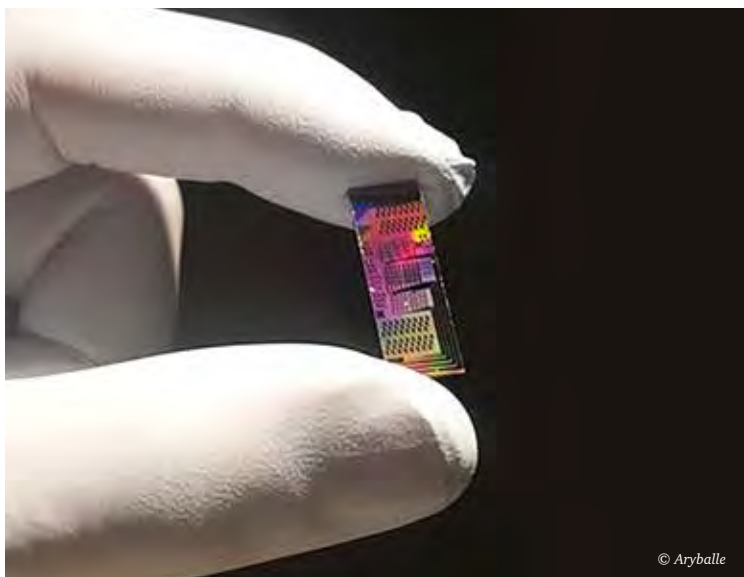
In 2020, about ten Easytech projects were carried out thanks to the student-engineer teams, with the support of the teachers and researchers at Esisar, the school of the Grenoble-INP - UGA group located in Valence.

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PUBLIC-PRIVATE R&D SYNERGY IN AUVERGNE RHÔNE-ALPES, FRANCE

Every year, Grenoble-INP oversees around ten Nanoelec/Easytech projects, which have been increasingly focused on digital technology, connected systems and embedded artificial intelligence.

> *Karim Chibane, Head of Technology Transfer at Esisar and Head of the Grenoble-INP Easytech Program, explains.*

Can you tell us about the Esisar program?

Every year for more than 20 years, the infrastructure and organization at Esisar has enabled the launch of thirty or so industrial projects in conjunction with companies from the Auvergne-Rhône-Alpes region. Each year, about ten of these projects are part of the Nanoelec/Easytech program, run by the global innovation cluster Minalogic.

How are the projects carried out?

Each year, Esisar fourth-year engineering students break up into 3-person teams to work on a project for a company. From January to June, each group has access to its own entirely equipped facility. Students are ensured to benefit from university/company supervision and support on a daily basis.

All the teams work in the same location and have access to pooled services and professional logistic and technical support. The R&D collaborative projects are carried out in optimal operational conditions and in compliance with the confidentiality requirements of partner companies.

How have the needs of companies, and as a result, Nanoelec/Easytech projects, evolved at Grenoble-INP?

Companies work with us on industrial projects in order to obtain POC (Proof of Concept) and, subsequently, functional demonstrators as part of product improvement or product development processes. It primarily deals with incremental innovation.

In 2020, technological areas such as embedded artificial intelligence and edge computing began to emerge. Projects also focus increasingly on safety and cybersecurity issues and take into account a secure-by-design approach.

What does the Nanoelec framework provide?

As part of the Nanoelec/Easytech →

program, projects benefit from the expertise and skills of Nanoelec partners. Startups, micro businesses and SMEs are backed by the Nanoelec ecosystem: a means to boost their R&D teams and ensure employee upskilling. The certification phase guarantees high-quality standards that provide solid foundations for the project.

In addition, the projects can count on the IRT's industrial know-how. To produce robust, simple, inexpensive demonstrators/proof of concepts, our laboratories often use mature technological components or building blocks, such as microcontrollers, sensors and actuators, and reusable wireless interfaces during the project's subsequent pre-industrialization process.

Can other Grenoble-INP Group entities carry out Nanoelec/Easytech projects?

In order to continuously and effectively meet the needs of companies, Grenoble-INP focuses on three areas : academic training of engineers, research and value creation. The primary goal is to provide support for innovation processes and collaborative R&D programs and make them readily available to startups, micro businesses and SMEs. With more than 20 years of experience at Esisar, it is safe to say that we have succeeded in creating innovation synergy within the regional ecosystem in order to drive company innovation. We are striving to increase these types of collaboration, in particular with Grenoble-INP Group research laboratories and technological platforms in order to profit from their wide range of competencies.

Finally, it is a means, for new generations of Grenoble-INP engineering graduates to become more familiar with tomorrow's environments such as startups, micro businesses and SMEs that provide growing employment opportunities. ■

KARIM CHIBANE,
Head of Technology Transfer at Esisar and
Head of the Grenoble-INP Easytech Initiative

Two of the 2020 projects carried out in Nanoelec/Easytech program aim to monitor odors and air quality
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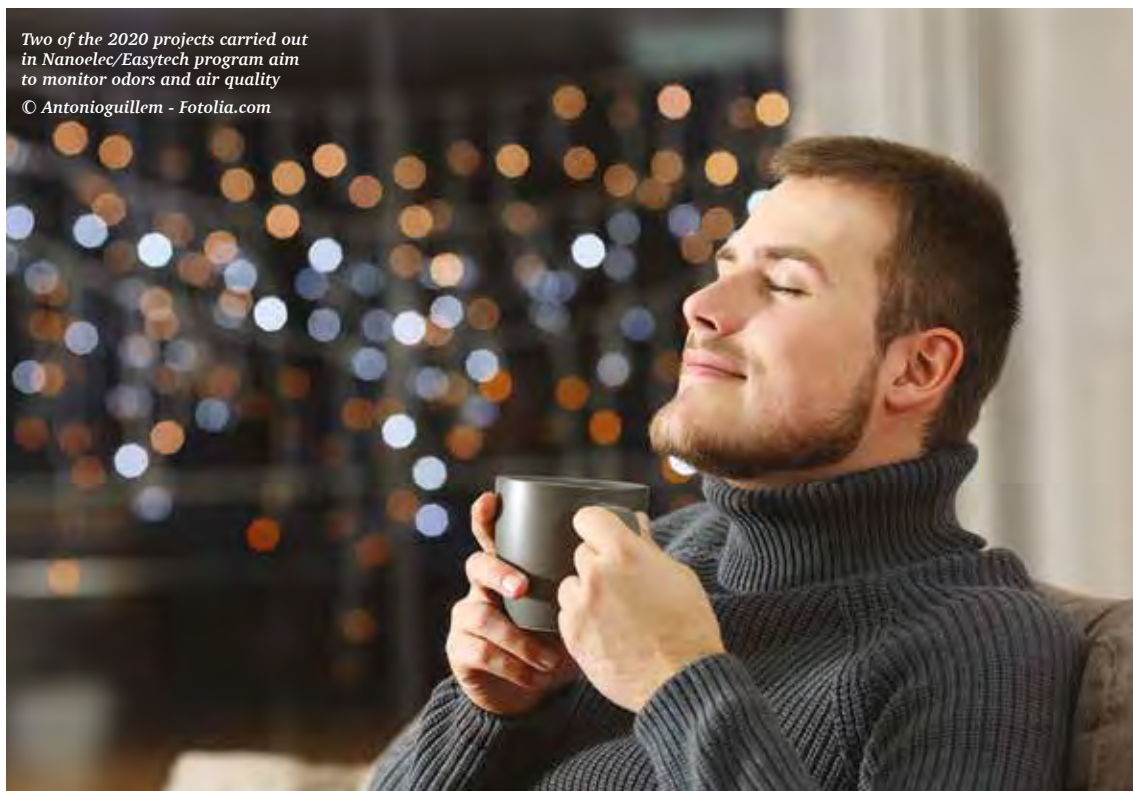
Embedded artificial intelligence

IRT Nanoelec tackles the topic of artificial intelligence (AI) from the perspective of embedded electronics. The development and expansion of embedded AI applications is triggered by the generation of large amounts of data that require local processing at component and system levels. The aim is to provide these components with the ability to make decisions in a more decentralized, autonomous and reliable manner.

Therefore, processing must be integrated close to the sensor in order to optimze the flow of data and to ensure that it remains undamaged and confidential.

This allows a good trade off between data flows from the sensor to the user, the related energy foo prints of both the sensor and the central computer handling reduced amounts of data..

The teams involved at Nanoelec mainly focus on image sensors and on the security of AI components and systems.

Smart Imagers

Imaging is one of the three main fields that use AI.

The aim is not only to achieve better image quality, but also to extract relevant data from the image, taking account of the environment, the object and the scene (potentially across a range of lighting conditions), and knowledge of the context. The main objective of the new Nanoelec/Smart Imager program is to evaluate the advantages of using 3D-stack technology to integrate the processing of artificial intelligence into the third layer of an image sensor.

The research teams focus on developing generic AI building blocks and the associated processing as well as on exploring the impact of these blocks on low-energy imager architectures. ■

Cyber-security of microcontrollers

Future connected objects will need reliable implementations of embedded AI algorithms and security mechanisms to protect them from potential software and hardware threats.

Securing the implementation of AI algorithms within these objects and the communications with the outside world is critical to the deployment and safe use of this technology in embedded systems. Researchers from academic labs as well as industrial teams are working together within the Nanoelec/Pulse program to make the implementation and deployment of AI algorithms, in particular machine-learning algorithms embedded in IoT components. Concerning the safety of autonomous vehicle, program teams are interested in the validation of artificial intelligence (AI) systems for mobility / vehicles. The question of evaluating and validating the effectiveness of these technologies is one of the last central issues delaying the adoption of embedded context capture technologies. It is therefore a major issue for the market access of autonomous vehicles. ■

Cytometry

Core partners of Nanoelec/Photonic Sensors program are participating in the European Neoteric project, which aims to design and build a cytometry demonstrator using photonic circuits.

Cytometry is a technique for the qualitative and quantitative counting and characterization of particles, molecules or biological cells in a fluid. Neoteric consists in demonstrating that a photonic circuit with learning functions (AI) can better perform image recognition of counted particles. Compared to conventional image analysis using deep learning software, silicon photonic technology promises an increase in frame rate, improved classification performance, and lower energy consumption by several orders of magnitude. ■

Processing characterization images

The development of deep learning algorithms and the use of artificial intelligence are of great interest for characterizing electronic components and systems.

In particular, these technologies will help improve the effectiveness of experiments conducted with large instruments available under the Nanoelec/PAC-G platform. These experiments generate very large data sets.
The pooled processing of data, metadata, simulations and images using AI in the associated images can accelerate convergence towards the development of required materials and aim at reducing the environmental footprint, ensuring supply sovereignty and operational reliability. ■

Application demonstrators for imagers

Teams involved in the Nanoelec/SystemLab initiative define, develop and test cases using embedded AI technologies that are integrated into or associated with image sensors.

The project aims to develop functional demonstrators and explore new applications scenarios. One of these use cases consists in positioning wireless image sensors in variuous natural environment to monitor fires or measure biodiversity, for instance. Another subject uses image sensors capable of analyzing human postures and expressions, with the aim of detecting emotions, to warn against the risks of reduced surveillance or prevent improper conduct. And a third use case will involve detecting obstacles, such as potholes and patches of ice for vehicles. ■

Learning IA on open hardware Risc-V

The Nanoelec/Human Capital and Training Design program led to a new training course on hardware-software codesign, thanks to the use of a free processor based on the Risc-V instruction set.

This instruction set and the processors implementing it are royalty-free and are increasingly used by the industry worldwide. In 2020, the teaching team at Grenoble-INP, again within the context of Nanoelec, developed a semi-generic reference platform based on Risc-V, designed a vision system embedded on FPGA and an FPGA for hardware processing of artificial intelligence algorithms. The combined software/hardware design, up to the actual prototype, allows the students to experiment with the respective advantages of these technologies (flexibility of software, efficiency of hardware) and to find a trade off between the two, within the same system. ■

Engaged in European space of R&D

A 100 kW motor inverter

For the purposes of the European H2020 ModulED (Modular Electrical Drivetrains) project, CEA has studied and built an inverter based on GaN/Si HEMT switches designed to supply a 6-phase motor with a peak power of 100 kW, which also entails switching 160 amperes in steady-state conditions.

The design, production and testing of the inverter power boards helped develop expertise in terms of the design stream for the GaN power boards and paralleling of GaN/Si switches in the particularly demanding environment of electrical vehicle applications.

Thanks to Nanoelec, teams from Siemens EDA and CEA are developing a digital twin of the moduled power board. Simulations are carried out with various digital design tools. They are compared with experimental data. ■

Exascale computing

Mont Blanc 2020 is a collaborative H2020 project which aims to define the architecture of a SoC (Silicon On Chip) processor in order to build a European low-consumption exascale machine by 2022 for high-performance computing.

With the support of Nanoelec, CEA is contributing to the project by providing real applications linked to the use of HPC infrastructure, the supply of various IP (communication, consumption management) and the final demonstration thanks to its hardware emulation infrastructure. The other French contributors are Kalray [1] and Bull, responsible for project coordination. ■

[1] French Deeptech resulting from a CEA spin-off which aims to make its mark with smart processors, a crucial technology for the data center, automotive, robotics, embedded AI and 5G markets

Cytometry

CEA-Leti and Prophesee, both partners in the Nanoelec consortium, are taking part in the Neoteric project.

Neoteric partners aim to develop a reconfigurable photonic circuit to detect cancer cells in a solution (cytometry-*presented in the AI chapter*). ■

Transceivers

The Masstart EU project will lead to the production of several Datacom and Telecom demonstrators.

It is focused on the development of advanced packaging and test methods for producing very high speed transceivers (800 Gbps and 1.6 Tbps), with reduced form factors (COBO type). CEA-Leti and Almae, partners in the Nanoelec consortium, are contributing to this project. A first generation of circuits was produced using the Silphide Design Kit developed within Nanoelec, and used by the partner Bright Photonics in its Nazca tool. ■

Packaging optoelectronic components

The purpose of Pixapp, standing for Photonic Integrated Circuit Assembly and Packaging Pilot line, is to set up a European platform for packaging photonic components.

It brings together 18 partners comprising photonic on silicon components manufacturers, component assembly specialists, systems assemblers, and players in the reliability field. Within Nanoelec, CEA-Leti is also a contributor. It focuses on demonstration of a self-assembly technique for micro-lenses on photonic on silicon components, in order to relax the optical alignment constraints between chips and fiber connectors, by shifting constraints to the precision of the photolithographic techniques. This packaging technological building block is generic and could be used for many applications. ■

Digitizing SMEs

DigiFed is run by Nanoelec through its founding partners, CEA and STMicroelectronics.
The aim is to demonstrate the potential of digital technologies in terms of hardware security, human-machine interaction, and autonomy for small and medium enterprises. DigiFed involves nearly 200 European SMEs in its innovation program. 80 of them can receive financial support and benefit from one of the DigiFed innovation channels. Half of them will be companies initiating their digital transformation. ■

Interoperability for IOT

The Brain-IoT project aims to establish a framework and a methodology for improved communication and cooperation between populations of heterogeneous IoT platforms which now interact closely with cyberphysical systems (CPS). CEA, UGA and STMicroelectronics are participants in this within Nanoelec. ■
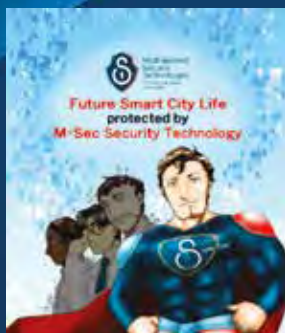
Secure architecture for smart cities

M-Sec published a 20-page comic strip to give you the opportunity to meet "security man", your new cyber hero!!
Nanoelec contributes to M-Sec, a #H2020-type Europe-Japan project, through CEA-Leti. Its goal is to achieve a proof-of-concept secure architecture for smart cities with two deployment sites, Santander in Spain and Fujisawa in Japan. Communication gateway security and security characterisations are carried out on the Nanoelec Product & Technologies Living Lab (PTL). ■

Elderly people

Focused on technologies to help seniors, Activage completed its fourth and final year of operation in 2020: deployment and evaluation of the home automation offer for home care for the elderly, the development of new interoperability and cybersecurity mechanisms. ■

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