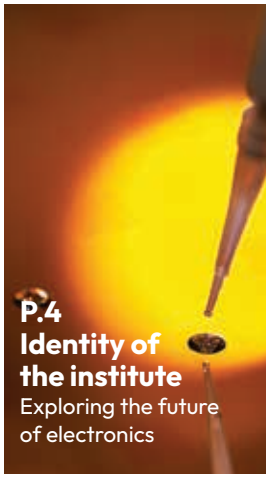
NANOELEC.

Scientific & technical highlights

2024 EDITION

AGENDA



Images & Photons

Smart imager

Displed

Photonic sensors

Digital trust

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Solutions for more secure digital components

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Correlative microscopy

Dissemination

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Responsible integration of digital devices in SME processes & products

Human capital & training design

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Sustainable development as a driver of innovation

Exploring the future of electronics

IRT Nanoelec runs multi-partner programs to make the electronics industry more competitive and greener, and thus contribute to the sustainable development of society.

The Nanoelec technological research institute (IRT) is a consortium of private and public sector players, hold by CEA. Our mission is to help companies create value and enable their products to stand out on the digital transition stage.

Nanoelec contributes to the competitiveness of the electronics industry, particularly in France. Based in Grenoble, the institute is a world-class hub for research, innovation and production in its field.

Our R&D programs are built jointly by representatives from the academic and industrial worlds. They deal with the design and development of new processes, systems and components in the following fields:

- photons & imaging: photonic sensors, new-generation displays and smart image sensors,
- digital trust: cybersecurity for connected objects, and characterization of components and systems by means of large instruments.

Nanoelec also runs engineering and technological dissemination training programs for SMEs with the support of the territorial public authorities. We implement open innovation techniques as well as more conventional technological development methods.

Given the pervasive nature of digital technologies, Nanoelec is in contact with actors from all sectors ranging from goods to services, industry, infrastructures, and consumer products, as well as transportation, environment and health.

Nanoelec is a member of FIT, a hub of technological research institutes (IRTs) and energy transition institutes (ITEs) set up by the French Government and financed by the invest plan for future (France 2030). The network of institutes was created to pool academic and industrial players who could run collaborative R&D and innovation projects aimed at boosting the competitiveness of the French economy. ◊

Photo
TEST OF A NEW COATING ON A SILICON WAFER
A.HAVRET/CEA

Microelectronics innovation

➔ Carry out world-class collaborative R&D in selected areas to produce innovative components and embedded systems: imagers, displays, photonic on Si and digital trust & security

➔ Develop and transfer these technologies to create the electronic circuits and components of the future

➔ Give industry players access to development, prototyping and advanced characterization resources

Technology dissemination

➔ Help businesses in the field of information and communication technologies meet the challenges of IoT through digital trust and security

➔ Provide expertise to help SMEs from various industrial sectors build new products and services with innovative components and embedded software

➔ Promote cooperation between SMEs, mid-caps and large companies

➔ Unveil new applications comprising environmental and social impact assessments by collaborative innovation

Development of human capital

➔ Attract young people to jobs in electronics that contribute to sustainable development

➔ Work with partners on parity and workplace equality

➔ Design training courses to meet current needs

➔ Anticipate future skill requirements in the sector: sustainability, cross-skills, social and professional communities for innovation

NANOELEC AT A GLANCE

A consortium of **22** **public & private members**
as of December 2023

247 patents and **57 software filed**
since 2012

704 **scientific** or **technical publications & communications**
since 2015

€52M **average annual budget**
Yearly average 2015-2023

324 **associated partners** including **245** SMEs
since 2012

213 **full-time jobs**
Yearly average 2015-2023

Trends notes on Nanoelec

by Sébastien Dauvé, Hughes Metras and Sandrine Maubert.

SÉBASTIEN DAUVÉ

DIRECTOR OF CEA-LETI AND PRESIDENT OF THE NANOELEC STEERING COMMITTEE

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Towards heterogeneous integration

By Sébastien Dauvé, President of the Nanoelec Steering Committee

Nanoelec has been active in the Grenoble ecosystem since 2012, and is your partner for boosting the competitiveness of reference players in the electronics sector. It represents an invaluable asset at a time when sovereignty and excellence are more than ever on the agenda in Europe.

The institute brings a strong capacity for acceleration on a selection of technological developments addressing highly specific medium-term challenges of interest to a large number of industrial partners. In so doing, Nanoelec supplements other France 2030 investments which notably addresses the development of FD-SOI technology, whether in Crolles for the industrial capability ramp-up, or at CEA-Leti for the FD10nm future generation.

For its future programs, the institute is thus actively positioned on heterogeneous integration, with the ability to contribute to a variety of applications markets, whether in the field of embedded computing, high performance computing, imagers, displays and telecommunications.

“Highly differentiating solutions for Nanoelec partners, on the road towards more responsible electronics.”

Heterogeneous integration is a technological solution that opens the door to efficiently embedding AI components. It is also possible to envisage more frugal manufacturing technologies and more repairable, recyclable and reusable components. This will enable highly differentiating technologies for Nanoelec partners on the road towards more responsible electronics.

This trend in the sector will require ambitious developments to meet the needs of industry and market. At stake are the sovereignty of the ecosystem, to ensure that Europe and France have the expertise needed for essential components and systems. ◊

HUGHES METRAS,
DIRECTOR OF NANOELEC

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Proven economic impact

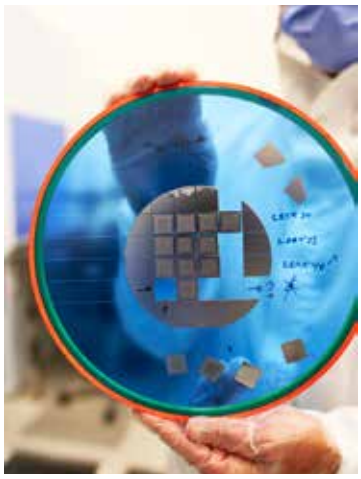
By Hugues Metras, Director of Nanoelec

In 2023, IRT Nanoelec continued to deploy the roadmaps defined for the period 2021-2025. We are expecting significant technological advances: hardware and software technology bricks for imagers, in particular with an event-based imager demonstrator, a technology demonstration to validate the feasibility of a novel concept for displays including tools for mass transfer of microleds, functional components for lidars using silicon photonic technologies, advances in the field of post-quantum cryptology, and security of neural networks embedded in components and systems.

In terms of economic impact, our partners move forward. STMicroelectronics is continuing to deploy its 3D integration technologies with new imager products; Prophesee has launched a new imager this year; Aledia has started to install its production lines in its plant near Grenoble and four companies accompanied by the Easytech initiative won first plant project awards[1]: Limatech, Dracula, CIXI and BeFC; these projects have all raised significant funds.

Our mission is to contribute to the competitiveness of the electronics sector. Beyond our technological R&D milestones, we are intensifying our commitment to questions related to human capital and to the responsibility of the sector. Since 2023, we have regularly taken part in the thematic working groups of the national industry's strategic committee on employment, training and eco-innovation. We are also continuing our commitment to debate and exert influence over questions of gender and professional equality. The institute is also moving forwards on the road to sustainable electronics: in 2024, our commitment to the Convention des Entreprises pour le Climat (Convention of businesses for the climate) will contribute to structuring roadmaps for the 2030 time-frame.

1. Under the France 2030 investment plan, the "First plant" call for projects aims to speed up the construction of pilot sites and/or industrial production by innovative start-ups, SMEs and mid-caps.



FIRST TOOLS FOR MICROLED MASS TRANSFER UNDER THE NANOELEC/DISPLED PROGRAM
© A.HAVRET/CEA 2024

2. Creations from students of the Brassart school with Schneider Electric, Teledyne E2V, Aniah, and the Dauphiné libéré newspaper, for the Tech&Fest 2024 festival.

Publications and communications were presented at high-profile conferences, including Display Week, Date, Risc-V EU, ECTC. Nanoelec was also behind the nationwide deployment of the Carac23 conference in close partnership with five other FIT institutes: Saint-Exupéry Railenium Supergrid, IPVF and Ines.2S.

Finally, to promote the image of our industry and make it more visible, Nanoelec was behind the *"Microelectronics for living in a better world"*[2] poster competition, with some entries being visible on the cover and throughout the chapters of this report. ◊

"We are firmly expecting significant technological advances: Embedded AI imagers, new concepts for displays, lidars using silicon photonic technologies, post-quantum cryptology, and secured AI embedded in components and systems."

SANDRINE MAUBERT,
DEPUTY DIRECTOR
OF NANOELEC
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Moving forward together to give meaning to our industry

Sandrine Maubert, Deputy director of Nanoelec

At the request of its industrial partners and further to a recommendation by the Government, Nanoelec is undertaking a large number of actions which fall under the United Nations sustainable development goals. We are aiming to combine our mission of technological innovation for competitiveness with the search for relevant and meaningful initiatives with our stakeholders in the light of the planet's finite resources.

The work of life cycle assesment in the R&D phase within the Displed project, the aim of which is to lay the groundwork for relocation of a display manufacturing industry to Europe, was the subject of a publication during Display Week 2023, a major event for the displays sector.

Eco-innovation assessments at the beginning of projects are being rolled out within the Easytech system with Minalogic. In this report, we present a selection of four of the most recent Easytech projects.
Through various European initiatives, we are looking at reducing electronic waste by addressing product end-of-life issues as of the design stage (EECONE project), the attractiveness of the industry for green electronics (GreenChip) and an ethical and sustainable approach to hardware technologies, whether for police investigations (Poliiice) or labor (Earashi).

Addressing challenges of sustainable development are among the key factors for the attractiveness of the industry. In 2023, Nanoelec and Minalogic co-organized the very first regional attractiveness forum for the electronic sector, which brought together 130 professionals from the industry, from training and from the institutional world, this was a way of answering the questions from students and young professionals in the sector. ◊

Four work areas for sustainable development in 2023

IRT Nanoelec launched a number of cross-cutting work actions in sustainable development, in response to the recommendations of our stakeholders. The IRT Nanoelec Sustainable Development action plan comprises four work areas.

2
OF THEM CONCERN **ECO-INNOVATION FOR R&D PROJECTS:**

→ **A quick and inexpensive diagnosis solution** for companies looking to run a project within the Easytech framework;

→ **An eco-innovation tool in the R&D phase** for the production sector of next-generation displays, currently under development with Aledia as part of the Displed program.

2
OF THESE WORK AREAS **CONCERN MANAGEMENT, SKILLS AND GOVERNANCE:**

→ **Events to promote greater gender equality** in the electronics sector;

→ **Design of training courses for sustainable electronics,** through the Human Capital and Training Design program.

"A competitive sector is one that satisfactorily manages its environmental and societal impact."

REGIONAL FORUM FOR THE ATTRACTIVENESS OF THE ELECTRONICS SECTOR, ORGANIZED BY NANOELEC AND MINALOGIC, ON MAY 11, 2023 IN GRENOBLE, UNDER THE AUSPICES OF SAMY SISAÏD, SUB-PREFECT AND COORDINATOR OF FRANCE 2030 AND THE INDUSTRIAL PROJECTS ACCELERATION PROGRAM
© P.JAYET/CEA 2023

Highlights

Attractiveness

FEBRUARY 3 | Webinar on the ninth-grade internships: How to spark interest in technology jobs with Schneider Electric and CEA.

© UTOPIKPHOTO

Smart Electronic for youth

FEBRUARY 9 | Webinar on the Smart Electronique platform, a learning kit for jobs in electronics developed for the CFS Electronique, with CEA and Acsiel.

JANUARY 2023

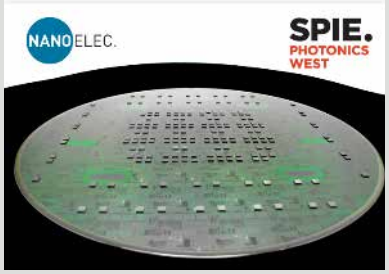
Sustainable Electronics

JANUARY 27 | Nanoelec/Human Capital & Training Design program conducted a seminar: "**Technology usages: how does sustainable development influence decision-making?"**
With contributions from Schneider Electric, Grenoble-Ecole de management, Grenoble-INP and CEA.

FEBRUARY 2023

Photonics West

FEBRUARY 1 | During his talk on next-gen photonics platforms for emerging applications, Bertrand Szelag, Integrated Photonics Program Manager @ CEA-Leti, presented III-V material integration on Si photonics platforms through direct bonding (wafer-to-wafer & die-to-wafer). As part of a Nanoelec initiative, the process is available for 200- and 300-mm wafers. It is CMOS-compatible and ready for large-scale integration.



MARCH 2023

On our business attractiveness

MARCH 2 | Seminar on the attractiveness of the microelectronics industry. Forty representatives from Nanoelec's core partners met for an initial collective discussion on commitment, education and recruitment.

International Women's Day

MARCH 7 | In association with Y.Spot and CEA, Nanoelec conducted a round table: "**How to attract innovative female talent?"** Participants included high-ranking women managers from CEA, GEM, HP France, Lynred, UGA & Nanoelec.

© P.JAYET/CEA

Photonic Sensors

MARCH 8 | CEA-Leti & Nanoelec booth at international Optical Fiber Communication conference (OFC), USA.

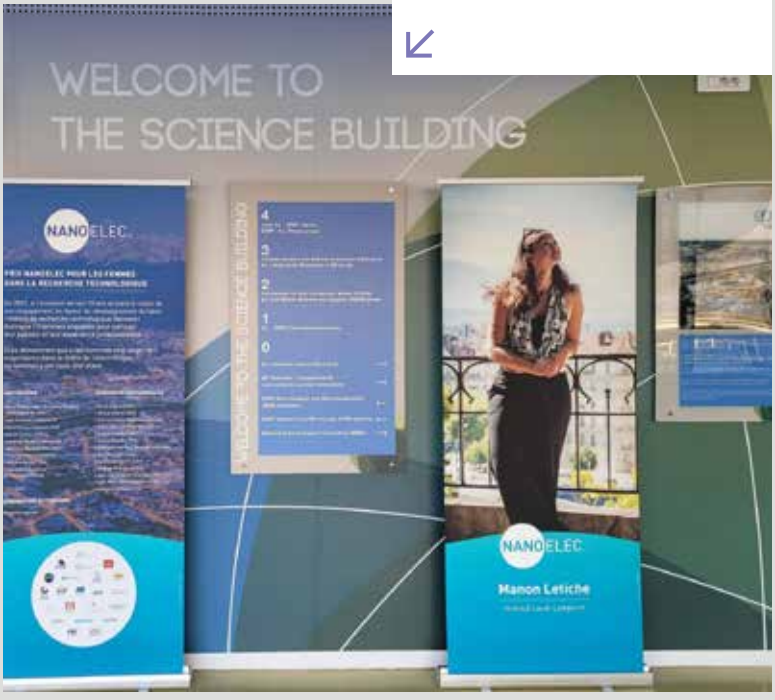
© DR

Territorial issues of attractiveness for the microelectronics

MARCH 17 | Webinar on the attractiveness of our region for the microelectronics industry, with Grenoble Alpes Métropole.

Women in Engineering

MARCH 27 | Nanoelec exhibition Women in Technological Research was presented at the Laue-Langevin Institute from March 27 to April 14.



APRIL 2023

Nanoelec ambassadors

APRIL 18 | Nanoelec exhibition Women in Technological Research was presented at the La Casemate, the center for scientific culture in Grenoble, from April 18 to May 30, as part of the 50 Audacieuses event.

3D integration: design & architecture

APRIL 19 | Annual workshop at the DATE international conference. Event-camera Dichotomy and the associated perspectives for Event-Graph Neural Networks.

System Lab

APRIL 26 | Colloquium on imagers, sports and health at CEA/Y.Spot (Grenoble).

MAY 23

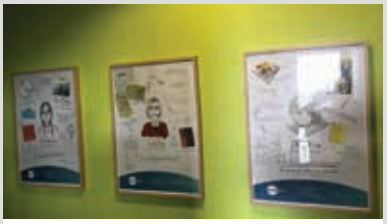
Industry attractiveness

MAY 11 | Local forum on the attractiveness of the microelectronics industry organized by Minalogic and Nanoelec.

© P. JAYET/CEA

TSV for an imager

MAY 30 | Test vehicle for recent progress in high-density TSV for 3-Layers CMOS image sensors presented at ECTC/IEEE Conference.



Nanoelec Ambassadors at La Casemate

MAY 30 | Portraits of Nanoelec women ambassadors by students from Pablo Picasso Middle School (Echirolles) were presented at La Casemate, the center for scientific culture in Grenoble.

JUNE 23

European Risc-V conference

JUNE 5 | Co-organization of European Risc-V conference (Barcelona). Intrinsically secure application processors and notably the CEA ScrambleCache demonstrator.

Addvisia

JUNE 6 | Webinar: Innovation Noon/CEA.

Observatory of Women Engineers

JUNE 23 | On the occasion of International Women Engineers Day, webinar on the Observatory of Women Engineers.

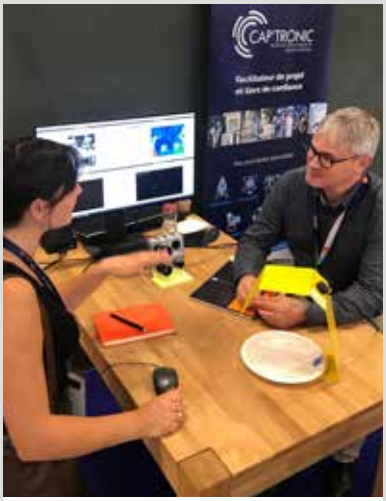
Leti Innovation Days

JUNE 27-29 | Three sessions of pitch forum for deeptech SMEs and startups.

JULY 23

Searching for talents

JULY 6 | Preview of the film "Microelectronics in search of talent" produced by DDETS.



SEPTEMBER 23

Sido Lyon

SEPTEMBER 20 | Partner with Minalogic at Sido Lyon; Addvisia demo on Captronic stand.

OCTOBER 2023

Addvisia at CCSTI La Casemate

OCTOBER 2 | Presentation/ demonstration of Addvisia at CCSTI La Casemate, on the occasion of the National Science Festival.

A view to a job in microelectronics

OCTOBER 19 | Round table at the Grenoble Career Forum, by the Grenoble Alpes Métropole regional authority, with Lynred, Soitec, SET, CEA, and the National Education authority.

NOVEMBER 2023

Irradiation

NOVEMBER 8 | Partner of G-RADNExt (Carac program).

A worldwide contest of hackers

NOVEMBER 10 | Partner of CSAW (the world's most comprehensive student-run cybersecurity event).

General Assembly

NOVEMBER 14 | General Assembly of Nanoelec (no-public).

Characterisation

NOVEMBER 21 | co-organization of a national workshop with the Railenium and Saint Exupéry IRT and the IPVF, Supergrid Institute and Ines.2S ITE, on the occasion of the FIT annual press conference.

Orientation Night

NOVEMBER 24 | Orientation Night of the Grenoble Chamber of Commerce and Industry, with UGA, Aledia, CEA, Grenoble INP-UGA, Siemens EDA.

Quantum Computing at the High-Level Forum

NOVEMBER 26 | Partner of the High-Level Forum (non-public); participation in the round-table on quantum computing.

DECEMBER 2023

The Convention of Companies for Climate

DECEMBER 5 | Webinar presenting the Convention of Companies for Climate, in the context of the microelectronics sector.

JANUARY 2024

Nanoelec at the Grenoble City Center

JANUARY 19 | Exhibition of the Nanoelec Ambassadors at the Grenoble Alpes Tourist Office.

FEBRUARY 2024

Tech&Fest

FEBRUARY 1 | Poster Contest: Microelectronics for a better World with Schneider Electric, Aniah & Teledyne E2V.

MARCH 2024

More women in the electronics industry

MARCH 8 | Round-table on International Women's Day.

APRIL 2024

Nanoelec ambassadors at STMicro-electronics

FROM APRIL 2 TO MAY 24 | Nanoelec exhibition at STMicroelectronics Crolles and STMicroelectronics Grenoble.

MAY 2024

3-layer integration

MAY 27 | Wafer level Face-To-Back (F2B) 3D integration and operational 3-layer test vehicle presente at ECTC/IEEE Conference.

From 3D integration to images

A view to a single chip with small form factor and enhanced electrical performance.

Progress in the semiconductor industry is divided into two classes: Moore's Law, where chips are manufactured with advanced technologies of 16 nanometers and smaller (this is the case for the processors at the heart of smartphones, tablets, PCs, and servers), and the More than Moore's approach, which uses mature manufacturing technologies of 20 nanometers and larger (this is the case for most components such as microcontrollers, power management circuits, sensors, power electronics, and radio-frequency circuits).

As the microelectronics industry continues to face challenges to further miniaturize components, according to Moore's Law, the More than Moore approach is also becoming more widespread. 3D integration technology has emerged in the last decade as a key process to combine multi-functional and technological integrated circuit devices to produce a single chip with small form factor and enhanced electrical performance.

AN OVERALL APPROACH COMBINING TECHNOLOGY AND DESIGN

At CEA-Leti, through Nanoelec, we are building on 10 years of R&D on three-dimensional architectures, which now enables us to address very ambitious applications prospects. 3D integration, which consists in interconnecting electronic chips in three dimensions, is a promising solution for addressing the growing need for functionality, density and performance in future integrated circuits.
However, to allow the rapid emergence of this technology in industry, an overall approach is needed, taking account of technological development and the design of new circuit architectures, the development of design and testing tools, as well as reliability.

CHALLENGES IN HYBRID BONDING

From 2012 to 2020, the academic and industrial teams working under the Nanoelec/3D Integration program focused on developing a comprehensive platform compatible with the full design cycle of new products. They dealt with technology for wafer-to-wafer or die-to-wafer hybrid bonding, but also design, electronic design automation (EDA) tools, testing and reliability.

"The hybrid bonding technology, one of the various 3D stacking options, is suited to advanced device miniaturization with the possibility of reducing the hybrid bonding pitch below one micrometer", says Bassel Ayoub introducing his thesis report prepared at STMicroelectronics and CEA-Leti within Nanoelec[1]. He considered the impact of such aggressive interconnection pitch scaling on the thermomechanical stability, the electrical performance and the reliability of the hybrid bonding level applied to the domain of Smart Image Sensors. In particular he led Laue-microdiffraction studies with the unique synchrotron beam at the ESRF for Cu/SiO2 hybrid bonding integration. Highlighting a profound understanding of the interface robustness and reliability, he demonstrated –in the frame of Nanoelec- high reliable Cu/SiO2 hybrid bonding integration for pitch down to 0.8 µm as well as for hybrid bonding pad width reduced to 0.35µm, in the case of consumer application. New architectures allowing enhanced electrical performances with pitch reduction are now available. ◊

1. Ayoub, B. (2023). Electrical and morphological characterizations of the hybrid bonding level down to submicron pitches. Bordeaux.

Three-layer integration breakthrough for AI-embedded CMOS image sensors

ERIC OLLIER

PROJECT MANAGER
AT CEA-LETI AND DIRECTOR
OF NANOELEC/SMART IMAGER
PROGRAM

In the frame of Nanoelec, CEA-Leti scientists reported a series of successes in three related projects that are key steps to enabling a new generation of CMOS image sensors (CIS) embedding AI from imaging to vision.

The aim of IRT Nanoelec's Smart Imager program is to develop the technologies needed for the next generation of imagers, which will allow the transition from image generation to analysis of the information included in these images, on the very sensor itself, in order to perceive a scene, understand the situation and intervene on it. This transition represents a very real disruption and a paradigm shift, with computing and memory issues becoming preponderant, in addition to image generation. This revolution implies the use of artificial intelligence on the image sensor itself.

The consortium's goal is to develop 3D stacking technologies in order to implement artificial intelligence functions on the sensor itself. This is why we are working both on the components and on the software, to transition our image sensor concepts from image generation to data generation, enabling a situation to be analyzed.

In 2023, work continued on the development of key technological building blocks: hybrid bonding, high density TSV (HD-TSV), heterogeneous integration and specific technologies for infrared applications. The main result is the very first demontration of the 3-layer stacking integration at CEA-Leti, through a functional test vehicle combining hybrid bonding in face-to-face & face-to-back configurations and HD-TSV, with functionality being verified via morphological and electrical characterizations. In addition, innovative architectures have been proposed for future visible & event-based smart image sensors.

Our program is very close to two other activities at Nanoelec: the System Lab initiative, searching for new multi-spectrum imaging applications, and Displed. We work on simulation & design tools for hybrid bonding components and technologies for 3D architectures.

TEST CHIPS ARE PREPARED FOR TRANSFERT
© A.HAVRET/CEA

SMART IMAGER PROGRAM AT A GLANCE

→ VISION

The transition from imagers to vision sensors is generating new market opportunities

→ AMBITION

To provide key hardware and software building blocks, to validate them through demonstrations ranging from test vehicles and proofs of concept to the prototyping of a smart, multi-layer imager

→ MISSION

Stacking/3D technologies, embedded AI and data management, New architectures

→ PARTNERS

CEA
Grenoble INP-UGA
Lynred
Prophesee
Siemens EDA
STMicroelectronics

Above, to the left
TRINAMIX, VISIONOX AND STMICROELECTRONICS PRESENT COST-EFFICIENT, SECURE FACE AUTHENTICATION SYSTEM FOR BEHIND-OLED INTEGRATION IN SMARTPHONES
© STMICROELECTRONICS

Above, to the right
A NEW GENERATION OF EVENT-BASED SENSOR FEATUREING SOME OF THE WORK LED IN THE FRAME OF NANOELEC/ SMART IMAGER PROGRAM
© PROPHESEE

STMICROELECTRONICS

New products being manufactured

Four new products designed in 2023 and based on 3D stacking technologies could rapidly be appearing on the image sensors market.

"The benefits of the approach developed by the teams involved in Nanoelec are still reduction in chip size, performance and consumption gains", says Eric Mazaleyrat, Technology watch and innovation director at STMicroelectronics. ◊

PROPHESEE

A frugal neuromorphic sensor for the IoT

The industrial version of the GenX320 product was officially launched in October 2023. *"This is our fifth generation sensor"*, says Luca Verre, co-founder of Prophesee. *"It is both highly efficient in terms of energy consumption and the smallest neuromorphic sensor[1] in the world."* This sensor is being used in AR/VR, for example in ultra high-speed, low energy eye tracking or hand tracking applications for headsets. *"With this new product, which features some of the work led with our partners from the Nanoelec/Smart Imager program, Prophesee intends to expand its market to more mass consumer markets such as IoT after having already demonstrated significant traction in the industrial automation market"*, explains Luca Verre.

GENX320, which already received 4 Award, including at CES 2024, *"opens the door to integration of this technology into connected devices, whether or not portable, used in low-light environments and incorporates artificial intelligence algorithms"*, notes the specialist site L'Embarqué. ◊

1. Event-based sensors, also known as neuromorphic vision sensors, consist of asynchronous pixels which react to changes in brightness with a far higher temporal dynamic than conventional imagers.

ARCHITECTURE & APPLICATIONS

Lightweight event stream classification

81% REDUCTION IN THE NUMBER OF CALCULATION OPERATIONS PER SECOND COMPARED TO THE STATE-OF-THE-ART.

Event camera pixels efficiently encode visual information through triggered events, offering advantages in temporal resolution, dynamic range, and data sparsity. In 2023, several results produced within the framework of Nanoelec supported Prophesee's core technology, while the company received an award for its 5th generation sensor at CES 2024. *"However, the optimal machine learning method for leveraging these characteristics remains unclear"*, said Thomas Mesquida, as first author of a study bringing together scientists from CEA and Prophesee presented at the 34th British Machine Vision Conference[2]. *"Existing approaches often convert events into 2D frames, losing crucial time-domain information"*, adds Thomas.

A promising alternative is event-graph neural networks. However, they suffer from computational intensity and limited temporal dependencies. As a solution, the study proposes combining the recent method of the HUGNet lightweight event-graph neural network with gated recurrent units to model temporal dependencies

Below and next page,
THOMAS MESQUIDA & SÉBASTIEN THURIES, ENGINEERS AT CEA-LIST, DURING A CREATIVE SESSION FOR OPTIMIZATION OF THE 3 LAYERS ARCHITECTURE FOR THE SMART IMAGER

2. Mesquida, T., Dampfhoffer, M, Dalgaty, T., Vivet, P., Sironi, A., & Posch, C. (s. d.). G2N2: Lightweight Event Stream Classification with GRU Graph Neural Networks. BMCV, Aberdeen, UK

A new event-data augmentation technique that boosts the performance of both event-graph and convolutional neural networks.

between the features extracted by HUGNet. *"Relative to the previous state-of-the-art in event-graphs, we reduce event-graph update latency by more than four orders of magnitude and reduce the number of neural network calculations per second by 70× while predicting optical flow more accurately[4]. In some cases, we also find that, relative to convolutional models, the number of operations per second was reduced by 81%"*, says Christoph Posch, Co-Founder and CTO at Prophesee.

Furthermore, the team introduced a new event-data augmentation technique that boosts the performance of both event-graph and convolutional neural networks on this task by up to 7.4%.

"Future work will focus on exploring alternatives to GRU task heads[3] to achieve lightweight and ultra-low latency implementation without relying on frame buffering", Thomas says.

At the DATE Conference 2023 in Antwerp (BE), the same team discussed the CNN vs. SNN Event-camera Dichotomy and the associated perspectives for Event-Graph Neural Networks[5] to again enhance performance and frequency response and reduce energy consumption. *"The latter is of particular importance since these algorithms will typically be employed near or inside the sensor at the edge where the power supply may be heavily constrained"*, points out Christoph Posch. ◊

3. Dalgaty, T., Mesquida, T., Joubert, D., Sironi, A., Vivet, P., & Posch, C. (2023). HUGNet : Hemi-Spherical Update Graph Neural Network applied to low-latency event-based optical flow. 2023 IEEE/CVF Conference on Computer Vision and Pattern Recognition Workshops (CVPRW), 3953-3962. https://doi.org/10.1109/CVPRW59228.2023.00411

4. The GRU (Gated Recurrent Units) are parts of neural networks. The first part of the network (the backbone) extracts and analyses information, while the end of the network (the task head) creates a dedicated application using the extracted data.

5. Dalgaty, T., Mesquida, T., Joubert, D., Sironi, A., Soubeyrat, C., Vivet, P., & Posch, C. (2023). The CNN vs. SNN Event-camera Dichotomy and Perspectives For Event-Graph Neural Networks. 2023 Design, Automation & Test in Europe Conference & Exhibition (DATE)

ARCHITECTURE & DESIGN

Efficient in-sensor processing based on advanced 3D technologies

A CEA-LIST TEAM INVOLVED IN THE NANOELEC/SMART IMAGER PROGRAM MAKES A YEARLY CONTRIBUTION TO THE ORGANIZATION AND CONTENT OF AN INTERNATIONAL WORKSHOP ON THE CHALLENGES OF HETEROGENEOUS 3D ARCHITECTURES AND SENSORS, AT THE DATE CONFERENCE.

"The 2023 edition attracted close to 50 experts in Antwerp (BE). AI, Quantum Computing as well as the Risc-V open standard instruction set architecture were discussed", says Pascal Vivet (CEA-List), as first member of the workshop organizing committee, and contributor to the Nanoelec/Smart Imager program.

"3D integration is THE technology for highly integrated image sensors", Sébastien Thuries (CEA-List), who also works at the Nanoelec/Smart Imager program, stated at the workshop. During the presentation at DATE, he pointed out two breakthroughs thanks to 3D heterogeneous integration: *"First, we can stack the backside Imager; secondly, we can combine a 3-layer imager with a CNN near sensor and an event-based sensor"*, he explains.

The 2024 edition of the DATE workshop focused on heterogeneous integration which *"enables larger system level integration and improves PPAC figure of merit "*, as pointed by Tony Mastroianni, Advanced Packaging Solutions Director at Siemens Digital Industries Software, in his talk.

Starting from the design & verification challenges of the Active Interposer 96-core Architecture developed by CEA within Nanoelec, Tony Mastroianni detailed a System Technology Co-Optimization strategy. *"3D IC ecosystem requires open standards and formats, support for multi-domain design, as well as marketplace including a rich library of reusable chiplet components and broad industry & government adoption"*, he concludes. ◊

TARGETING NEW MARKETS

Infrared opting for 300mm

3D STACKING TECHNOLOGIES COMBINED WITH THE POSSIBILITY OF FABRICATION ON 300MM SILICON WAFERS ENABLES THE INFRARED IMAGING MARKETS TO BE EXPANDED, FOR EXAMPLE TO PEDESTRIAN DETECTION FOR THE AUTOMOTIVE INDUSTRY.

Infrared represents a broad technological spectrum and numerous applications in highly diverse industrial sectors, from space imaging to thermography, to defense and autonomous vehicles. As a specialist in this field, Lynred is involved in two Nanoelec programs. *"With Smart Imager, we are addressing major technological challenges for the medium/long term: we envisage that 3D stacking technology and the associated architectures will appear in our products by the 2030-2035 timeframe."*

For that purpose, Nanoelec/Smart Imager will first investigate different technological options for infrared to access 300mm CMOS nodes, explains Sébastien Cortial, Senior Expert at Lynred. *"In addition, the Nanoelec/System Lab initiative enables us to continue the process with research opening up new applications possibilities, which these technological advances are making possible."*

"A number of Nanoelec/Smart Imager program results in 2023 are contributing to strengthening our roadmap", explains Xavier Brenière, head of the application laboratory at Lynred. ◊

With hybrid bonding (HB) pitch reduction, many challenges are arising.

Photos of the double page,
IN THE CEA-LETI CLEAN ROOM, PIERRE MONTMEAT ET MÉLANIE VACON, ENGINEERS AT CEA, BEING ABOUT TO START AN HYBRID BOUNDING PROCESS ON EVG TOOL
© A.HAVRET/CEA 2024

SILICON TECHNOLOGICAL DEVELOPMENTS

Hybrid bonding pitch reduction

IN ADDITION OF BASSEL AYOUB'S PHD, A TEAM FROM STMICROELECTRONICS AND CEA-LETI GATHERED IN NANOELEC/SMART IMAGER PROGRAM, PUBLISHED NOT LESS THAN SEVEN PAPERS IN 2023 ON RELIABILITY OF THE CU/SIO$_2$ HYBRID BONDING INTERFACE.

With hybrid bonding (HB) pitch reduction, many challenges are arising. One of them is related to the reliability of HB-based interconnects and in particular the thermomechanical stability of the Cu/SiO_2 hybrid bonding interface and its electromigration performances as electromigration (EM)-related degradation is intimately linked to the electrical current in addition to temperature and mechanical stresses. During 2023, at four IEEE International Conferences[6], Sandrine Lhostis (STMicroelectronics) and Stéphane Moreau (CEA-Leti) together with scientist from IMS Laboratory (University of Bordeaux), reported recent advances on qualification and reliability of Cu/SiO_2 to Cu/SiO_2 hybrid bonds for 3D ICs. *"High robustness is validated to all the standard reliability tests within the specifications for consumer applications for bonding pitch down to 0.81 µm. Compared to standard BEoL interconnects, few differences are observed: modification of the TTF dependency behaviour at low electrical field, and new failure mode in electromigration for small bonding pads width"* says Sandrine Lhostis, engineer at STMicroelectronics.

"For EM-related failures in HB-based interconnects when decreasing the interconnect pitch from 6.84 down to 1.44µm, the weakest link moves from the BEOL levels to hybrid bonding

6. International Interconnect Technology Conference (IITC), the Reliability Physics Symposium (IRPS), European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF) and Electronics Packaging Technology Conference (EPTC).

ones, without affecting the projected performance under use conditions. Additional studies done on design aspects do not evidence any negative impact on the electromigration resistance of the HB brick", explains Stéphane Moreau, research engineer at CEA-Leti.

"As pitch reduction tends to submicronic size pads, their microstructure moves from a polycrystalline one to a monocrystalline one", underlines Bassel Ayoub, co-author of the four communications, now engineer at STMicroelectronics. As a teaser for future studies, their talks at IRPS and IITC-MAM pointed out few hot questions that *"have to be investigated in a near future as dimension shrinkage"*, like : *"is there any new failure mechanisms, especially EM-related below 1 µm pitch? Is there any additional effects stress for die-to-wafer integration"*? ◊

TEST CHIPS & PERFORMANCE ASSESSMENT

Achieving 3-layer stacking integration for future smart imagers

FOR THE NEEDS OF THE NANOELEC/SMART IMAGER PROGRAM, A CEA-LETI TEAM DEMONSTRATES WAFER LEVEL FACE-TO-BACK (F2B) 3D INTEGRATION. YEAR ON YEAR, THEY IMPROVE THEIR PERFORMANCE IN COMBINING FINE PITCH CU-CU HYBRID BONDING WITH HIGH-DENSITY CONNECTORS UP TO AN OPERATIONAL 3-LAYER TEST VEHICLE.

We reached 100% connection yield through hybrid bonding and TSV.

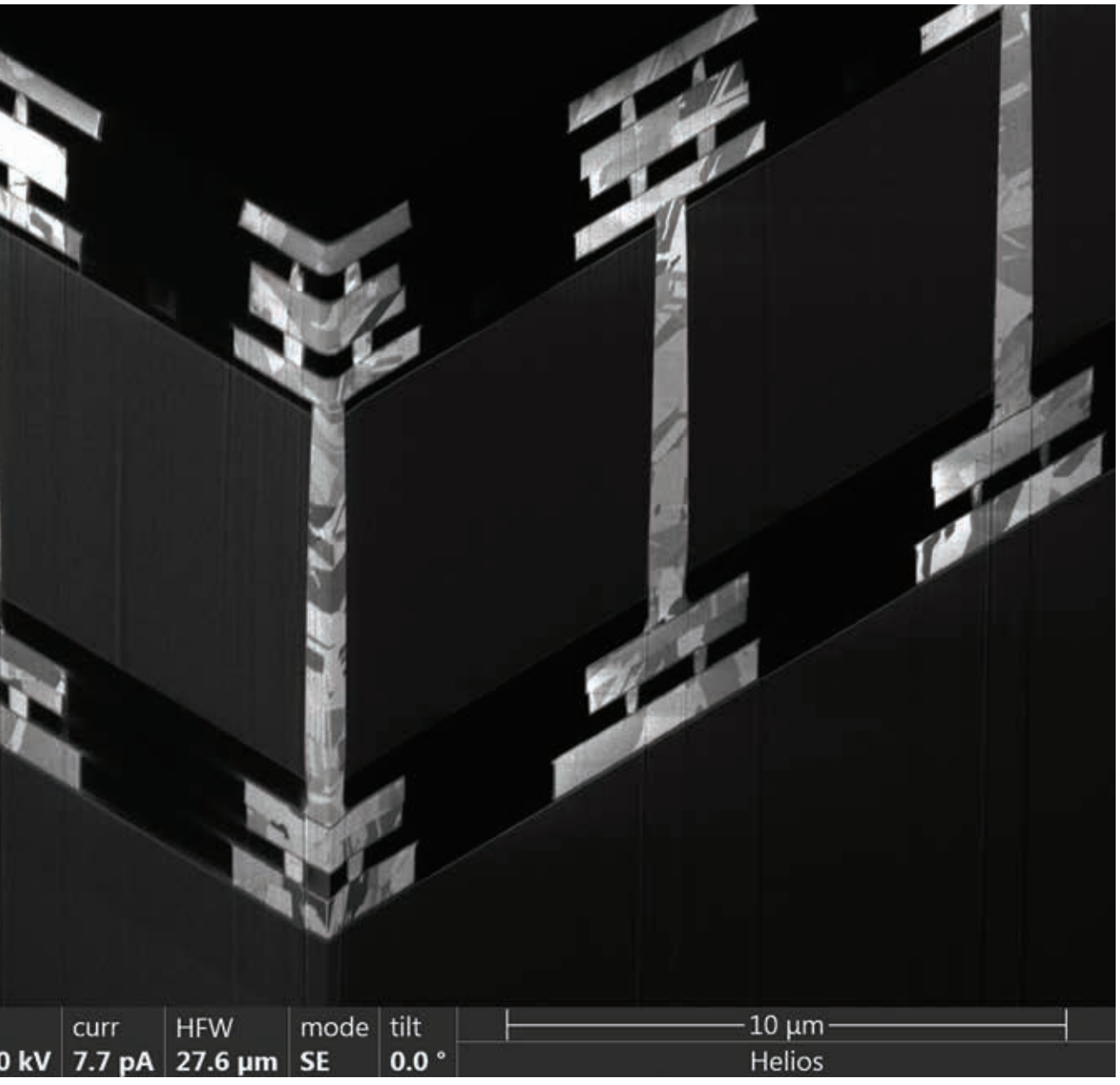
3D stacks offer multiple advantages for advanced components such as smart imagers and their assembly in a wafer-to-wafer (W2W) approach opens up access to very fine pitch interconnections. While hybrid bonding is commonly used to connect the layers, high-density (HD) TSV are mandatory for the signals to be transmitted through them.

For several years now, a CEA-Leti team has focused on the key enabling technology of TSV for the 3-Layer CMOS image sensors under development at Nanoelec, and every year publish several papers to report on their progress at the international ECTC conference.

"HD TSV technology was transposed from a stack with a 9 µm-thick substrate to a thinner stack with only 5 µm of silicon", reports Stephan Borel[7]. The improvement of the thinning process by using a more recent and more efficient grinding tool reduced the TTV (Total Thickness Variation) around 1 µm. *"We reached 100% connection yield through hybrid bonding and TSV. At the same time, we optimized the TSV by upgrading the materials and processes for even higher performance"*, he adds.

On the right,
AT THE IEEE 74TH ELECTRONIC COMPONENTS AND TECHNOLOGY CONFERENCE (ECTC 2024, DENVER, COLORADO, MAY 28 – 31, 2024), CEA-LETI DEMONSTRATES FEASIBILITY OF COMBINING HYBRID BONDING AND HIGH-DENSITY THROUGH-SILICON VIAS. THESE DEVELOPMENT ARE CONDUCTED TO MEET THE NEEDS OF THE NANOELEC/SMART IMAGE PROGRAM. FIB-SEM 3D CROSS-SECTION OF THE 3L TV STRUCTURE: THE PITCH IS 6µM FOR THE BONDING PADS; AND THE HD TSVS DIMENSIONS ARE 1X10µM

7. "Low Resistance and High Isolation HD TSV for 3-Layer CMOS Image Sensors", S. Borel & al., ECTC 2024 TO BE PUBLISHED


curr
HFW
mode
tilt
0 kV
7.7 pA
27.6 µm
SE
0.0 °
10 µm
Helios

Below,
CROSS-SECTIONAL SEM MICROGRAPHS OF HD TSV IN A DENSE ENVIRONMENT. HD TSV DIMENSIONS ARE 1µm IN DIAMETER AND 10µm IN HEIGHT
© CEA

On the right,
AT CEA-LETI CLEANROOM, THE MACHINE USE FOR CMP PLANARIZATION
© AUBERT/CEA

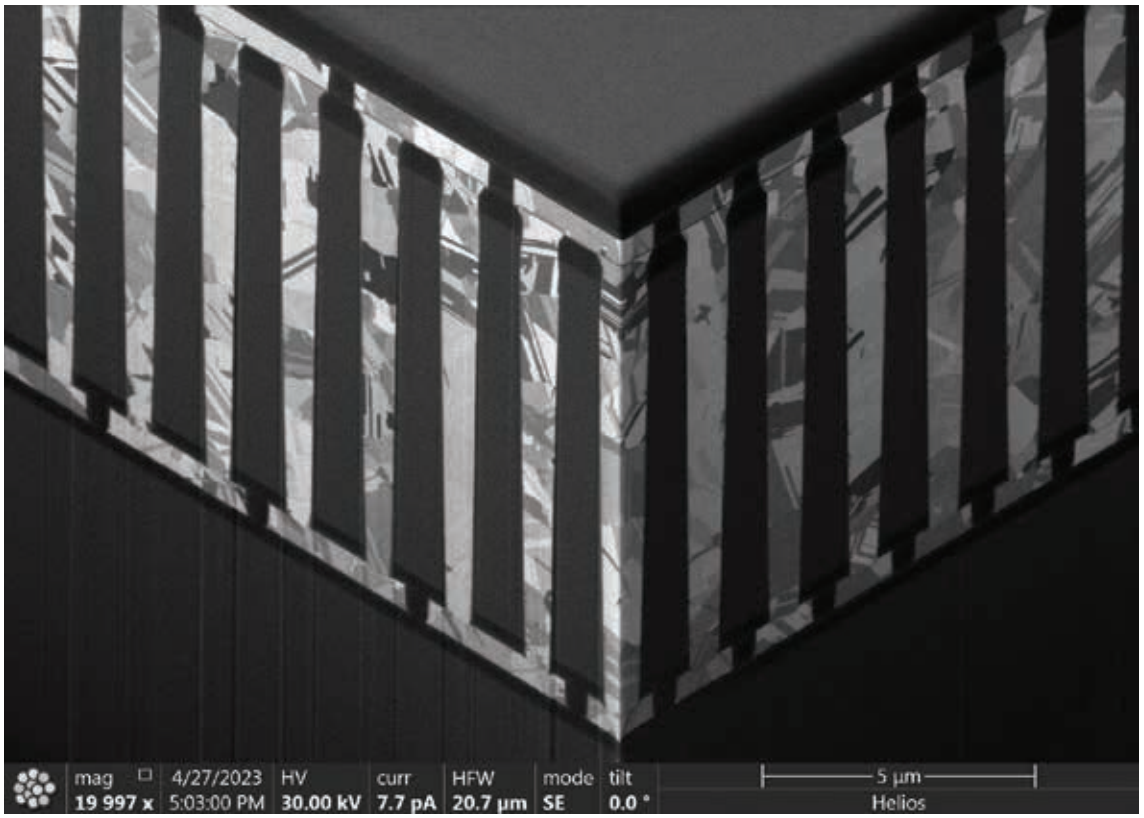
8. "Backside Thinning Process Development for High-Density TSV in a 3-Layer Integration", R. Bouis & al. ECTC 2024 TO BE PUBLISHED

9. 3-layer Fine Pitch Cu-Cu Hybrid Bonding Demonstrator With High Density TSV For Advanced CMOS Image Sensor Applications, S. Nicolas & al., R. Bouis & al. ECTC 2024 TO BE PUBLISHED

The HD TSV technology roadmap entails lower silicon thickness to improve performance. Focusing on the backside thinning flow (grinding, CMP, metrology) for TSV depths of 6µm or less, the same team implemented stringent process control from grinding to CMP finishing, to obtain remarkably low silicon total thickness variations below 1µm. *"Our work opens up prospects for lesser silicon thicknesses (<5µm) and paves the way for industrial implementation"*, says Renan Bouis[8].

By means of gradual progress, the team presented a 2-Layer Face-To-Back (F2B) test vehicle (TV) at the ECTC 2023 Conference that they had already demonstrated the previous year. *"And now, we unveil the next level of integration by achieving a 3-layer TV with fine-pitch Cu-Cu hybrid bonding (HB) technology and high density (HD)"*, says Stéphane Nicolas[9] at the ECTC 2024 edition. Their most recent TV has hybrid bonding pad dimensions of 3µm and 2 µm along with standard pitch (6 µm) and fine pitch (4µm) respectively.
HD TSV dimensions are 1µm in diameter and 10µm in height.

"Our next step will be to implement this 3D technology in a functional advanced CMOS image sensor", adds Stéphane. ◊



DESIGN TOOLS

An imager built on a disruptive 3-layer architecture

ONE OF THE MAIN CHALLENGES OF THE NANOELEC/SMART IMAGER PROGRAM IS TO EMBED THE POWER OF AN AI ALGORITHM DIRECTLY UNDER AN IMAGE SENSOR IN A CONSTRAINED, LOWPOWER ENVIRONMENT.

The Nanoelec/Smart imager sensor architecture has been defined this year: it includes a layer of image-sensitive pixels, a layer combining analog reading of the image and pre-processing of the digitized pixels, and a third layer dedicated to the hardware and software deployment of artificial intelligence (AI) functions.

To speed up the design, simulations and functional verification of the AI layer and the entire architecture, Siemens EDA teams have implemented four of their software tools: Catapult, Questa, Symphony and Tessent.

In a communication at the Chiplet Summit (January 2023, USA), scientists from Siemens EDA and CEA-Leti presented a warpage simulation methodology for assessing chip-package interaction in chiplet-based 3D stacks[10]. *"Combining simulations with layout analysis capabilities allows obtaining Chip-Package Interaction stresses with any desired resolution, by applying multi-scale simulation technique. The study demonstrates that, for the purpose of mechanical failure analysis in the early stage of a package design, the warpage measurements can be used for the tool's calibration"*, summarizes Jun-Ho Choy, engineer at Siemens EDA in Fremont (CA, USA) as the first author of the study rolled out for the needs of Nanoelec.

Data from simulations from a recently proposed methodology for electromigration (EM) assessment in an on-chip power/ground grid of integrated circuits were compared with physical measurements on dedicated test grids, through Nanoelec[11]. *"We set two different test vehicles on electrical and temperature characterization protocols. The existing current distributions resulted in different behavior of electromigration-induced failures in these nets: a gradual voltage evolution in the power net, and sharp changes in the ground net were observed in the experiment, and successfully reproduced in simulations"*, reports Armen Kteyan, engineer at Siemens EDA in Yerevan (Armenia). ◊

10. Choy, J.-H., Sukharev, V., Kteyan, A., Moreau, S., & Brunet-Manquat, C. (2023, January 24). Warpage simulation methodology for assessing chip-package interaction in chiplet-based 3D stacks. Chiplet Summit, San Jose, California, US

11. Kteyan, A., Sukharev, V., Volkov, A., Choy, J. H., Najm, F. N., Yi, Y. H., Kim, C. H., & Moreau, S. (2023). Electromigration Assessment in Power Grids with Account of Redundancy and Non-Uniform Temperature Distribution. Proceedings of the 2023 International Symposium on Physical Design, 124-132.

DESIGN TOOLS

Bridging the gap between neural network exploration and hardware implementation

AT THE 60TH DESIGN AUTOMATION CONFERENCE (DAC 2023), A TEAM FROM SIEMENS EDA AND CEA-LIST UNDERLINED THE ISSUES OF THE HARDWARE DESIGN CYCLE IN THE FAST GROWING RESEARCH TOPIC OF AI DEEP LEARNING(12).

"Hardware designers struggle to master all algorithmic optimizations", points out Nermine Ali, research engineer in embedded AI at CEA-List, as contributor to the Nanoelec/Smart Imager program. *"We have to cope with the increasing complexity of the design cycle and multiplying constraints like real-time constraints, memory and power constraints, etc."*, she adds.

The team proposed a new N2D2 Catapult-Stream export that has the potential to become a leading high level synthesis generator for large CNN networks. *"Fully automatic generation is ongoing, for full compatibility of C++ export with Catapult"*, underlines Ronan Poirier, Application Engineer at Siemens EDA, also involved in the program. ◊

Below,
RONAN POIRIER (SIEMENS EDA) & NERMINE ALI (CEA-LIST) PRESENTING THEIR COLLABORATION AT NANOELEC GENERAL ASSEMBLY 2023
© P.JAYET/CEA 2023

12. Ali, N., Szczepanski, M., Pajaniradja, S., & Vivet, P. (2023, June 9). Bridging The Gap Between Neural Network Exploration And Hardware Implementation with N2D2 & HLS. 60th Design Automation Conference (DAC 2023), San Francisco, USA.

ONE OF THE EIGHT POSTERS ON THE TOPIC **"LA MICROÉLECTRONIQUE POUR VIVRE DANS UN MONDE MEILLEUR"** (MICROELECTRONICS FOR LIVING IN A BETTER WORLD) CREATED BY THE STUDENTS OF THE BRASSART-GRENOBLE SCHOOL FOR TECH&FEST 2024.
POSTER BY AMBRE FENIX, "GRAPHIC CREATION" STUDENT

Displed

Towards a renewal of display technology in Europe

FRANÇOIS TEMPLIER
PROGRAM MANAGER FOR DISPLAYS AT CEA AND DIRECTOR OF THE NANOELEC/ DISPLED PROGRAM

MicroLED technology is bringing about a revolution in the field of displays, by providing outstanding image quality and immersion capability, for display sizes ranging from smart-phones to large TVs.

The IRT Nanoelec Displed project is based on the Smart-Pixel concept, a patented key enabling technology that paves the way for the manufacture of new display concepts in Europe. The first goal of the project is to develop the Smart-Pixel concept through proof-of-concept demonstrations and the second is to develop new concepts for display features (light field multi-views, sensor display, flexible display...).

In 2023, we obtained the very first results from our pilot initiative on life cycle analysis as applied to the early R&D phase on Smart-Pixel. We achieved the very first full-integration 3D-LED Smart-Pixel technology, as well as the first RGB (Green-Red-Blue) pixel proof–of-concept in three colors.

A new-generation 2D-LED Smart-Pixel demonstrator has been delivered. It consists of a PCB with a matrix of 8x8 smart pixels, that is fully operational. EVGroup and SET provided new tools for advanced hybrid bonding. Aledia has completed the construction of its production site and the pilot line will be fully equipped in 2024.

FRÉDERIC BERGER (CEA-LETI) IS SETTING THE SET MACHINE FOR TESTING A NEW KIND OF TOOL FOR THE MASS TRANSFERT OF MICROLED FOR NANOELEC/DISPLED PROGRAM

DISPLED PROGRAM AT A GLANCE

→ VISION

A unique opportunity for a French & European ecosystem on large display technologies for immersive applications

→ AMBITION

To design and demonstrate key microLED technologies for high-end, immersive displays

→ MISSION

To develop process flows for microLED, Smart-Pixel fabrication and mass transfer onto the display

→ PARTNERS

Aledia
CEA
EVGroup
SET

SUSTAINABILITY

Smart-pixel life cycle analysis

LOOKING FOR THE KEY PARAMETERS TO OPTIMIZE THE ENVIRONMENTAL FOOTPRINT OF THE SMART-PIXEL PROCESS FLOW.

Environmental impacts must be taken into account when developing any new technology. This applies to the display industry design work carried out in the Nanoelec/Displed program.

In 2022 and 2023, a Life Cycle Assessment (LCA) of the Smart-Pixel was conducted on R&D work (for the very first time in the World), as well as the study of a tool dedicated to identifying the key parameters of the environmental footprint of the associated process flow. *"The overall objective of this study is to assess the environmental impacts of this kind of display manufacturing, considering not only climate change but also all the sixteen environmental impacts recommended by the Product Environmental Footprint method (PEF). Hence, the aim of this study is to propose a methodology based on LCA for the first time"*, explains Antonin Holo, LCA engineer at CEA-Leti, which carried out the study.

An initial set of results has been obtained, for all sixteen environmental impact categories of the PEF 3.0 method recommended by the European Commission.
"For example, the contribution of the epitaxy step could be seen with regard to every environmental impact. Etching, deposition and stripping process-family contributions were also underlined, given their large contribution to each of the selected environmental impacts", Antonin Holo reports[1]. He presented the study at the Display Week, in San Jose (US), on May 2023.

Since there are no databases for microelectronics at the component scale, or the literature is outdated and does not reflect current trends, this LCA will provide new and previously unseen results.

These new LCA results are used on an in-house eco-design tool, allowing comparison of new technologies with reference technology. It relies on a similar tool designed by CEA-Liten for photovoltaic R&D[2]. The fabrication flow parameters can be easily altered in order to obtain an overview of how this changes the sixteen environmental impacts addressed.

Among other results of interest is demonstration of the impact of the type of electricity (carbonated vs. nuclear) on CO_2 generation for Smart-Pixel fabrication. *"In fact, the biggest factor impacting our carbon footprint in this process is the contribution of CMOS. If we source it from Asia, the impact on the climate is high; if we buy it from a country with a low-carbon energy mix, the balance is more favorable"*, explains Sandrine Chabaud, Safety and Environment Manager at Aledia. ◊

1. Holo, Antonin, Dubarry, C., Lopes, J.-C., Dupont, M., Chabaud, S., & Templier, F. (12-17 may). MicroLED Display Life Cycle Assessment. Display Week, San Jose, USA.

2. Nouha Gazbourg "Systemic integration of Eco-design in photovoltaic technologies R&D", PhD Report UGA on a doctoral thesis prepared at CEA-Liten, Feb. 2019.

3. Templier, F. (2023, August 16). Integration technologies for hybridizing GaN microleds and CMOS circuits. K-Display 2023 Conference & Exhibition, Seoul, Korea

TECHNOLOGY STATE OF THE ART

Hybridizing GaN microleds and CMOS circuits

REVIEWING HYBRID BONDING POSSIBILITIES FOR HETEROGENEOUS INTEGRATION.

At the K-Display Conference in Seoul, Korea, François Templier reviewed the challenges for the factoring of MicroLED arrays driven by CMOS circuits[3] : *"Such devices are needed for GaN microdisplays and large area displays"*, he underlines. Several technologies may be used to hybridize the two parts, and Smart-Pixel should be the one to enhance throughput. *"It is promising for mass production for displays as demonstrated with recent results in hybrid bonding by the Nanoelec/Displed program"*, suggests François. ◊

A STEP AHEAD

The move to flexible displays

FIRST RESULTS FOR THE TRANSFER OF MULTIPLE DIES ON NON-RIGID SUBSTRATES.

As part of the Nanoelec/Displed program, CEA-Leti and Aledia teams are investigating how to open up the application of MicroLED Smart-Pixels to flexible displays, or to new functionality based on the addition of sensors, or to multiview displays.

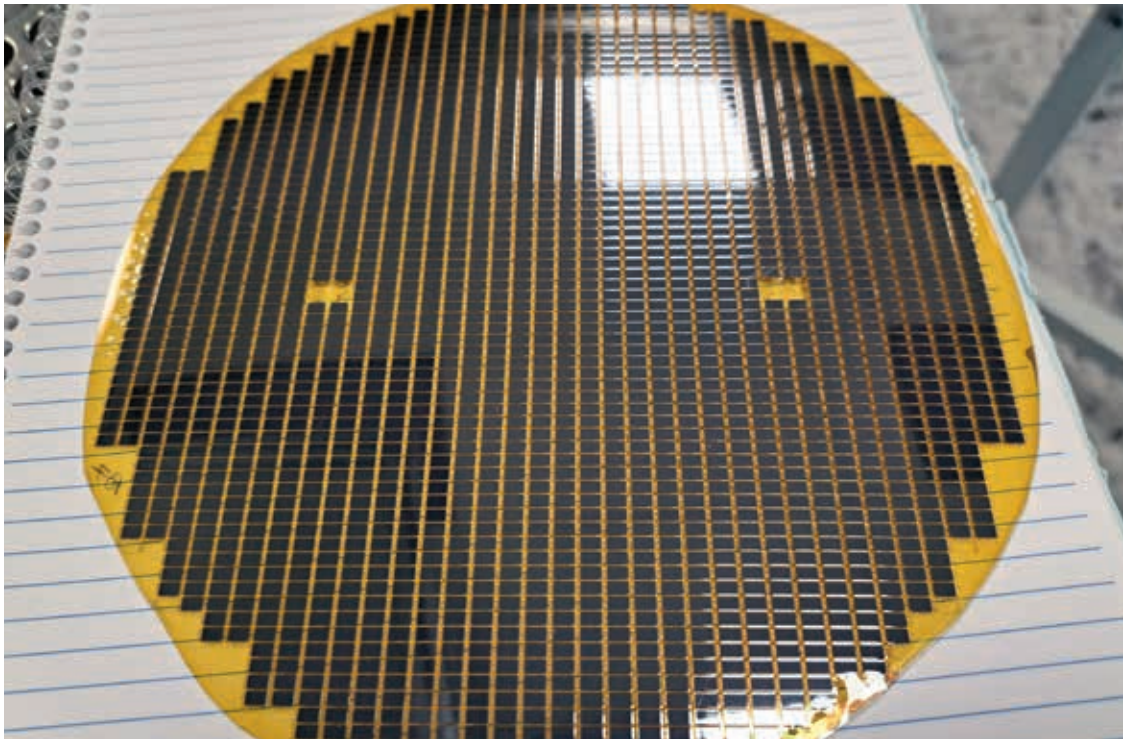
Thus in 2023, design and development of a Smart-Pixel flexible display started at Nanoelec.

"An important step towards the flexible demo is to evaluate how multiple, very small dies (<500µm) can be transferred with high accuracy onto foldable or rollable plastic substrates", explains Aurélie Beaumont, leading the study at CEA-Leti, together with Hugues Lebrun, Display Engineering at Aledia. *"Our test vehicle showed how flexible and conformable displays of various dimensions (from a few cm² to a full 200mm surface) can be fabricated and successfully populated with multiple Si bare dies – coarse pitch in this case"*.

15 flex wafers were produced and the fabrication of a fine-pitch test chip was run in parallel *"in order to define the best configurations regarding die assembly"*, Aurélie Beaumont adds. The next step is now to develop the assembly of the flexible substrates with the fine-pitch test chip, and then with the functional Smart-Pixel Chips.

Today's flexible or foldable displays use TFT (thin-film transistor) driving devices (active matrix backplanes) with thin-film OLED emitters, which are themselves flexible. Both TFTs and OLEDs are suffuring mechanical stress during folding. MicroLED Smart-Pixels make it possible to get around the difficulty of making the whole technology flexible. *"In our case, only the support circuit, which is totally passive (no transistors), is flexible due to the pixelation of the microLEDs"*, underlines Hugues Lebrun. *"The flexibility is then only limited by the surface occupied by the LED in the pixel area."* ◊

Below,
CHIP TEST ON FLEXIBLE SUBSTRATE (WITH TOP POLYMER)
© DR



Abdenacer Aitmani, engineer at CEA-Leti, receiving a firt set of tools for mass transfert of dies, for a new concept of displays including microleds on smart pixels.

© A.HAVRET/CEA

MANUFACTURING TOOLS FOR HETEROGENEOUS INTEGRATION

Picking and placing dies on a substrate

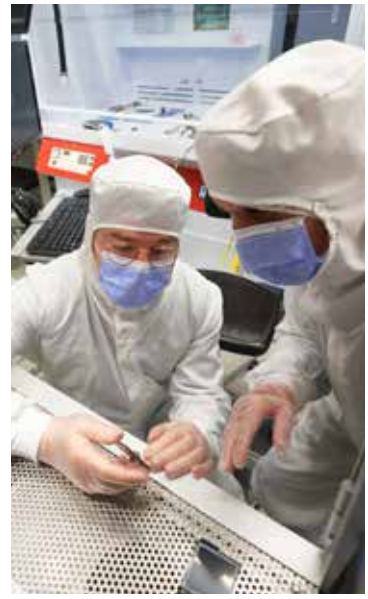
NEW MACHINES WILL ACCELERATE THE DEPLOYMENT OF A MASS PRODUCTION LINE OF DISPLAYS.

"In the previous phase of the Displed program, we already demonstrated the use of dedicated micro-tools mounted on our flip-chip bonder machine to pick up small dies individually and several of them collectively", says Pascal Metzger, CEO of SET. This year, SET and CEA teams did the same successfully but with much smaller dies, picking them up individually and placing them on a substrate.

SET is also investigating the possibility of flipping the dies. *"To meet the accurate placement requirement set in the Nanoelec/ Displed program, we have decided to completely redesign the motorization chain including motors, guidance systems and encoders to improve the precision of the movements of our robot"*, adds Pascal Metzger.

Below,
ASSEMBLY ROOM AT SET, A CORE PARTNER OF NANOELEC. SET IS A FRENCH TOOL SUPPLIER FOR ELECTRONICS VALUE CHAIN, SPECIALIZED IN FLIP-CHIP BONDING, A PROCESS TO ASSEMBLE TWO COMPONENTS TOGETHER, MECHANICALLY AND ELECTRICALLY.
© SET

With regard to the mass transfer of microLEDs, SET is working with the other Nanoelec/Displed partners on the feasibility of a concept, which is a prerequisite for an industrial machine that will be essential for the deployment of a screen production line in France and Europe. *"With the Nanoelec ecosystem, we feel we have a good lead in the field of direct bonding, particularly in terms of assembly precision and yield"*, Pascal Metzger adds. ◊



Above,
SET FACTORY IN HAUTE-SAVOIE, FRANCE
© SET

Side right,
SET EQUIPMENTS UNDER TESTING IN CEA-LETI CLEANROOM
© A.HAVRET/CEA

Beyond the Nanoelec/Displed program, SET teams are also taking part in transverse actions set by Nanoelec to boost the attractiveness of the electronics business. *"As a supplier for the development of the microelectronics and digital industry, we have to find ways to attract, hire and keep top-skilled collaborators, even if we are a small company based in the heart of the Alps"*, Pascal Metzger says. He is in the center of the above picture, as one of the guest speakers at the Territorial forum on the attractiveness of the electronics industry, May 11, 2023 in Grenoble, with Stéphane Berthier, Head of HR Dev at ST Microelectronics – Business Coach (left) and Jean-Philippe Gene, Director for Business & Equity at Linksium (right).

INDUSTRIAL RAMP-UP

New tool for advanced hybrid bonding

WITHIN THE FRAMEWORK OF IRT NANOELEC, EV GROUP DELIVERED A DIE DIE-TO-WAFER SELF-ASSEMBLY EQUIPMENT TO CEA-LETI'S CLEAN ROOM.

This innovative technique enables high throughput collective die-to-wafer bonding with high accuracy alignment.

Access to state-of-the-art samples through a program like Nanoelec/Displed is crucial for developing and advancing this technology. EVG bridges the gap between CEA-Leti's cutting-edge process development and the industry. Initial results pave the way for high-volume manufacturing, and the ability to reach new markets is growing as die-to-wafer bonding gains traction in heterogeneous and hybrid integration. *"In addition, we completed a new manufacturing building in 2023. This facility is the latest in a series of expansion phases and investments driven by continued strong demand for EVG's hybrid bonding and other process solutions and process development services to support the rapidly growing advanced packaging and 3D/heterogeneous integration market"* emphasizes Markus Wimplinger, Corporate Technology Development & IP Director of EV Group. ◊

Photo,
PIERRE MONTMEAT AND MÉLANIE VACON, CEA-LETI ENGINEERS, PREPARING A 3D CHIP BONDING FOR NANOELEC ON EVG 810A LOW TEMPERATURE PLASMA ACTIVATION SYSTEM

SMART-PIXEL DEMONSTRATORS

RGB pixels work

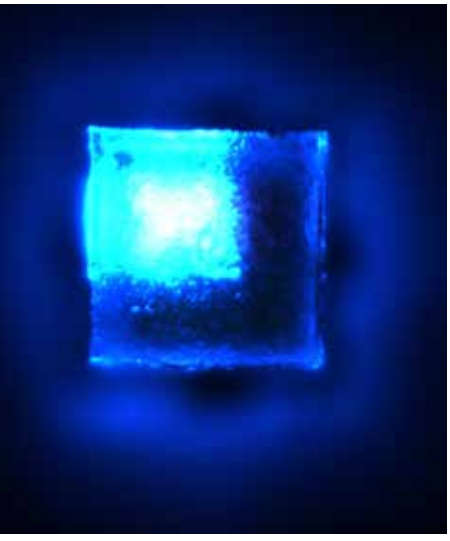
WHILE ALEDIA COMPLETES THE CONSTRUCTION OF ITS FUTURE FACILITY, TECHNICAL RESULTS ENABLE THE DESIGN OF THE PRODUCTION FLOW TO CONTINUE FOR THE DISPLED PROGRAM.

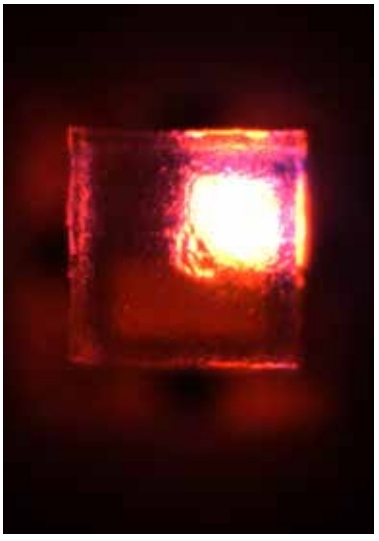
"3D-LED Smart-Pixel development[4] *has reached an important step this year with successful Smart-Pixel process integration, involving two metal levels, hybrid bonding and backside grinding"*, says Muriel Dupont, R&D partnership manager at Aledia.

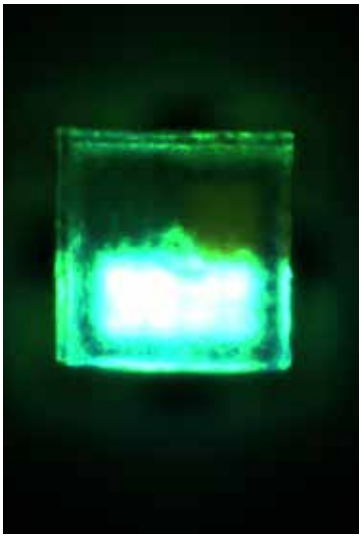
For the demonstration of full-color units, the test vehicle implemented by Aledia teams showed blue emission coming from the nanowires and green and red emission based on QD conversion. *"This is the first proof-of-concept of RGB Smart-Pixel in three colors"*, highlighted Muriel.

At the same time, a demonstrator including a matrix of a new generation of 2D-LED Smart-Pixels on a PCB has been fully operational and major improvements have been obtained on the roadmap towards 300mm microLED production. LED growth on the 300mm MOCVD system installed at Aledia/Echirolles showed an emission wavelength centered on 446.4nm with very low standard deviation among the LEDs. *"We are achieving very good uniformity and this is promising for further developments of 300mm Smart-Pixel integration"*, reports Jérome Napierala, epitaxy expert at Aledia. ◊

Below,
DEMONSTRATION OF A FULL-COLOR UNIT BY ALEDIA: BLUE EMISSION COMES FROM THE NANOWIRES AND GREEN AND RED EMISSION BASED ON QD CONVERSION
© ALEDIA







4. For high resolution displays with small pixel pitch

ONE OF THE EIGHT POSTERS CREATED BY THE STUDENTS OF THE BRASSART-GRENOBLE SCHOOL ON THE TOPIC **"LA MICROÉLECTRONIQUE POUR VIVRE DANS UN MONDE MEILLEUR"** (MICROELECTRONICS FOR LIVING IN A BETTER WORLD) FOR THE TECH&FEST 2024 FESTIVAL.

POSTER BY ERIC DECOUD, "GRAPHIC DESIGN" STUDENT

Photonic sensors

Innovation in silicon photonics: from design tools to mass production processes

STÉPHANIE GAUGIRAN
HEAD OF THE NEW PHOTONIC APPLICATIONS SECTION AT CEA-LETI & DIRECTOR OF THE NANOELEC/PHOTONIC SENSORS PROGRAM

The partners in the Nanoelec/Photonic Sensors program are preparing to be competitive on the emerging photonics on silicon chips market. This market should enjoy an annual growth rate of 44%, reaching more than 600 millions US dollars in 2027[1].

Our aim is to provide the Nanoelec partners with a complete chain of solutions – from EDA to mass production – designed to facilitate the adoption of photonics on silicon by new applications requiring complex detection functions such as 3D detection in mobile phones, autonomous vehicles, or biochemical detection for health care and environmental surveillance.

In 2023, we studied new waveguide antenna array architectures with very low divergence at a wavelength of 1550nm. With regard to simulation and design tools, we worked on Process Design Kits tailored to the design of III-V components such as lasers and modulators and compatible with industrial standards, along with a numerical model of the gain function in a III-V materials laser. Work on hybrid lasers is continuing with two new designs and initial study on producing tunable lasers. Finally, we are beginning development of a photonic sensor for titrating ethanol, liable to be of interest to a number of large industrial sectors.

1. According to the Yole "Silicon Photonics" report in 2023. The growing number of products under development for various applications sectors, including the flourishing AI sector, is driving the largest industrial foundries to invest in the development or even the creation of photonics platforms on their sites. Most of them around the world are already including co-packaged optics solutions in their ranges.

HYBRIDATION OF III-V MATERIALS ON A 300-MM INDUSTRIAL STANDARD WAFER
© A.HAVRET/CEA

PHOTONICS SENSORS AT A GLANCE

→ VISION

New sensor opportunities based on large-scale 300mm silicon photonic industrial technologies

→ AMBITION

Provide the Nanoelec partners with a complete chain of solutions – from EDA to mass production – designed to facilitate the adoption of photonics on silicon by new applications requiring complex detection functions such as 3D detection in mobile phones, autonomous vehicles, or biochemical detection for health care and environmental surveillance

→ MISSION

Our main technological challenges for such sensors are measurement precision, miniaturization, data processing and transfer, and also compatibility with mass production. The unique properties and performance of integrated photonics are essential in being able to meet these demands and these challenges

→ PARTNERS

Almae
CEA
CNRS
Siemens EDA
STMicroelectronics

EMERGING APPLICATION

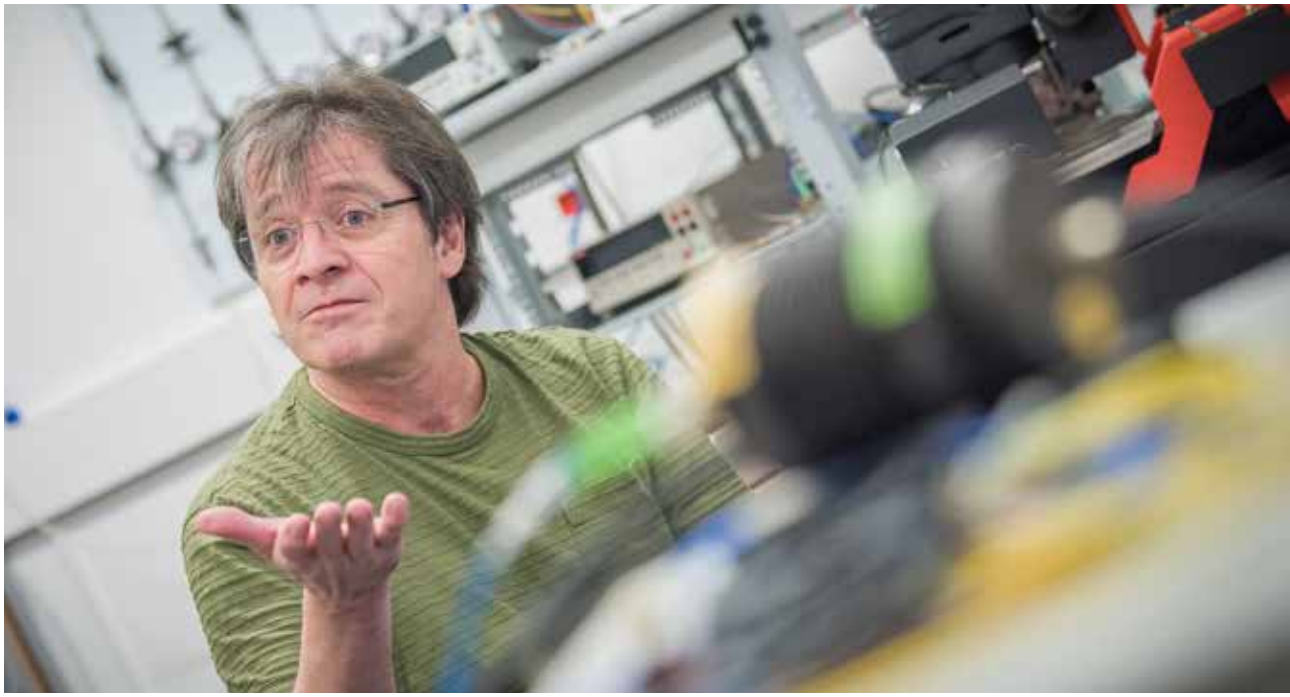
A photonic sensor to titrate ethanol

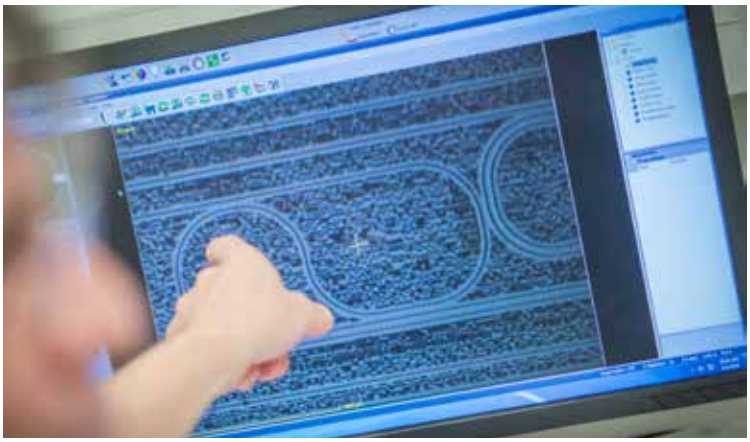
CEA-LETI IS DEVELOPING AN INTERFEROMETER TO DIRECTLY MEASURE THE CONCENTRATION OF ETHANOL IN VERY SMALL QUANTITIES OF LIQUIDS. THE APPLICATION COULD BE OF INTEREST FOR THE AGRI-FOOD INDUSTRY AND THE HEALTH SECTOR.

Titration of ethanol is of interest to numerous industrial players, for example in the field of paints, solvents and petrochemistry, as well as in the agri-food industry and the health sector. CEA-Leti's photonic platform, developed by the industrial and academic partners within Nanoelec, will act as the basis for development of a very low-cost sensor which can titrate ethanol in a volume of a few microliters of liquid. *"We have chosen a photonics approach based on Mach-Zehnder interferometers (MZI) in the near-infrared band: a laser beam illuminates two channels, one of which contains a micro-cavity for the liquid. The two beams are recombined and their phase shift depends directly on the quantity of alcohol in the liquid"*, explains Pierre Labeye, engineer at CEA-Leti.

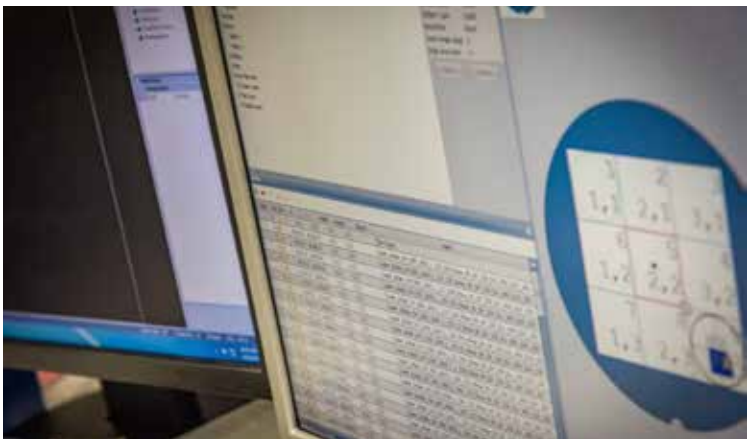
Proof of concept was carried out in 2022 on the existing MZIs used to measure the absorption of colored inks in different concentrations. The etching process used to obtain a specific cavity for the liquid sample above the waveguides was developed in 2023. *"The first operating tests performed with alcohol in early 2024 are promising"*, says Pierre Labeyre. ◊

Above,
PIERRE LABEYE (CEA-LETI) IS DEVELOPPING A SENSOR FOR ALCOHOL DOSE TITRATION
© O.DEVISE/CEA 2024



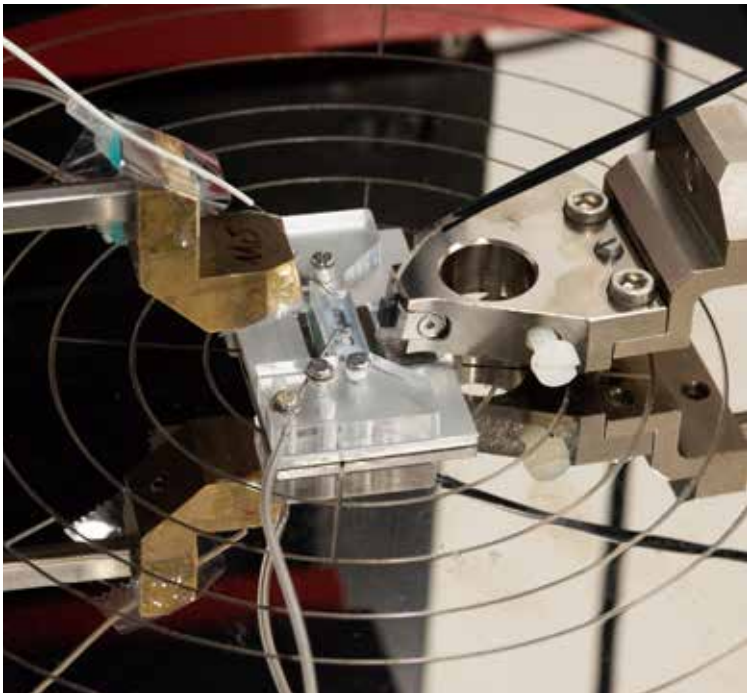


Top,
MICROSCOPE VIEW OF THE PHOTONIC MZI CIRCUIT DESIGNED AND PRODUCED AT CEA-LETI FOR ALCOHOL DOSE TITRATION
© O.DEVISE/CEA 2024



On the right,
DATA SCREEN FOR THE CIRCUIT DEDICATED TO ALCOHOL DOSE TITRATION
© O.DEVISE/CEA 2024

Above right,
TESTING THE VERY FIRST PROTOTYPE OF A PHOTONIC SENSOR FOR ALCOHOL DOSE TITRATION
© O.DEVISE/CEA



CIRCUIT DESIGN

Design kits and model libraries for photonics process

THE CIRCUITS DESIGN AND MODELING SOFTWARE RESOURCES USED WITHIN NANOELEC NOW INCLUDE III-V COMPONENTS AND MODELLING OF A MACH-ZENDER INTERFEROMETER (MZI).

Within the Nanoelec consortium, Siemens EDA[4] and CEA are establishing reference flows for the design and verification of integrated circuits, and are developing process design kits (PDK) and verification software tools, as well as component model libraries (PMS).

"A PDK[5] provides a standardized methodology for the design and manufacture of integrated circuits, which is essential to guarantee their correct operation", says Jean-Marc Talbot, Head of Solutions & Strategic Partnerships at Siemens EDA.

The PDK generally comprises information about the manufacturing process for integrated circuits, such as stacking, the steps in the process and the materials used. It also includes design rules which specify the constraints regarding the layout of the integrated circuit.

LASERS AND MODULATORS

In 2023, an extension module for the Siemens software suite was specifically developed to validate architectures of III-V components such as lasers and modulators. *"This new module can be superposed on various 300 or 200mm Photonic Core PDKs and on Si310 or SOI220 photonic technologies"*, explains Fabien Gays, in charge of the project at CEA-Leti. *"It contains all the necessary levels for backside or frontside III-V integration and rule set for Siemens verification tool."*

VALUE PROPOSAL FOR INDUSTRY

"On Spice[6] simulators, we are working with the other Nanoelec partners to determine the use cases and methodology associated with the use of PMS (Photonic Model Suite) libraries for actual industrial applications and the related circuits, in order to rapidly identify the value proposal", adds Jean-Marc Talbot. ◊

4. Siemens Electronic Design Automation SARL – Siemens EDA, world leader in design, verification and manufacturing assistance tools for integrated circuits, packages and PCBs, is one of the founding members of IRT Nanoelec. It is the only IRT Nanoelec partner in electronics and microelectronics CAD

5. Set of tools, data files and documentation supporting the design tools used to develop integrated circuits (IC)

6. SPICE (Simulation Program with Integrated Circuit Emphasis) is a free general-purpose simulation software for analog PCBs. It can be used to simulate the individual components (resistors, capacitors, transistors)

7. De Foucauld, E., Rozeau, O., Myko, A., Fowler, D., Virot, L., & Gays, F. (2023). Compact modeling of photonic devices in Verilog-A for integrated circuit design. Solid-State Electronics, 200

A FULL SILICON PHOTONICS PROCESS FLOW

Verilog-A language to simulate photonic integrated circuits

SIMULATION OF A MACH-ZENDER INTERFEROMETER (MZI).

In a paper published in Solid-State Electronics Review[7], scientists from CEA-Leti, working within Nanoelec, put forward a methodology to simulate photonic integrated circuits (PIC) using commercial IC simulators. *"For this, all photonic devices are modelled using Verilog-A language including transmission and reflection of light"*, states Emeric De Foucauld, as first author of the study. *"For each model, both polarizations, transverse electric (TE) and transverse magnetic (TM) polarized waves, are considered. The methodology is able to simulate resonant and interference effects and we demonstrated waveguide and ring resonator simulations."* The extraction of a Mach-Zender Interferometer (MZI) illustrates the modeling based on measurements with Nanoelec silicon technology developed by CEA-Leti: despite only being passive structures, these MZI were fabricated using a full silicon photonics process flow including active devices with ion implantation steps and two levels of Back-End-Of-Line (BEOL). *"Simulations of attenuation and reflection demonstrate the advantages of this Verilog modeling"*, concludes Emeric De Foucauld. ◊

APPLICATIONS

Large-scale lidar

AN OPA INTEGRATION SCHEME HAS BEEN DRAWN UP WITH A VIEW TO INTEGRATION ON AN INDUSTRIAL PRODUCTION PLATFORM.

With a view to developing large-scale production of Lidars at low unit cost, Nanoelec supported Cyrille Barrera's thesis, prepared at STMicroelectronics[8].

This work led to the definition of an integration scheme for an Optical Phased Array[9] on STMicroelectronics' PIC50G photonic platform. The scheme includes 256 photonic antennas, each being phase-modulated by an individual phase-modulator, and separated by 2 microns to generate a laser beam with 0.18° angular divergence, which can be repositioned in less than a microsecond for an average power consumption of less than 1mW.

Eleven scientists from CNRS, STMicroelectronics and CEA (including M. Barrera) working together in the Nanoelec/ Photonic Sensor Program reported[10] the demonstration of a 256-channel 1D optical phased-array (OPA) based on plasma-dispersion effect. *"Our system exhibits ultra-low power consumption (~1mW) revealing the potential of a carrier depletion scheme at low doping dose for solid-state Lidar applications"*, comments Louise-Eugénie Bataille, as first author of the study. *"All in all, our work indicates that the low-doped carrier-depletion-based OPAs have great prospects as ultra-low power solid-state Lidar"*, she said. ◊

8. Design, characterization and integration of a laser scanning system in silicon photonics for Lidar detection applications at 1.55 µm, PhD thesis defended on March 24, 2024 at Université Paris-Saclay

9. An Optical Phased Array (OPA) allows an optical beam to be directed at very high speed, without any mechanical movement, to scan a scene over ranges of several tens of meters

10. Bataille, L.-E., Barrera, C., Guerber, S., Monfray, S., Grosse, P., Fowler, D., Brision, S., Charlet, I., Vivien, L., Dagens, B., & Boeuf, F. (2023). Ultra-low power 256 channels optical phased-array based on low-doped carrier-depletion modulators. 2023 CLEO (2023, San Jose, CA, United States)

OPTICAL PHASED ARRAY

Operating at 1550nm wavelenght

STMICROELECTRONICS AND CEA ARE DEVELOPING NEW SLOTTED WAVEGUIDE ANTENNA ARRAYS.

Low-doped carrier-depletion-based OPAs have great prospects as ultralow power solid-state Lidar.

Obstacle detection with a Lidar requires a focused beam to ensure precise sweep, with the preference thus being for arrays with long diffraction and low diffraction force based on a low index contrast. *"In this context, within Nanoelec, we were this year able to demonstrate a BIC (Bound state In the Continuum) effect slotted waveguide antenna (SWGA) array one millimeter long, so as dual layers Si-SiN antennas, both designed to achieve divergence of less than 0.08° operating at 1550nm wavelenght"*, says Stéphane Monfray, Engineer, manager of the action at STMicrolectronics. ◊

EMERGING CONCEPTS

Low-power low-loss phase modulators for Lidars

HYBRID InGaAsP/Si CAPACITIVE MODULATORS WERE DEMONSTRATED BY CEA FROM 300MM STMICROELECTRONICS PHOTONIC WAFERS.

To control the beam scan in a Lidar based on optical phased array (OPA) circuits, a phase modulator in each arm of the OPA is needed. Since 2021, scientists working within the Nanoelec/Photonic program, from STMicroelectronics, CEA and Almae, have been developping a low-loss low-power phase shifter based on a III-V/Si hybrid capacitor integrated on standard silicon photonic circuits from STMicroelectronics. *"In 2023, we have realized and measured our first prototypes of hybrid modulators, based on the transfer of an InGaAsP layer onto a gate oxide of the order of 10nm. Dephasing up to 250°/mm have been measured on our first prototypes"*, explains Yohan Désières, in charge of the project at CEA-Leti. The following picture gallery shows the different steps in the fabrication and test of the demonstrator at CEA-Leti from photonics wafers made at STMicroelectronics and III-V epiwafer from Almae. ◊

Below,
DEMONSTRATOR OF THE CAPACITIVE MODULATOR FOR LIDAR UNDER DEVELOPMENT AT CEA-LETI, WITH STMICROELECTRONICS AND ALMAE, IN THE FRAME OF THE NANOELEC/PHOTONIC SENSORS PROGRAM
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To the right,
TRISTAN FAURE, TECHNICIAN AT CEA-LETI, SUPERVISES THE III-V MATERIALS LITHOGRAPHY STEP FOR THE CAPACITIVE MODULATOR DEMONSTRATOR
© A.HAVRET/CEA 2024

To the right,
LOIC SANCHEZ, ENGINEER AT CEA-LETI, PERFORMING MOLECULAR BONDING OF WAFERS OF III-V MATERIALS SUPPLIED BY ALMAE ON 300MM PHOTONICS WAFERS SUPPLIED BY STMICROELECTRONICS
© A.HAVRET/CEA 2024

Below,
ELECTRO-OPTICAL MEASUREMENTS ON InGaAsP/Si MODULATORS BY YOHAN DÉSIÈRES, PHOTONICS ENGINEER IN CHARGE OF THE CAPACITIVE MODULATOR PROJECT AT CEA-LETI
© O.DEVISE/CEA 2024

Clément Castan, CMP (chemical & mechanical polishing) engineer at CEA-Leti, loads 300mm silicon wafers into the machine which is used for planarizing before molecular bonding of the III-V materials.

UPCOMING TECHNOLOGIES

Taking photonic integration technologies further

NANOELEC PRESENT AT THE IEEE SILICON PHOTONICS CONFERENCE AND AT PHOTONIC WEST.

Very promising devices for quantum photonics.

Frederic Bœuf, Photonics Innovation Technology Director at STMicroelectronics, and Bertrand Szelag, a scientist at CEA were guest speakers at the IEEE Silicon Photonics Conference[11]. Noting that *"III-V materials have optical properties complementary to Si"*, Frédéric Bœuf pointed out that hybrid III-V/Si device applications should not be restricted to laser sources. *"Backside integration is simplifying integration of III-V in CMOS fabs, even if several challenges still remain, such as multi-III-V/Si device integration"*, he added.

For Bertrand Szelag, *"there is no standardization of Si photonics platforms & no performance roadmap (Moore law like) leading to technological nodes but available foundry process capabilities are definitely leading to different levels of performance and yield."* He referred to several examples, including *"SOI Substrates optimized for Si Photonics leading to better stability & higher product yield."*

At Photonic West 2023[12], a team from CEA involved in the Nanoelec/Photonic Sensors program, together with their colleagues from Università di Pavia (Italy), unveiled very promising results on high rejection filters based on cascaded ring resonators in a 300mm Silicon photonics platform.

"Silicon photonics is a platform of choice for integrated quantum photonics. The advent of 300mm fabrication tools and immersion lithography for photonics may be a game changer and lead to the practical use of ring resonator based devices", states Leopold Virot (CEA-Leti) as first author of the publication. They implemented this type of ring resonators on their 300mm SOI platform for Silicon photonics using immersion lithography. *"This type of technology offers unprecedented levels of uniformity and reproducibility within a die but also from die to die"*, adds Leopold. *"Thus, we combined and cascaded ring resonators to fabricate high rejection filters in Coupled Resonator Optical Waveguide (CROW) configurations."* Such high rejection filters are very promising candidates for quantum photonics, and more particularly in circuits based on photon pair generation, where pump rejection filters with over 100dB of rejection are needed. ◊

11. April 2023, Arlington, VA/USA

12. Virot, L., Ferrara, A., Wilmart, Q., Galli, M., Bajoni, D., & Olivier, S. (2023). High rejection filters based on cascaded ring resonators in a 300mm silicon photonics platform. Silicon Photonics XVIII, PC12426, PC124260C. https://doi.org/10.1117/12.2646814

SiN WG patterning (combining hard mask strategy patterning and the plasma etching steps involved in WG fabrication) is one of the solutions for accurately controlling the roughness of the SiN waveguide sidewalls and thus controlling SiN-based photonic platform performance (in terms of optical losses).
The Microelectronic Technologies Laboratory (CNRS-UGA) has the know-how, not only to pattern SiN WG with low roughness, but also to quantify the sidewalls roughness present after patterning thanks to its powerful 300mm etching platform and its expertise in sidewalls roughness metrology.

TOWARDS 300MM STANDARD PROCESS

Microleds based on III-V materials

EXTREMELY BRIGHT RED DIODES SHOULD ALLOW THE INDUSTRIAL PRODUCTION OF NEW LIGHT SOURCES.

The arrival of new applications using micro-displays for virtual and augmented reality is arousing growing interest in the development of light emitting diodes (LEDs).

In her thesis work at CNRS and CEA[2], Pauline Gaillard focused on studying a process for obtaining red diodes based on III-V materials (gallium arsenides and phosphides) with direct epitaxial growth on 300mm silicon wafers. *"But this is not the only challenge facing us in this work!"*, she states.

The components must be extremely bright so that they remain visible in highly luminous environments; in addition, the high image definition requires increasingly small pixels. *"Only micro-LEDs can meet these criteria"*, says Pauline, who focused on manufacturing inorganic LEDs, red emitters in particular *"as of the three colors, they are the most complex to develop."* These red LEDs can be produced from color conversion layers on GaN, InGaN on GaN or arsenides and phosphides on GaAs. This latter is the most efficient and mature system for producing the color red.

In the article in the IEEE Photonics Technology Letters review associated with the thesis[3], a team of scientists from CEA and CNRS supported by Nanoelec considers that *"these results could pave the way for large-scale, low-cost monolithic integration of red µ-LEDs on 300mm Si-CMOS control circuits and the production of high-resolution RGB micro-displays, which are usable in various optoelectronic applications."*

After obtaining her PhD, Pauline Gaillard was hired by STMicroelectronics. ◊

2. *"Développement de LEDs rouges en matériaux III-V (type GaAs) directement épitaxié sur silicium 300mm"* (development of red LEDs in III-V materials (GaAs type) with direct epitaxial growth on 300mm silicon), PhD thesis defended by Pauline Gaillard (CNRS/LTM) on 21 February 2023 at Grenoble-Alpes University

3. Gaillard, P., Ndiaye, A., Ben Bakir, B., Le Maitre, P., Da Fonseca, J., Hartmann, J. M., Martin, M., Moeyaert, J., Mehdi, H., Baron, T., & Jany, C. (2023). III-V Heterostructure Grown on 300mm (Ga/Si) Wafer for Large-Scale Fabrication of Red µ-LEDs. IEEE Photonics Technology Letters, 35(2), 101-104. https://doi.org/10.1109/LPT.2022.3225219

Photos,
MICKAEL MARTIN, MICROELECTRONICS ENGINEER AT THE CNRS. MOCVD III-V (METAL-ORGANIC CHEMICAL VAPOR DEPOSITION) EPITAXY DEPOSITION PLATFORM CONTROL CONSOLE – OPERATED BY THE MICROELECTRONIC TECHNOLOGIES LABORATORY (CNRS-UGA) AND CEA-LETI, THIS MACHINE WAS USED TO DEVELOP INDUSTRIAL STANDARD RED LEDS

BOOK CHAPTER

Packaging and testing of photonic integrated circuits (PICs)

REVIEW OF DIFFERENT OPTICAL PACKAGING TECHNIQUES AND THEIR UNDERLYING THEORY.

A report on the developments in assembly and test equipment and the PIC design environment.

Packaging and testing of Photonic Integrated Circuits (PICs) have changed dramatically in recent years, as the applications addressed by PIC-based modules shift to mass production. This entails new and more challenging requirements for the packaging and testing of PICs, which are expected to converge towards approaches similar to CMOS microelectronics, with high throughput and yield. However, packaging and testing of PICs still need to address several well-known critical requirements such as accurate alignment (laser/PIC and PIC/fiber coupling) or thermal management due to the thermal sensitivity of the alignment and photonic devices, and efficient co-packaging of the photonic circuits together with electronic drivers and host chips.

Three CEA-Leti scientists, working within Nanoelec, together with their German colleagues from Fraunhofer IZM and Ficontec Service, cosigned a contribution to the Integrated Nanophotonics book[13]. *"In our chapter, we are considering different optical packaging techniques as well as the underlying theory, examining current trends and requirements from emerging applications and architectures of PIC-based modules: co-packaged modules or photonic interposers among others. It also examines the evolution of the ecosystem, especially developments in assembly and test equipment and the PIC design environment"*, comments Stéphane Bernabé, as first author. ◊

13. Bernabé, S., Tekin, T., Sirbu, B., Charbonnier, J., Grosse, P., & Seyfried, M. (2023). Packaging and Test of Photonic Integrated Circuits (PICs). In Integrated Nanophotonics (p. 1-52). John Wiley & Sons, Ltd.

ONE OF THE EIGHT POSTERS ON THE THEME **"MICROELECTRONICS FOR LIVING IN A BETTER WORLD"** CREATED BY THE STUDENTS FROM THE BRASSART-GRENOBLE SCHOOL FOR TECH&FEST 2024.
POSTER BY LUCIE LAINÉ, "GRAPHIC DESIGN" STUDENT

Solutions for more secure digital components

VINCENT CACHARD

HARDWARE SECURITY GROUP MANAGER AT CEA-LETI AND DIRECTOR OF THE NANOELEC/PULSE PROGRAM

The emergence of the Internet of Things (IoT) has led to a proliferation of new services leveraging heterogeneous connected devices and data management. However, this growth is paralleled by a significant increase in cyberattacks, which has raised public and institutional awareness regarding the risks associated with rapid and inadequately controlled digital transitions.

As medical devices, automobiles, industrial equipment and urban infrastructure become increasingly connected and autonomous, new vulnerabilities are being identified in both hardware and software. These vulnerabilities are exposed to the public domain, eroding trust in connected products and services. Consequently, they not only impact the reputation of companies but also have wider implications for the economy and citizen privacy, potentially compromising the legal and social liability of public or private entities that have failed to adequately protect their products.

In addition, cybersecurity is often seen as a constraint in the design of digital products, with stakeholders reluctant to allocate significant resources in terms of cost, performance or ergonomics, fearing it may impede primary functions such as healthcare, mobility, or manufacturing.

The challenge of the Nanoelec/Pulse program is therefore to determine how electronic technologies can provide an adequate response to this new paradigm. The aim is to develop new technologies that will enable the emergence of connected products and services capable of increasing security, protecting the confidentiality, authenticity and integrity of digital data, ensuring protection of privacy, and simplifying the deployment of cybersecurity strategies. Our work focuses on three application areas: cybersecurity of industrial systems, cybersecurity of healthcare products, and security of autonomous systems and self-driving cars.

In 2023, we continued to enhance our solutions for more secure digital components, in particular in post-quantum cryptography and the security of embedded AI. We are also moving forwards on highly operational applications offering a very direct response to the needs of industry, such as to improve performance in terms of range, travel speed and safety to an overhead crane autonomous, to secure a microprocessor against malicious attacks, to detect them and provide restoration solutions in the event of incidents, or to validate multimodal perception solutions for autonomous vehicles. Finally, to address the needs of our industrial partners as well as those from society, we are redirecting our program towards the concepts of frugal electronics and digital systems.

PROTOCOL SECURITY TESTS FOR CONSUMERS WIRELESS DEVICES
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PULSE AT A GLANCE

→ VISION

Due to the rise in cybercrime, Internet of Things (IoT) cybersecurity is a major challenge for digital trust. Strengthening and hardening critical embedded, increasingly interconnected and smarter systems is now vital

→ AMBITION

New smart and intrinsically secure nanocomponents to reinforce the resistance of systems to future cyberattacks
+ improved security of smart embedded systems throughout their lifecycle (including AI algorithms)
+ safer deployment environments through digital ID, data sovereignty and secure interactions between smart systems

→ MISSION

To develop and test new security features for components and systems in three fields of application: Industry 4.0, healthcare and robotics

→ PARTNERS

CEA
Diabeloop
Grenoble INP-UGA
Inria
Schneider Electric
STMicroelectronics
UGA

CONNECTED HEALTH CYBERSECURITY

Secure implementation of AI in embedded systems

THE MASSIVE DEPLOYMENT OF MACHINE LEARNING (ML) MODELS ACROSS A BROAD SPECTRUM OF FIELDS RAISES A NUMBER OF SECURITY CONCERNS RELATED TO THEIR INTEGRITY, CONFIDENTIALITY AND AVAILABILITY.

Until recently, most research work focused on API (Application Processing Interface)-based attacks that consider an ML model as a pure algorithmic abstraction. However, new implementation-based threats have been revealed, emphasizing the urgent need to propose both practical and simulation-based methods to properly evaluate the robustness of models.

"To carry out security testing, we are the first to achieve a successful variant of the bit-flip attack (BFA) on a 32-bit Cortex-M microcontroller using laser fault injection", explains Pierre-Alain Moëllic (CEA), co-author of the study reported at SAFECOMP 2023[1]. *"This is a standard mean of fault injection for security evaluation that enables spatially and temporally accurate faults to be injected."*

Indeed, the challenge is to target precisely the bits of the parameters of a model that are stored in a Flash memory with a potentially complex organization. *"Parameter-based attack still lacks maturity and recent work highlights the limitations of the BFA and proposes improvements or alternatives. Thus, considering or combining more attack methods would improve the evaluation by simulating a more powerful adversary"*, says Mathieu Dumont to highlight an important perspective of this work.

The same team also assessed several attacks on the control flow of a neural network inference[2]. *"We reveal integrity threats by targeting several steps in the inference program of typical convolutional neural network models, which may be exploited by an attacker to alter the predictions of the target models with different adversarial goals"*, summarizes Clément Gaine (Mine Saint Etienne).

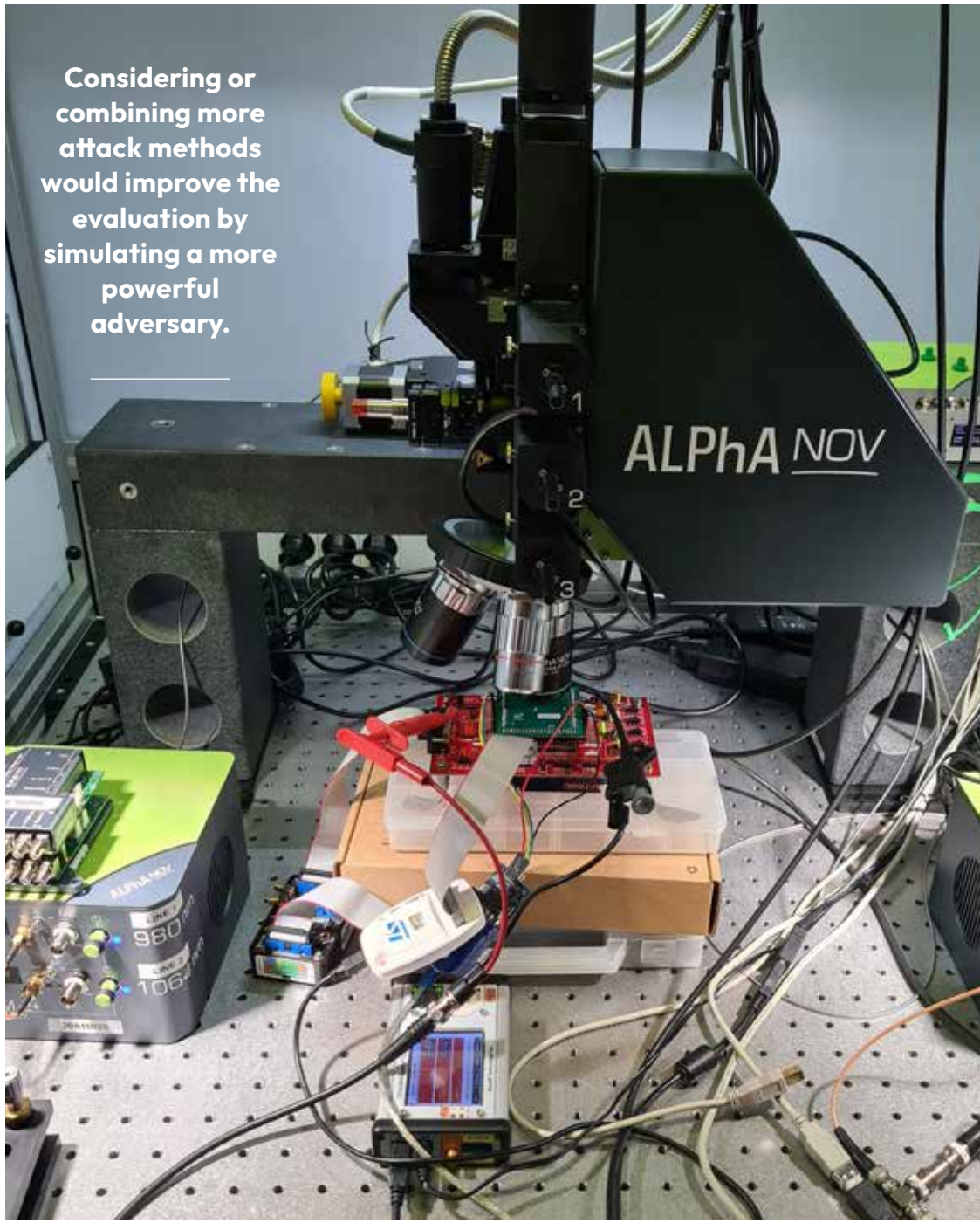
Last, they focused on embedded deep neural network models on 32-bit microcontrollers, a widespread family of hardware platforms in IoT, and the use of a standard fault injection strategy – Safe Error Attack (SEA) – to perform a model extraction attack with an adversary having limited access to training data. *"Since the attack depends to a large extent on the input queries, we propose a black-box approach to craft a successful attack set"*, explains Kevin Hector in a paper which received an award in the workshop SECAI, collocated with the European Symposium on Research in Computer Security[3]. *"Our model extraction attack is specifically tailored to models deployed in constrained platforms that are vulnerable to memory alterations. We extract information from a victim model by using a safe-error attack principle with custom inputs that optimize the leakage of parameters with bit-set fault injections."* ◊

1. Dumont, M., Hector, K., Moellic, P.-A., Dutertre, J.-M., & Pontié, S. (2023, September 19). Evaluation of Parameter-based Attacks against Embedded Neural Networks with Laser Injection. SAFECOMP 2023. 42nd International Conference on Computer Safety, Reliability and Security, Toulouse, France.

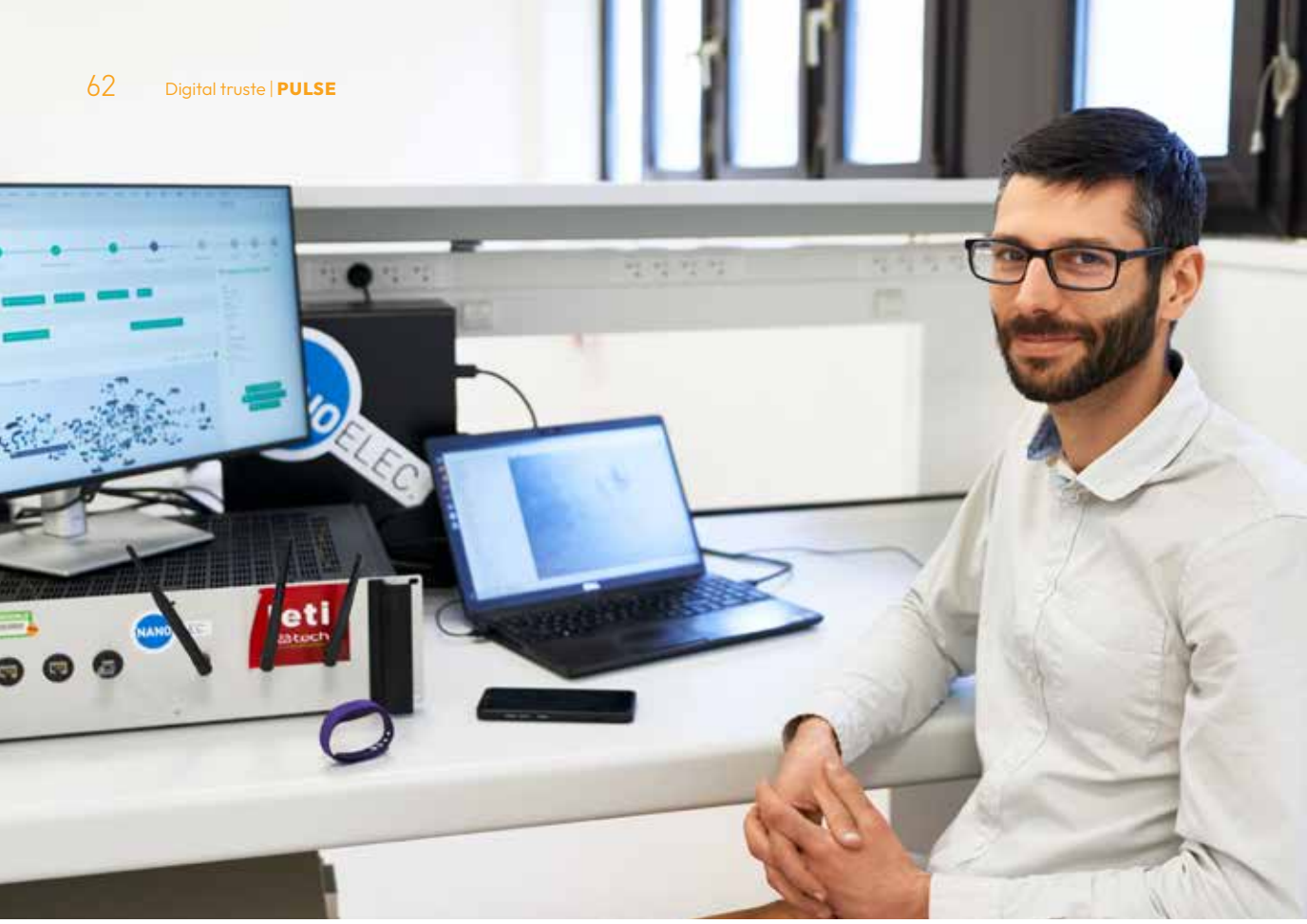
2. -Gaine, C., Moellic, P.-A., Potin, O., & Dutertre, J.-M. (2023, September 6). Fault Injection on Embedded Neural Networks : Impact of a Single Instruction Skip. DSD 2023. Architectures and Hardware for Security Applications, Durres, Albania.

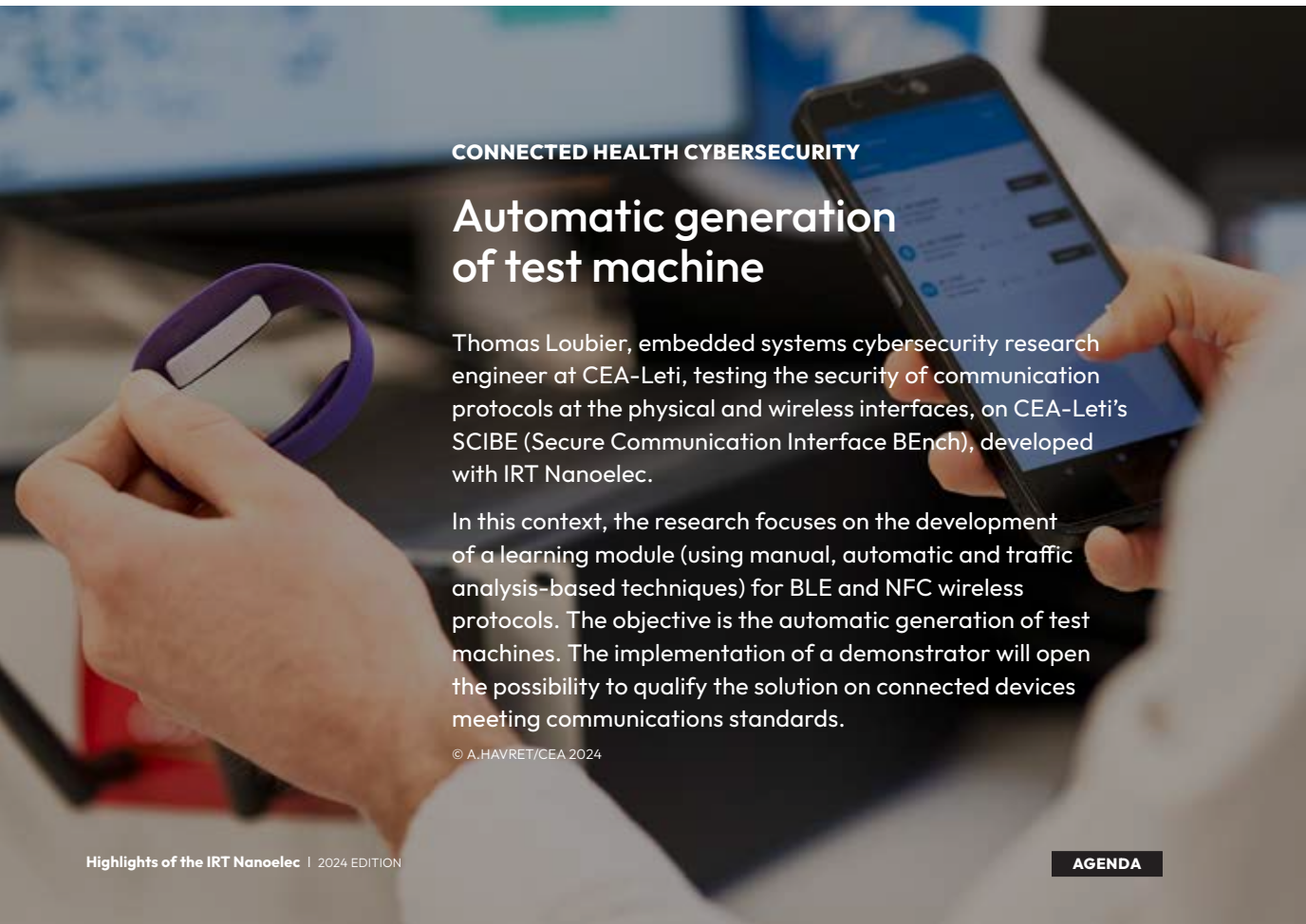
3. Hector, K., Moellic, P.-A., & Dumont, M. (2023, September 28). Fault Injection and Safe-Error Attack for Extraction of Embedded Neural Network Models. ESORICS 2023. European Symposium on Research in Computer Security (ESORICS). SECAI Workshop., The Hague, The Netherlands.

Considering or combining more attack methods would improve the evaluation by simulating a more powerful adversary.



LASER INJECTION BENCH FOR CHARACTERIZING AN EMBEDDED NEURAL NETWORK MODEL.
© CEA





CONNECTED HEALTH CYBERSECURITY

Automatic generation of test machine

Thomas Loubier, embedded systems cybersecurity research engineer at CEA-Leti, testing the security of communication protocols at the physical and wireless interfaces, on CEA-Leti's SCIBE (Secure Communication Interface BEnch), developed with IRT Nanoelec.

In this context, the research focuses on the development of a learning module (using manual, automatic and traffic analysis-based techniques) for BLE and NFC wireless protocols. The objective is the automatic generation of test machines. The implementation of a demonstrator will open the possibility to qualify the solution on connected devices meeting communications standards.

CONNECTED HEALTH CYBERSECURITY

A new open-source hardware processor standard

CEA TEAMS INVOLVED IN NANOELEC PARTICIPATE AT THE ANNUAL EUROPEAN RISC-V6 SUMMIT.

Over 80 million Risc-V cores in the automotive, IoT, and industrial markets by 2025

Unlike the world's most common instruction set architectures (ISA)4, Risc-V is an open-source model5. This means that developers can fully access and modify the architecture, and use it for their own applications. Mikael Carmona, Head of Laboratory for Security of Hardware Components (CEA-Leti), talked to us about the challenges of this technology, poised to become a new standard.

WHAT ARE THE ADVANTAGES OF OPEN-SOURCE MATERIALS AND APPLICATIONS FOR INNOVATIVE ARCHITECTURE?

M.C. By using an open-source instruction set architecture, or ISA, developers can build end-to-end processors since they have full control over material and application components. There are at least two advantages for innovation: first, it offers myriad possibilities to design new, technologically disruptive processors with high performance and security features. Second, part of the development can be shared with a community well beyond the project's initiator. Sharing ensures faster and consolidated development of technology blocks without having to transfer intellectual property rights.

WHAT ROLE DOES RISC-V PLAY IN NANOELEC'S DIGITAL TRUST APPLICATIONS?

M.C. The goal of the Nanoelec/Pulse program is to make Isa Risc-V processors secure; open source ISAs are a means to ensure that their architecture is intrinsically secure. For processors based on a proprietary ISA, any detected vulnerability is fixed by adding a "patch". This leads to a significant cost increase in surface (silica) and performance (time) due to the need for a solution that will directly modify the core and make it resilient.

Against,
MIKAEL CARMONA, HEAD OF LABORATORY FOR SECURITY OF HARDWARE COMPONENTS (CEA-LETI)
© P.JAYET/CEA 2023

4. An ISA defines the set of basic operations (representation and address mode of data types, registers, instructions) to execute computer programs (codes) via a processor.

5.Risc-V stands for Reduced Instruction Set Computing Five, meaning it is a simplified (reduced) version of the set of instructions compared with older, more complex architectures. The term "Five" indicates the fifth version of the architecture.

6.The Risc-V Summit Europe https://riscv-europe.org/

HOW CAN RISC-V STANDARD BE AN ALTERNATIVE TO ARM PROCESSORS, WHICH ARE UBIQUITOUS IN MOBILE PHONES AND TABLETS, AND EVEN IN CERTAIN COMPUTERS?

M.C. The Risc-V Foundation foresees over 80 million Risc-V cores in the automobile, IoT, and industrial markets by 2025. In 2022, ROMA, the first Risc-V laptop, arrived on the market, and Android was able to support Risc-V architecture. As a result, Risc-V has become a direct competitor of ARM in an ecosystem which is powerful (Google, IBM, Samsung) and dense (number of markets and company types).

WHY IS Risc-V NOT AN ISSUE IN THE TRADE WAR BETWEEN THE UNITED STATES AND CHINA?

M.C. An ISA is not the only hardware component of a processor. Although there is no current fight for sovereignty over ISAs, the trade war has nevertheless affected electronic components. One of the goals of the Nanoelec/Pulse program is to design and characterize intrinsically secure Risc-V processors, and therefore gain a competitive edge over current security solutions.

WHAT WERE THE HIGHLIGHTS OF THE 2023 Risc-V SUMMIT EUROPE?

M.C. In Barcelona, we introduced two security innovations for Risc-V processors: ScrambleCache is a highly effective technique for securing the cache of application processors. Safeguarding against cache-based attacks means, for example, protecting the data encryption key on a medical device processor to prevent theft of medical data.

Protecting the data encryption key on a medical device processor to prevent theft of medical data

The memory encryption engine (MEE) encrypts (confidentiality) and authenticates (integrity) data stored in DRAM (or Flash) memory, which then travels to lower-level caches to be executed by the processor. With an additional cost of only 10% on Linux execution latency and 3% on core area used, this innovation offers consistent protection against DRAM and Rowhammer attacks, which can alter data stored in non-volatile memory, and render systems unusable. ◊

CONNECTED HEALTH CYBERSECURITY

Increasing the security of data streams in the IOT

HOW TO MAKE THE PROCESSOR OF A CONNECTED OBJECT RESISTANT AND RESILIENT TO ATTACK.

In his doctoral thesis prepared under the Nanoelec/Pulse program, Gaetan Leplus studied several types of countermeasures to protect the data pipelines of connected objects against fault injection and side channel attacks[7]. *"For example, for the instructions path, we propose a mechanism to mask the current instruction, in which a mask is generated according to the previous instruction"*, he explains, before pointing out that *"this innovative technique effectively secures the instructions at very little extra cost."* ◊

7. "Processor resistant and resilient to fault and side channel attacks" Doctoral thesis at the University of Saint Etienne defended on 18/12/2023, by Gaëtan Leplus

CONNECTED HEALTH CYBERSECURITY

An intrinsically secure processor

A MODULAR DESIGN ALLOWS INTEGRATING ALL THE SECURITY FUNCTIONS.

After carefully identifying the vulnerabilities of the most common processors (microcontrollers, processors for IOT, personal computers and servers) in an award-winning work in 2019[8], a team from CEA-Leti is continuing its work under the Nanoelec/Pulse program on 64-bit NaxRiscV, a Risc-V open standard processor. *"By separately examining each logic level of the processor, we are looking to implement the "intrinsically secure processor" concept. The approach is in response to the worrying exponential increase in attacks and the impossibility of guaranteeing a fault-free software code. It is then up to the intrinsically secure processor to prevent these vulnerabilities from being exploited"*, explains Olivier Savry, a researcher at CEA-Leti. *"The particularity of this highly advanced processor is its modular design: we can thus study countermeasures proportionately to different levels of attack. Our goal is to add to this processor all the security functions we have developed to ensure confidentiality, integrity, authenticity and end-to-end availability type security (from Flash up to execution in the ALU) and in real time."* ◊

Above,
OLIVIER SAVRY, EMBEDDED SYSTEMS SECURITY EXPERT AT CEA, BREIFING ON THE MODULAR DESIGN FOR THE CONCEPT OF AN INTRINSICALLY SECURE PROCESSOR
© A.HAVRET/CEA 2024

8. Olivier Savry, Thomas Hiscock, Mustapha El Majihi "Sécurité matérielle des systèmes", Dunod, 2019

SECURITY OF AUTONOMOUS MOBILE ROBOTICS

Safe and autonomous overhead crane

AN OVERHEAD CRANE WITH GREATER AUTONOMOUS PERFORMANCE THANKS TO ARTIFICIAL INTELLIGENCE.

Within the framework of Nanoelec, the teams from Schneider Electric and Inria are developing a learning pipeline for artificial intelligence dedicated to automatic control of load swinging during autonomous movements by an overhead crane.

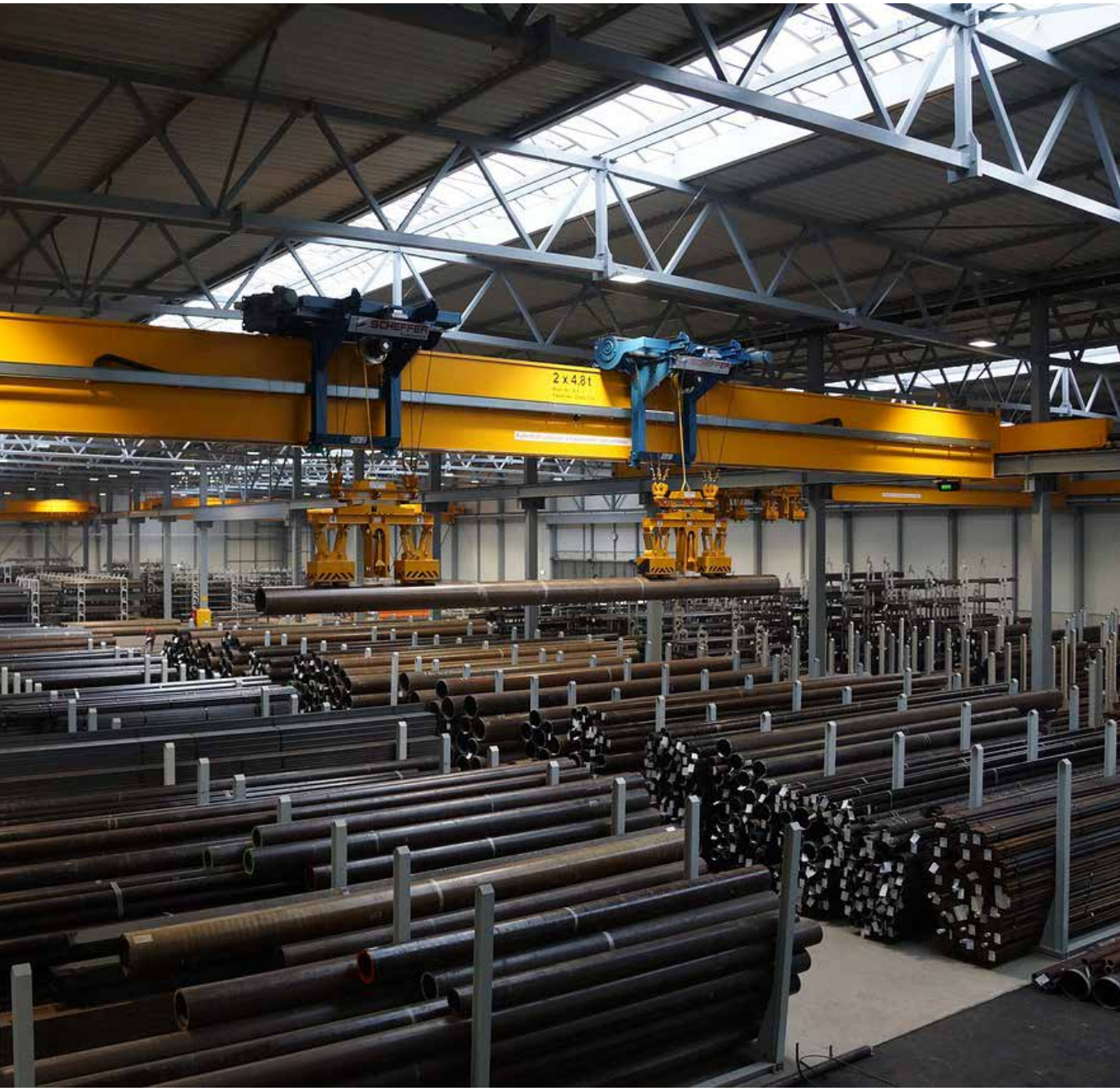
"The aim is to increase the autonomy of the overhead crane without compromising on safety while reducing equipment maintenance and parameter setting times", says Charles Blondel, Head of R&D Dpt of the Industrial Automation Business Unit at Schneider Electric. *"Automation of lifting gear requires the use of advanced sensors, such as scanners and cameras, as well as algorithms to interpret a whole range of data to generate reliable and safe decisions."*

Robotics are increasingly present in plants, notably to achieve productivity and safety gains with respect to the movement of heavy loads.

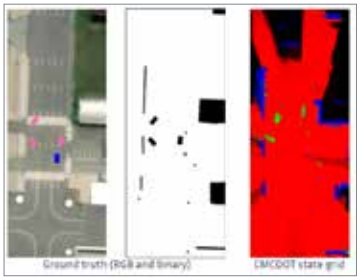
"Autonomous Intelligent Vehicles (AIV) or Autonomous Mobile Robots (AMR) are now integrated into production lines, including with remote sensors around the infrastructure", explains Charles Blondel. It must be possible to integrate this new mobile handling technology without endangering the production line, surrounded by human employees.

Following mathematical modeling of an overhead crane, the teams at Nanoelec defined an approach to the problem of crane control aiming to optimize the parameter settings of the existing controllers. A learning pipeline for AI incorporating a simulator developed by Schneider Electric was then installed.

"We have generated data sets for simulations by varying the system parameters (acceleration, deceleration, maximum linear speed, overall time delay) through the range of coefficients of the control algorithm. A total of 32 distinct crane models was simulated", says Charles Blondel. The next step is to compare these numerical simulations with a physical experimentation platform in order to characterize performance in terms of optimization. ◊



WITHIN NANOELEC, THE TEAMS FROM SCHNEIDER ELECTRIC AND INRIA ARE DEVELOPING A LEARNING PIPELINE FOR AI DEDICATED TO AUTOMATIC CONTROL OF SWINGING OF THE LOADS CARRIED BY AN AUTONOMOUS OVERHEAD CRANE.



Above, to the right,
AUTONOMOUS ZOE TESTING AT TRANSPOLIS FACILITY WITH FAKE PEDESTRIANS IN DIFFERENT SCENARIOS.
© INRIA

Above, to the left,
OCCUPANCY GRIDS GENERATED BY THE PERCEPTION SYSTEM OF AN AUTONOMOUS ZOE, DURING A TEST SCENARIO AT TRANSPOLIS FACILITY, A DEDICATED TEST TRACK FOR VEHICLES. SIMILARITY BETWEEN GROUND TRUTH AND INFERENCE ARE TO BE COMPARED USING THE METRICS PRESENTED AT ITSC 2023.
© INRIA

SECURITY OF AUTONOMOUS MOBILE ROBOTICS

Perception solutions for autonomous vehicles

NEW NAVIGATION-BASED METRICS FOR PERCEPTION SYSTEMS.

Within Nanoelec, Inria has been developing probabilistic perception and navigation systems for autonomous vehicles for years, enabling safe and explainable fusion and filtering of information and decision-making. The systems developed are particularly effective at dealing with multimodal data sources, coming from different types of embedded or deported sensors, making them particullarely well-suited to complex dynamic environments. Thanks to the probabilistic framework used, several prototypes were developed in 2023, including a proper fusion of proven embedded Bayesian methods and data-driven artificial intelligence systems, as well as a realistic infrastructure-vehicle perception fusion. These prototypes are key for innovation projects with industrial partners in diverse use cases.

As explained by Lukas Rummelhard, research engineer at Inria working in the frame of Nanoelec, the current improvement rate in data-driven AI systems might pave the way for the large-scale deployment of autonomous vehicles in certain environments; the spread of such these breakthrough technologies in many other use-cases may be hindered, by a lack of sufficient relevant data and dedicated computing power, or by validation and regulatory concerns.

When developing these probabilistic methods, and in order to progress towards mainstream deployment, particular attention needs to be paid to validation methods, and the definition of the right metrics for their evaluation and characterization. Following research in this field, Jean-Baptiste Horel, PhD student at Inria, presented at ITSC 2023[10], a Navigation-Based Evaluation Metric for Probabilistic Occupancy Grids. *"We proposed a new navigation-based metric for evaluating the similarity of occupancy grids. The metric defines the difference between two occupancy grids as the measured spread between the navigation behavior their use induces, which emphasizes variations in general topology over local occupancy fluctuations. Experimental results on 10,000 driving scenes show the relevance of our approach for quantifying grid disparities compared with existing approaches"*, he states. ◊

10. Horel, J.-B., Baruffa, R., Rummelhard, L., Renzaglia, A., & Laugier, C. (2023). A Navigation-Based Evaluation Metric for Probabilistic Occupancy Grids : Pathfinding Cost Mean Squared Error. ITCS 2023 - 26th IEEE International Conference on Intelligent Transportation Systems, 1-6. https://hal.science/hal-04211125

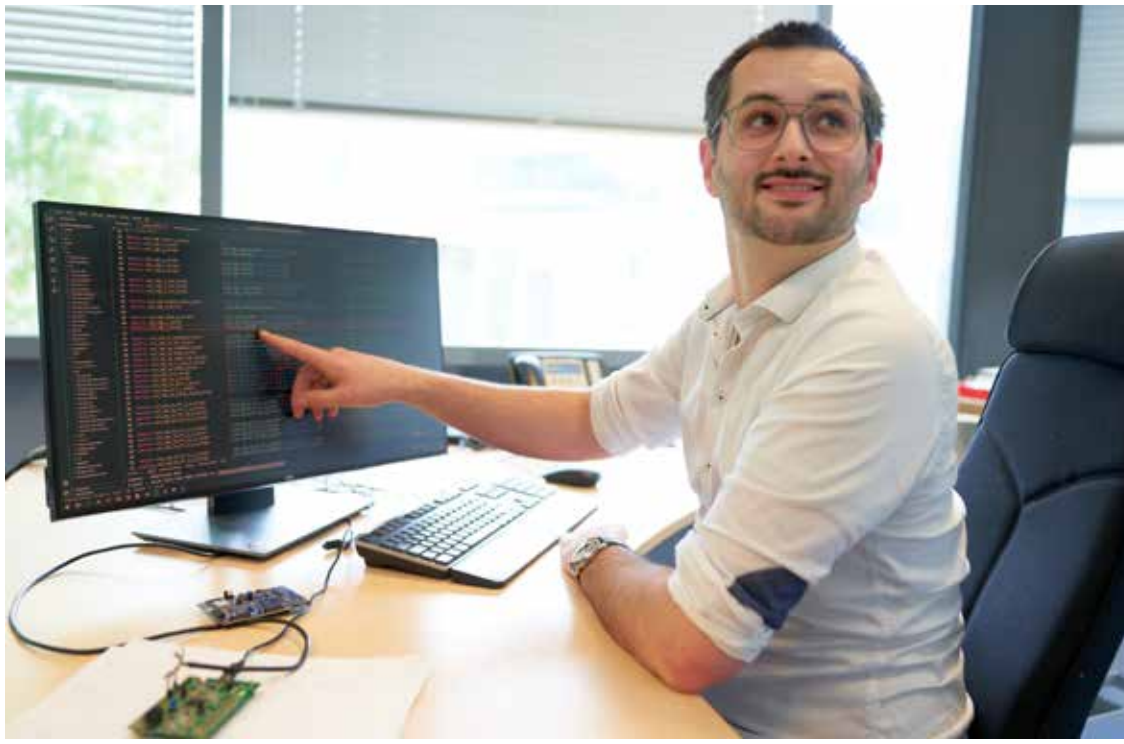
SECURITY OF AUTONOMOUS MOBILE ROBOTICS

Secure hardware implementation of blockchain

Following on from the "blockchain and digital identification" white paper, and in order to envisage the technology readiness level (TRL) of the demonstrators, Nanoelec is a member of the "Alliance Blockchain France" association. Within this framework, Nanoelec showcases its R&D activities aiming to build physical, secure devices to protect our personal data, which can be connected to different systems, including blockchains and smart contracts. *"The challenge is to provide innovative solutions reconciling a high level of security with performance and low-consumption for the PCBs developed, which will be at the heart of tomorrow's personal and industrial devices"*, explains Christine Hennebert, in charge of projects at CEA-Leti.

Ultra-secure critical IoT

Developed at CEA-Leti under Nanoelec, SecIoT comprises an enhanced arsenal of hardware and software security features. It simultaneously ensures object authentication and protection of sensitive data in terms of confidentiality and integrity. The security functions implemented leverage both local capacities and off-the-shelf hardware security components to maximize security and performance. Along with management of encryption keys, automatic recovery and quantum threat protection, SecIoT automatically detects when the case is opened in order to prevent reverse engineering. The demonstrator was presented at the European Cyber Week (ECW) 2022 and at Leti Innovation Days 2023.



Photo,
ANTOINE LOISEAU, CRYPTOGRAPHY RESEARCHER AT CEA-LETI, SHOWS ONGOING DEVELOPMENTS UNDER NANOELEC, TO IMPROVE OVERALL UPSKILLING ON PQC
© A.HAVRET/CEA

CYBERSECURITY OF INDUSTRIAL SYSTEMS

Secure implementation of post-quantum encryption

THROUGH NANOELEC, CEA-LETI TAKES UP THE CHALLENGES OF SECURING ENCRYPTED COMMUNICATIONS IN QUANTUM CRYPTOGRAPHY.

The advent of quantum computing could very well make asymmetric cryptography vulnerable. Today, among other things, this type of cryptography ensures confidential communication on the internet, and integrity of embedded software on critical devices. *"Post-quantum cryptography (PQC)*[11] *will become the standard in the coming years; it will replace current cryptography. The NIST in the United States, the ANSSI in France and the BSI in Germany have initiated the technological and industrial transition of cryptography"*, explains Guillaume Goy (UGA and CEA), who is conducting PhD research on the subject as part of Nanoelec.

"Since 2016, the NIST has conducted a selection process for cryptosystems that can resist attacks from quantum and traditional computers[12]*. The goal of the competition-like process is to identify the most secure and effective cryptographic schemes, and to establish standards by 2024"*, explains Antoine Loiseau, PQC specialist at CEA who oversees the research that CEA and UGA are conducting with STMicroelectronics. *"The selections that the NIST has made among research teams all around the world, from 2016 until today, are proof of the difficulty of the task."*

11. Cryptography aims to ensure data security against quantum-computing attacks.

12. US National Institute of Standard & Technology https://csrc.nist.gov/projects/post-quantum-cryptography

The Nanoelec implementation offers a much higher optimization level than the standard scheme.

Below,
WITHIN NANOELEC, RESEARCHERS FROM CEA, UGA AND STMICROELECTRONICS HAVE PUBLISHED A FIRST LEVEL OF OPTIMIZATION FOR THE IMPLEMENTATION OF A COMMUNITY-ACCLAIMED STANDARDIZED POST-QUANTUM ALGORITHM (NIST COMPETITION), IN OPEN SOURCE
© CEA

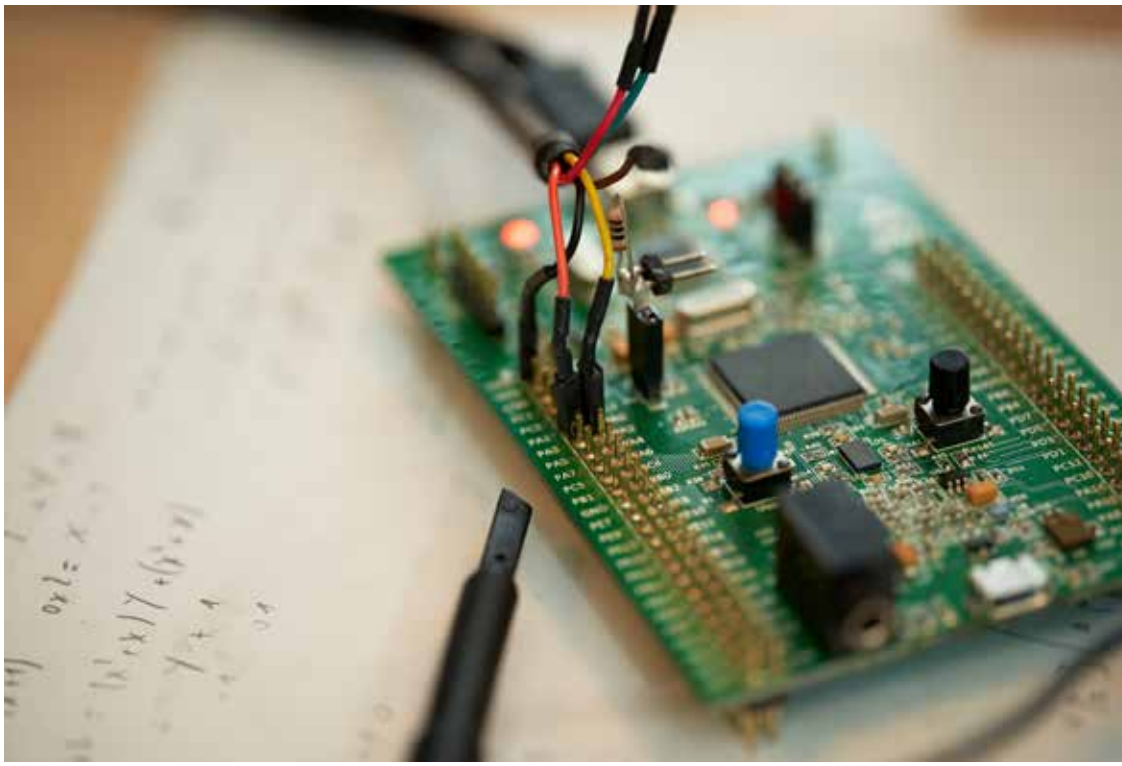
Nanoelec/Pulse program partners have decided to examine one of the standardization approaches selected by the NIST: Hamming Quasi-cyclic (HQC). *"By choosing to work on a specific system, our goal was to improve overall upskilling on PQC, and to obtain concrete results pertaining to a given cryptosystem"*, adds Antoine Loiseau.

"In comparison with the state-of-the-art scientific literature review, we have a 40 to 60% better performance rate in terms of computing time, and a 70% smaller memory footprint", declares Guillaume Goy.

The same team carried out an optimized HQC implementation for their embedded system on an STMicroelectronics STM32U5 microcontroller (available on the market), adapted to an embedded device (portable medical device, household appliance, industrial sensor), and including hardware security primitives. *"As a result of these tests, we were able to truly observe the impact of our modifications by comparison with the standard implementation"*, continues Antoine Loiseau. Conclusion: The Nanoelec implementation offers a much higher optimization level than the scheme's standard implementation.

"Nanoelec helped us to anticipate the future roll-out of post-quantum cryptography in our products. We were able to have discussions and actively collaborate with academic partners from UGA and CEA", adds Serges Veyres, Partnership & Ecosystem relations Director, at STMicroelectronics Microcontrollers and Digital IC's Group Grenoble.

The research was published in open source so that the entire community could benefit from the performance implementation for an embedded system. ◊



We are looking to take our IoT cybersecurity culture further, firstly for our teams, but also for our customers.

Photo,
PREPARING A TEST AT THE WONDERICS PLATFORM FOR CYBERSECURITY THREAT AT INDUSTRIAL CONTROL SYSTEMS
© P.JAYET/CEA

13. The WonderICS platform installed under Nanoelec at CEA-Leti, consists of a hardware-software co-simulation environment designed to alert the public and professionals to the cybersecurity threat to industrial control systems and experiment with innovative security solutions. It includes a System of control and data acquisition (Scada).

CYBERSECURITY OF INDUSTRIAL SYSTEMS

Simulating cyberattacks on industrial control systems

SCHNEIDER ELECTRIC ACQUIRES A SIMULATOR TO REINFORCE ITS CYBERSECURITY CULTURE.

In 2023, an association of the teams at Schneider Electric and CEA within Nanoelec duplicated and adapted a part of the WonderICS[13] industrial IoT cybersecurity platform at the Schneider Electric R&D Energy Management center. *"The information system part of the WonderICS platform was duplicated on the installation used to demonstrate the hospital zone of our Customer and Innovation lab"*, explains Laurent Crémillieux, Europe partnerships director and Nanoelec correspondent at Schneider Electric. *"By acquiring a cybersecurity demonstrator on our commercial electrical installations, we are looking to take our IoT cybersecurity culture further, firstly for our teams, but also for our customers."* ◊

CYBERSECURITY OF INDUSTRIAL SYSTEMS

Microprocessor security

EMBEDDED SUPERVISION CAN DETECT A VARIETY OF ATTACKS.

For several years now, work has been done on the combination of AI with hardware information to detect micro-architecture attacks, such as Spectre or Rowhammer, but also attacks with an impact on the system, such as a cryptolocker. *"Under the Nanoelec/Pulse program, we are enhancing this work by integrating this type of solution into a generic embedded system representative of an IoT or I-IoT gateway"*, explains Victor Breux, in charge of AI in the project at CEA-Leti, in the frame of Nanoelec. The embedded target chosen for these developments is the STM32MP1 microprocessor from STMicroelectronics which has two Cortex-A7 cores. ◊

CYBERSECURITY OF INDUSTRIAL SYSTEMS

Digitalizing products and services for SMEs

FROM JANUARY 2020 TO MARCH 2023, ISABELLE CHARTIER (CEA-LETI) COORDINATED DIGIFED, A PROJECT DEVELOPED IN CONJUNCTION WITH IRT NANOELEC, AND FUNDED BY THE EUROPEAN COMMISSION. THIS IS HER TAKE ON A COLLECTIVE EXPERIENCE THAT INCLUDED TWELVE PARTNERS AND CASCADE FUNDING SCHEMES.

IS DIGIFED SOMEWHAT SIMILAR TO NANOELEC/EASYTECH, BUT AT A EUROPEAN LEVEL AND WITH THE GOAL OF FOSTERING CROSS-BORDER COLLABORATIONS?

I.C. Yes, it is similar in the sense that we champion small projects: we have provided support for SMEs with a maximum budget of €70,000 to develop a demonstrator within a year or more. Projects must be developed with a partner from another country (cross-border collaboration): another SME, or a Digifed partner contributing a technological block.
Projects covered a wide range of fields: automation of pollen analyses for honey producers (Spain/Greece), optimization of dental implants (Spain/Romania), and electric vehicle chargers (Slovakia/Czech Republic).

WHAT OPERATIONAL CONTRIBUTIONS DID IRT NANOELEC BRING TO DIGIFED?

I.C. Digifed is made up of twelve partners, three of which are Nanoelec consortium members: Minalogic provided innovation/management assistance; as digitalization often entails changes in a company's business model. CEA-Leti and STMicroelectronics contributed their technical expertise, particularly a kit of ready-to-use and secure blocks for SMEs: a secure gateway[14] based on secure STMicroelectronics components (STM32MP1).

WHY IS DIGITAL TRUST THE PROJECT'S MAIN FOCUS AREA?

I.C. We have supported projects for companies that specialize in data security and communication (CYSEC in Switzerland), others in agrifood industry logistics (NGS in Italy) — security is important for the legal aspects of cold chain control — and others in healthcare (Panoramic Digital Health in France), all of which require digital trust for data confidentiality and integrity.

A new cascade funding mechanism aims to improve the safety of individuals in the workplace by using robotics and AI.

Thanks to Digifed we have also initiated a novel collaboration mode called Generic Experiment. Its goal is to rally an SME community around a research center in order to enhance mutual knowledge and initiate future collaborations. CEA and STMicroelectronics led a community discussion on cybersecurity with a focus on secure gateway design standards. CEA/Y.Spot initially led the group to define common objectives. Technical developments — co-funded by the Easypoc program and the Auvergne-Rhône-Alpes region — helped to set up algorithms that detect intrusions and cyberattacks. Five SME community members were able to test the prototype.

WHY DID DIGIFED MAKE CROSS-BORDER COLLABORATION A PRIORITY?

I.C. There are many funding opportunities for French SMEs that want to work with a French research center. It is much more difficult for an Irish SME, for example.
We therefore focused on small consortiums with two SMEs from different countries. Our idea was greatly appreciated; companies made joint progress. It also fostered collaborations between mid caps and big groups, which otherwise would not have obtained funding. In addition, we funded a consortium between an SME and a large group via a new tool called Digital Challenge.

HAS THE EUROPEAN COMMISSION RECOGNIZED YOUR APPROACH?

I.C. Yes. DigiFed followed three cascade funding projects (EuroCPS, GateOne and FED4SAE) which ensured upskilling and the optimization of funding processes for SMEs. In 2023, as part of Nanoelec, CEA-Leti was selected to coordinate a new project called Earashi[15]: a new cascade funding mechanism that aims to improve the safety of individuals in the workplace by using robotics and AI. ◊

14. https://digifed.org/news-events/success-stories/segway-cysec/
15. https://earashi.eu/open-calls/

PULSE AT INTERNATIONAL EVENTS

ESISAR ENGINEERING SCHOOL (GRENOBLE INP-UGA) GATHERED EU CHALLEGERS OF THE CSAW, ONCE AGAIN IN 2023, WITH SUPPORT FROM NANOELEC.
© GRENOBLE INP-UGA

→ CSAW 2023

The 20th edition of Cyber Security Awareness (CSAW) was held **last November 9 and 10 at Grenoble INP-UGA/Esisar**, and was also the 7th anniversary of CSAW Europe. This event stands at the crossroads between competition and discovery of cybersecurity, with the European final this year being held once again in Valence by Grenoble-INP/Esisar and the LCIS laboratory, with the support of Valence Romans Agglo and Nanoelec.

PULSE AT INTERNATIONAL EVENTS

MASTERCLASS BY MR. EL MAJIHI AT FIC 2023
© DR

→ FIC 2023

The International Cybersecurity Forum (FIC) has established itself as **the reference event in Europe for digital security and trust.** The 15th edition was held in Lille from April 5 to 7, 2023. This year, the FIC welcomed more than 16,000 participants, 650 exhibitors and 50 international delegations around 250 conferences and roundtables. A masterclass was organized by the members of Nanoelec/Pulse on the subject of cache memory security against software side channel attacks.

NANOELEC STAND WITH SCRAMBLECACHE (Risc-V) DEMONSTRATOR AT THE Risc-V SUMMIT 2023
© DR

→ Risc-V Summit

The teams from the Nanoelec/Pulse program took part in organizing the **1st Risc-V Summit Europe, held in Barcelona from June 5 to 9, 2023.** Following the success of the previous French editions supported by Nanoelec, this event has taken on a European dimension this year and attracted more than 500 participants from around the world, with more than 40 plenary sessions and representatives from industry and the university world throughout Europe, covering key vertical markets such as aerospace, AI/ML, automotive, data centers, embedded components, HPC, security, etc. It was an opportunity for PULSE to present its work around intrinsically secure application processors and notably the ScrambleCache demonstrator on its stand.

→ ECW 2023

European Cyber Week (ECW) is a **European-wide reference event in the strategic fields of cyber defense, cybersecurity and artificial intelligence.** For its 8th edition, ECW 2023 was held from November 21 to 23, 2023 in Rennes and attracted more than 6,000 participants and 120 exhibitors. It was an opportunity for the PULSE program to present its work on intrinsically secure application processors and the SCIBE (Secure Communication Interface BEnch).

ONE OF THE EIGHT POSTERS ON THE THEME **"MICROELECTRONICS FOR LIVING IN A BETTER WORLD"** CREATED BY THE STUDENTS FROM THE BRASSART-GRENOBLE SCHOOL FOR TECH&FEST 2024.
POSTER BY LAURIE DECHAUX-BLANC, "GRAPHIC DESIGN" STUDENT

Characterisation

Correlative microscopy

ENNIO CAPRIA
DEPUTY HEAD OF BUSINESS DEVELOPMENT AT ESRF AND DIRECTOR OF THE NANOELEC CHARACTERISATION PROGRAM

In 2023, teams of the Nanoelec/ Characterisation program explored the potential of novel correlative microscopy methods combining several instruments available in Grenoble ecosystem.

Through the Nanoelec Characterisation program, industrial firms and researchers have access to top-notch tools to study the effects of ionizing radiation on components and systems, to characterise the properties of their materials contributing to the quality of their products and processes. Thanks to the high penetrating power of neutrons and X-rays, these evaluations can be performed non-destructively, without the need to open or damage the objects, and in many cases while in operation.

2023 is marked by several achievements in close collaboration with the industrial partners. The synchrotron beams at the ESRF were used to define the operating scope of the facility installed on line ID09, for irradiating different types of electronic circuits.

Our teams also explored the potential of novel correlative microscope methods between instruments available at the ESRF and at the CEA-Leti's nano-characterisation platform. In particular a complete process for the characterisation of defects in the SiC has been demonstrated. Finally, research into innovative materials is opening the door to more structured expansion of the methodology to other fields of application, like the one of energy (mainly battery).

This year, we participated extensively in various scientific events. More particularly, we organized the very first French symposium on characterisation, with five other member institutes of the FIT, and we were associated with the G-Radnext European symposium at the Cern, on the topic of irradiation. Since the end of 2023, Nanoelec has been a member of the *Centre français de fiabilité* (French reliably center), a group of systems and electronic components reliability experts. This further enhances our presence in the expertise networks.

NANO-FOCUSING ON ID01 BEALINE AT THE ESRF DEDICATED TO MICRODIFFRACTION IMAGING

LARGE SCALE INSTRUMENTS FOR CHARACTERISATION AT A GLANCE

→ VISION

The unmatched performance of large-scale instruments must be identified by industrial users as a cutting-edge tool to perform advanced characterisations of electronic components and devices

→ AMBITION

Develop a competence center for testing radiation hardness of electronic components and systems

→ MISSION

Continue to make unique scientific instruments & methodologies available to meet the new challenges of the electronics industry for the serenity and sovereignty of the digital transition

→ PARTNERS

CEA
CNRS/LPSC
ESRF
ILL
Schneider Electric
Soitec
STMicroelectronics
Iroc Technologies

IRRADIATION

Resistance to irradiation of electronic components and circuits

IRRADIATION CAMPAIGNS UP TO 5 MRAD WERE PERFORMED ON ESRF/ID09 BEAMLINE.

The particularity of the ESRF/ID09 beamline is its ability to select isolated X-ray pulses, which was used in 2023 to irradiate different types of electronic circuits, based on silicon, SiC and GaN technologies, whether test circuits or actual commercial components.

"Successful irradiation campaigns were run on several fronts at ID09, in 2023", says Philippe Roche, Company Fellow Radiation and R&D Sr. Director High Reliability at STMicroelectronics. *"We tested shift registers and integrated dosimeters, as well as advanced digital CMOS processors and new-generation image sensors. Irradiation campaigns with doses of up 5 Mrad enabled us to test advanced components in chips."*

Customized sample-holders make it easier to adapt the experimental configurations, while the ultra-focused beamline is capable of precisely examining standard and robust blocks. The measurements accessible on ID09 can be used to determine what events can be induced in these electronic circuits using single X-ray pulses, in differing conditions, and to establish correlations with results obtained on other qualifying installations – such as the heavy ion beams for total ionizing dose (TID) tests and single event effects (SEE)[1]. ◊

Photo,
ON ID09 (ESRF), CUSTOMIZED SAMPLE-HOLDERS MAKE IT EASIER TO ADAPT THE EXPERIMENTAL CONFIGURATIONS, WHILE THE ULTRA-FOCUSED BEAMLINE CAN PRECISELY EXAMINE STANDARD AND ROBUST BLOCKS
© S.CANDE/ESRF

1. Single Event Effects (SEEs) are caused by a single, energetic particle, and can take on many forms. As an example, spacecraft designers have to be concerned with two main causes of Single Event Effects (SEEs): cosmic rays and high-energy protons.

LARGE MULTIMODAL & MULTISCALE CHARACTERISATION

Defects in SiC epitaxial wafers

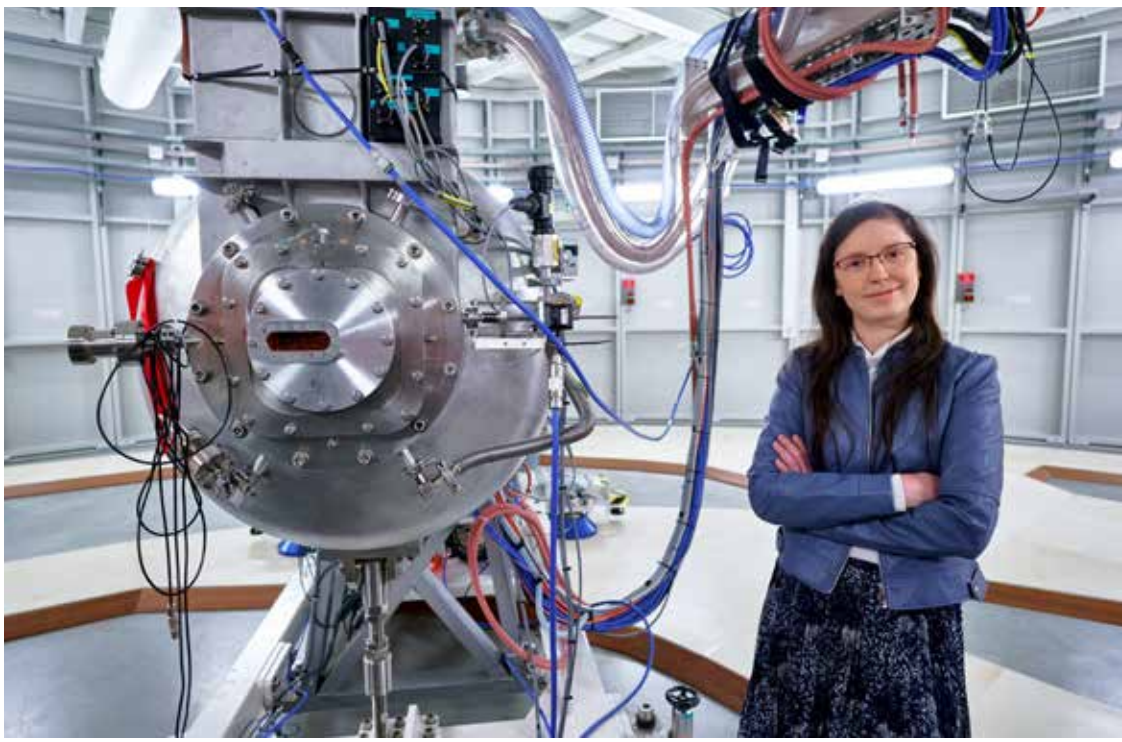
KEEPING THE SAME REFERENCE SYSTEM OF EPITAXIAL CRYSTALS, WAFERS WENT THROUGH SIX DIFFERENT CHARACTERISATION PLATFORMS.

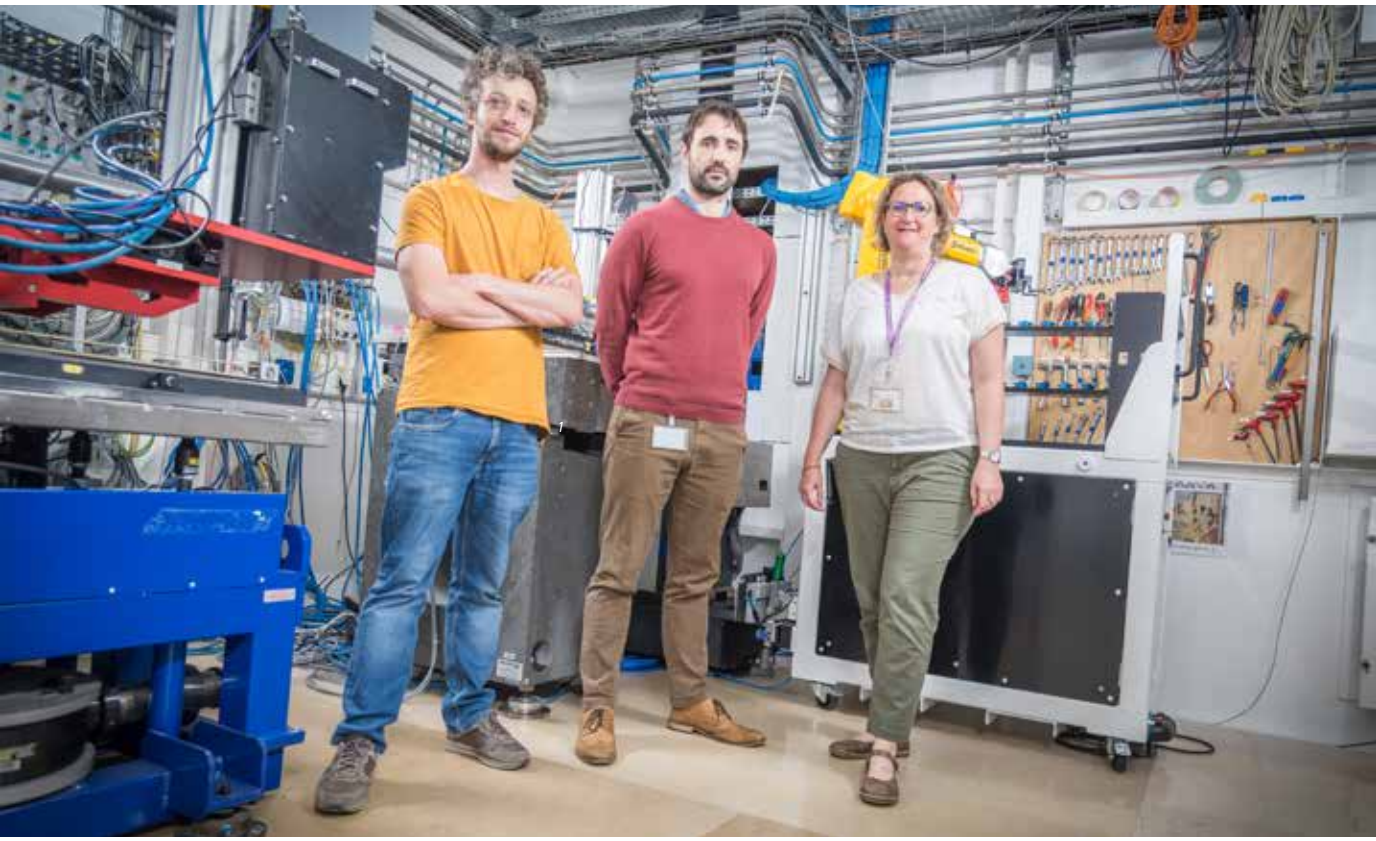
A team from ESRF and CEA visualized and quantified crystalline defects and induced strain on homoepitaxial SiC wafers[2]. *"We used a correlation microscopy platform, with the implementation of a multimodal/multiscale approach"*, says Rébecca Dowek, engineer at the ESRF. Under the Nanoelec/Characterisation program, a large selection of techniques were combined while keeping the same reference system of epitaxial crystals coordinates throughout the experiments: XRD topography and microscopy with synchrotron beams from different beamlines of the ESRF, photoluminescence, cathodoluminescence, Electron Channeling Contrast Microscopy, Focused Ion Beam (FIB) and Transmission Electron Microscopy (TEM).

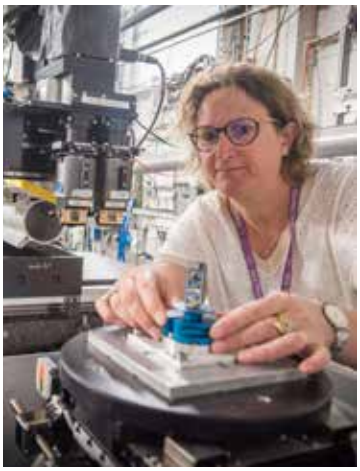
"We investigated four categories of defects in the epitaxial layers: dislocations, extended crystal defects, deformation and curvature of the crystal matrix and topography defect) and demonstrated the possibility for correlations in multi-characterisation", adds Rebecca Dowek. ◊

2. Epitaxial layers on wafers dedicated to power applications

Below,
REBECCA DOWEK, POST-DOCTORATE ON MULTI-CHARACTERISATION OF DEFECTS IN SILICON CARBIDES (SIC)
© A.HAVRET/CEA







Above,
SIMON BENICHOU, FABIEN LEONARD AND ELODIE BOLLER ARE COMMITTED FOR TOMOGRAPHY ANALYSIS AT ESRF BM05 BEAMLINE

CORRELATIVE MATERIAL CHARACTERISATION

Investigating defects in diamond

WITH A NEW SETUP AT THE ESRF BM05 BEAMLINE, X-RAY BEAM INDUCED CURRENT (X-BIC) ANALYSIS BRINGS CORRELATIONS BETWEEN THE CHARGE COLLECTION EFFICIENCY AND DEFECTS IN THE MATERIALS.

A new instrument capable of performing correlative analyses between XBIC (X-ray Beam Induced Current) and topography is now operational at the ESRF BM05 beamline. *"We successfully developed and implemented a new XBIC setup that allows characterisations of semiconductors. This technique was shown to be complementary to existing techniques (like RCI, spectroscopy, XRF microscopy, etc.). The characterisation of different diamond samples enabled us to identify the correlations between the charge collection efficiency and defects like dislocations, growth boundaries and growth sectors, impurities, and color centers*", explains Thu-Nhi Tran-Caliste, engineer for industrial users at the ESRF, who took part in the study[3] for the Nanoelec/Characterisation program.

Further investigations are already scheduled with other semiconductors materials (GaN, SiC or CdTe) to fully evaluate the potential of this technique coupled with Bragg diffraction imaging.

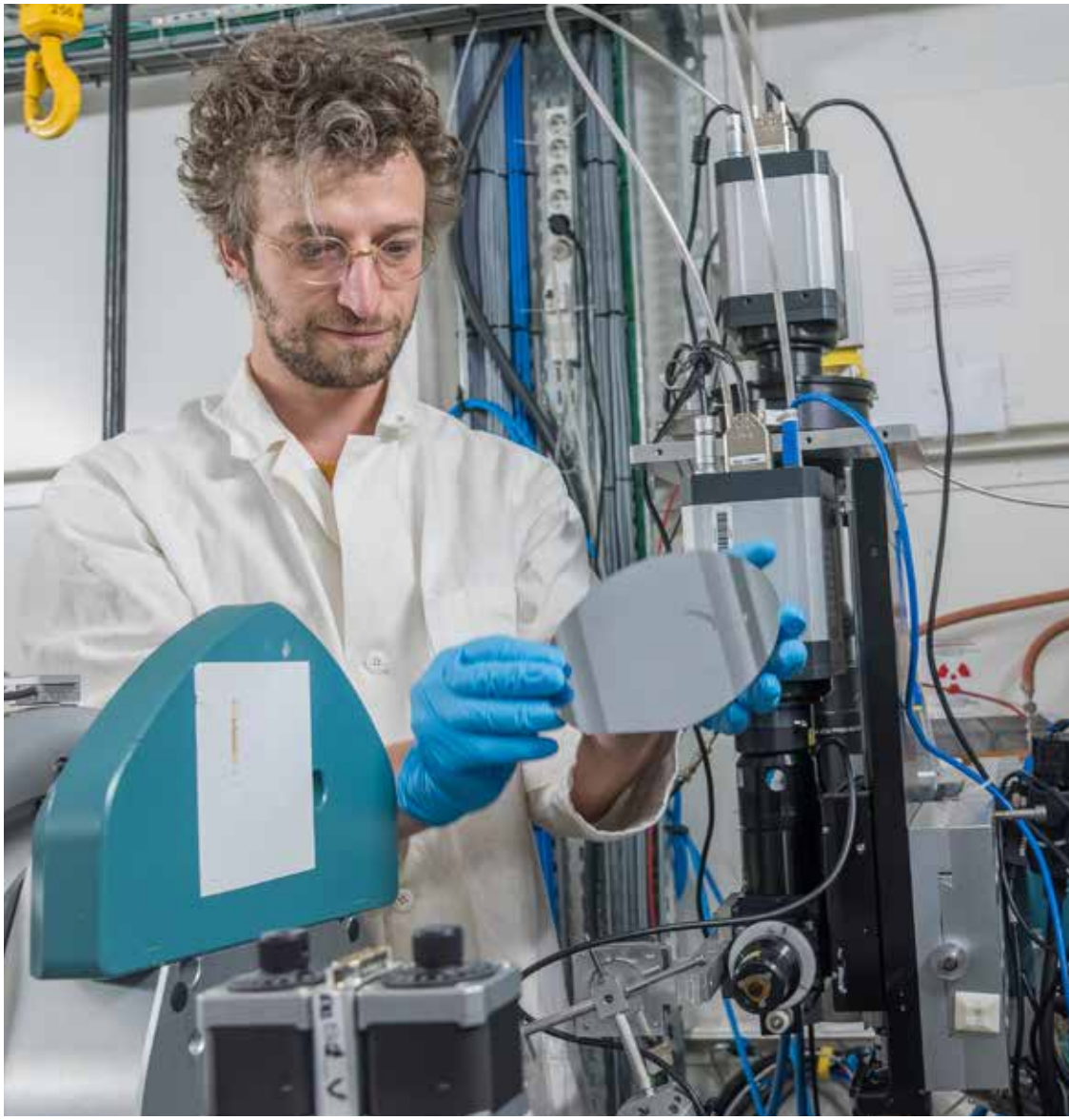
The novel correlative microscopy methodologies for semiconductor substrates, together with its first results, have been presented at the International Conference on Functional Materials for Sustainable Energy and Environment (INSC FMSEE)[4] as well as at the European Materials Research Society (EMRS) Spring meeting[5]. ◊

Photo,
SIMON BENICHOU AND THU NHI TRAN-CALISTE ARE OPERATING NANOELEC GIANT GONIOMETER FOR X-RAY REFLECTOMETRY AND DIFFRACTOMETRY AT ESRF BM05 BEAMLINE
© O.DEVISE/CEA

3. Lafont, F., Baruchel, J., Bousquet, J., Capria, E., Celestre, R., Cotte, M., Dauvergne, D., Everaere, P., Gallin-Martel, M. L., Hoarau, C., Ibourk, O., Letellier, J., Molle, R., Muraz, J.-F., Nusimovici, D. Z., Reynaud, M., & Tran-Caliste, T. N. (2023). A new X-ray beam induced current setup, coupled with X-ray diffraction imaging, for diamonds and semiconductors characterisation by synchrotron techniques at ESRF. Diamond and Related Materials, 140, 110454. https://doi.org/10.1016/j.diamond.2023.110454

4. Lafont, F., & Caliste, T. N. T. High spatial resolution structural characterisation of novel semiconductor substrates. INSC FMSEE. https://icamsee2023.sciencesconf.org/

5. Lafont, F., & Caliste, T. N. T. (s. d.). Novel correlative microscopy methodologies for semiconductor substrates. EMRS Spring edition. https://www.european-mrs.com/meetings/archives/2023/2023-spring-meeting



Above,
SIMON BENICHOU PREPARES A WAFER TO BE SCANNED AT ESRF. AT BM05, A FIVE-CIRCLE COMMERCIAL DIFFRACTOMETER (3 CIRCLES FOR SAMPLE ORIENTATION, 2 CIRCLES FOR DETECTORS) IS AVAILABLE TO ADDRESS THE HIGH-THROUGHPUT MULTI-CHARACTERISATION R&D RAPID-ACCESS NEEDS OF THE ELECTRONICS INDUSTRY

IRRADIATION

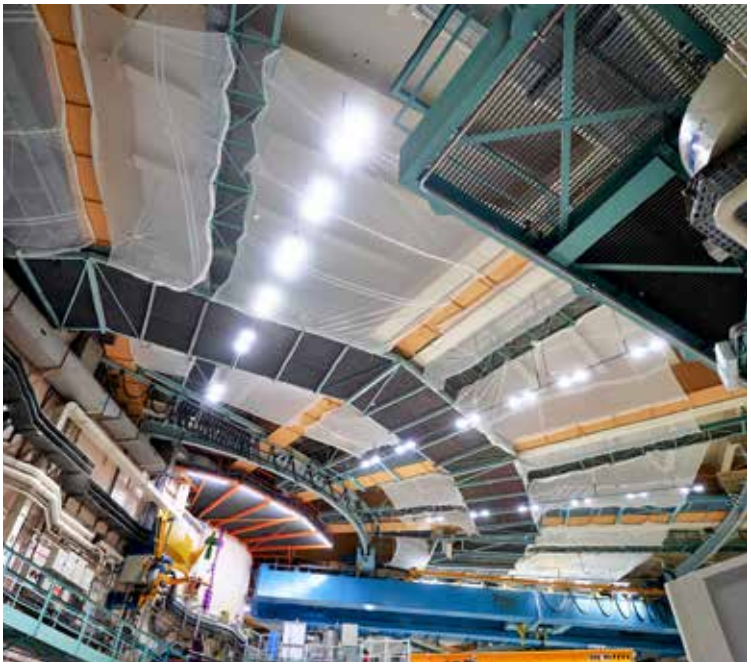
Single-event upsets induced by thermal neutrons in SRAMs

NO NEED FOR A VERY LARGE AMOUNT OF NITRIDES TO CAUSE A SUBSTANTIAL NUMBER OF UPSETS IN SRAMS.

Investigations of single-event upsets (SEU)[6] induced by thermal neutrons continued in 2023 at the Thermal and Epithermal Neutron Irradiation Station (TENIS ILL/ Nanoelec beamline)[7]. Thermal neutrons are an important contributor to any radiation environment where spallation reactions and neutron moderation are involved. This is the case of the atmosphere (ground level to flight altitudes) as well as of high-energy physics accelerators. Thermal neutrons can trigger single-event upsets (SEUs) in memory-based devices through indirect ionization following their nuclear absorption in ^{10}B atoms that may be present within or near to sensitive cells.

Combining experiments at Tenis, as part of the Nanoelec/Carac program, with simulations, a pan-European collaboration was published in the IEEE Transactions on Nuclear Science Review[8]. *"We introduce the possibility that thermal neutron SEUs may not only be caused by the interaction with ^{10}B in the proximity of the SV, but also by the interaction with ^{14}N that may result in the release of low-energy protons (LEPs)[9]"*, explains Andrea Coronetti (Cern) as the first author of the paper.

Typically, nitrogen is used in thin barrier layers made of TaN or TiN or even as an insulator in the form of Si3N4.



Photo,
ROOF OF THE ILL EXPERIMENTAL HALL, ABOVE THE NANOELEC/ TENIS BEAMLINE (THERMAL AND EPI-THERMAL NEUTRON IRRADIATION STATION)
© A.HAVRET/CEA 2024

6. The terms single-event upset (SEU), single-event effect (SEE) or single-event latch-up (SEL) refer to the highly localized deposition of energy by single particles or their reaction products causing adverse effects in a sensitive node of a microelectronic device.

7. In 2023, ten external experiments took place on the TENIS instrument (Thermal and Epi-Thermal Neutron Irradiation Station), although the ILL reactor did not deliver any neutrons from October 2021 to March 2023, due to a major maintenance and upgrade program.

8. Coronetti, A., Alía, R. G., Lucsanyi, D., Letiche, M., Kastriotou, M., Cazzaniga, C., Frost, C. D., & Saigné, F. (2023). An Analysis of the Significance of the 14N(n, p) 14C Reaction for Single-Event Upsets Induced by Thermal Neutrons in SRAMs. IEEE Transactions on Nuclear Science, 70(8), 1634-1642. https://doi.org/10.1109/TNS.2023.3239407

9. When a capture of thermal neutrons releases low-energy protons into the material.

Richard Davies, Industrie application scientist at ILL & Nanoelec/Carac program and Emmanuel Atukpor, ILL research engineer responsible for Nanoelec/Tenis beamline are preparing a setup for the next run of irradiation.

The presence of nitrogen in these thin barrier layers can be enough to justify the experimentally observed thermal neutron SEU cross-section for a static random access memory (SRAM). Nevertheless, the expected SEU cross-section from thermal neutrons is usually a few orders of magnitude lower than that of high-energy particles, and does not therefore represent a major threat in atmospheric applications. At the same time, for high-energy accelerators, the contribution to the total soft error rate could become substantial, although easy to handle by means of margins.

"The devices that may be affected are therefore only those showing a marked sensitivity to LEPs. At the same time, there is no need for a very large amount of nitrides (TaN, TiN, or Si3N4) to cause a substantial number of upsets in these kinds of devices", warns Andrea Coronetti. ◊

Photos,
EMMANUEL ATUKPOR, ILL RESEARCH ENGINEER RESPONSIBLE FOR NANOELEC/TENIS BEAMLINE
© A.HAVRET/CEA 2024

IRRADIATION

Challenging the reliability of Commercial-Off-The-Shelf items for the New Space

SINGLE EVENT EFFECTS HAVE BEEN INVESTIGATED IN A COMMERCIAL FPGA (ARTIX).

We designed, set up and used a modeling tool to predict the device's sensitivity.

Photo,
POSTIONING THE SAMPLE HOLDER FOR AN IRRADIATION EXPERIMENTATION AT THE NANOELEC/TENIS BEAMLINE AT THE ILL
© A.HAVRET/CEA

In recent years, a state-of-the-art trend has emerged in space activities to present a new paradigm for the space ecosystem by developing the technologies and approaches used in the traditional space industry; it is known as "New Space". Thus, some FPGAs based on Static Random Access Memory (SRAM) are widely deployed in satellites and other spacecraft. Hence, new companies are adopting flexible, economical, and high-performance devices as they play a significant role in space missions. Among these, Commercial-Off-The-Shelf (COTS) devices are increasingly used to meet critical demands as they can satisfy reliability criteria.

"The effects caused by space radiation are a growing issue that poses a threat to the proper functioning of COTS SRAM-based FPGAs. Indeed, particles such as protons and neutrons existing in aerospace environments can induce Single Event Effects (SEEs)", underlines Golnaz Korkian, at Computense (University of Madrid). In association with his colleagues from Onera and the ILL, he investigated SEE sensitivity under thermal neutrons and different incident angles of a COTS 28nm SRAM-based FPGA. The experiments were conducted at the new Thermal and Epithermal Neutron Irradiation Station (TENIS), under a Nanoelec/Carac program.

"Our results are compared with 14.2-MeV neutrons, demonstrating a considerable difference in the device's sensitivity against both irradiation sources. Finally, we designed, set up and used a modeling tool to predict the device's sensitivity under the same environmental conditions. The experimental results obtained will show good and highly accurate alignment with the predicted results", summarizes Golnaz Korkian. Results have been published in Microprocessors and Microsystems[10]. ◊

10. Fabero, J. C., Korkian, G., Franco, F. J., Hubert, G., Mecha, H., Letiche, M., & Clemente, J. A. (2023). SEE sensitivity of a COTS 28-nm SRAM-based FPGA under thermal neutrons and different incident angles. Microprocessors and Microsystems, 96, 104743. https://doi.org/10.1016/j.micpro.2022.104743

A COMMON AMBITION

A national symposium on characterisation

CARAC 2023, INITIATED BY NANOELEC, IN COLLABORATION WITH FIVE OTHER IRTS AND ITES, WAS HELD IN PARIS IN NOVEMBER 2023, UNDER THE FIT BANNER.

On 21 November 2023, researchers and industry were given an opportunity to discover the full range of characterisation expertise of the technological research institutes and the energy transition institutes with the aim of building confidence for industry: systems reliability, analysis of failures and materials.

During the course of this day in Paris, a number of subjects were documented and discussed via numerous application examples, both with regard to materials and to integrated systems. Two questions were debated: one on the efficient use of characterisation data, the other on their implementation in a sustainable and responsible development approach.

By jointly organizing this unprecedented technical event together, the Nanoelec, Saint Exupéry and Railenium IRTs and the IPVF, SuperGrid Institute and Ines.2S[11] ITEs clearly stated a common ambition by presenting their complementary characterisation capabilities to contribute to building confidence within industry. An initial catalogue of the characterisation offerings from the institutes was published on this occasion, along with a live webinar by the laboratories of the institutes concerned. During the symposium, a series of four sessions provided an overview of the tools available and the challenges for the coming years. The day attracted about a hundred experts. ◊

Complementary characterisation capabilities to contribute to building confidence within industry.

Photo,
THE DIRECTORS GENERAL OF THE SIX FIT INSTITUTES DURING THE CONCLUSION OF THE NATIONAL CARAC SYMPOSIUM, IN NOVEMBER 2023
© L.GODART/CEA

11. Member Institutes of the FIT association: French Institutes of technology

Photo,
TIME-OUT FOR A GROUP SHOT AT THE G-RADNEXT WORKSHOP, IN 2024
© DR

NETWORKING IN EU

A european irradiation workshop

TWO DAYS OF SCIENTIFIC AND TECHNICAL DISCUSSIONS ON RADIOLOGICAL RESISTANCE TESTING OF SEMICONDUCTOR DEVICES AND SYSTEMS FOR INDUSTRY.

Together with the Radnext[12] project and the Radecs[13] association, the Nanoelec/Characterisation program jointly organized the third edition of the G-RADNEXT workshop at the Cern in Geneva, for the first time in person. This is an event dedicated to professionals in the radiation resistance of electronic components. Over the course of these two days, the participants had the opportunity to attend numerous talks by experts covering various aspects of the irradiation of electronic components.
The program included a session devoted to young scientists as well as visits of the Cern. ◊

12. Radnext is an H2020 INFRAIA-02-2020 infrastructure project with the objective of creating a network of facilities and related irradiation methodology for responding to the emerging needs of electronic components and systems irradiation. https://radnext.web.cern.ch/

13. Radecs association promotes basic and applied science and research in the field of radiation and its effects on materials, components and systems, especially for relevant industries: space, civil nuclear and military applications. https://www.radecs-association.net/steering/

NETWORKING IN FRANCE

French reliability center

NANOELEC JOINS THE NATIONAL COMMUNITY OF RELIABILITY EXPERTS.

Since the end of 2023, Nanoelec has been a member of the French Reliability Center (CFF), a grouping of reliability experts for electronic systems and components. The CFF is a national organization and includes academic and industrial entities, laboratories and research units, large groups and SMEs/mid-caps. CFF's vocation is to bring competent players together to resolve technical and/or technological problems related to reliability, to create synergy between skills, resources and users. François Bouvry, CFF coordinator, sees in this a real advantage for Nanoelec, through the area of the CFF dedicated to the reliability of electronic components and their packaging: *"The Nanoelec/Carac program enhances the scientific potential of the CFF community. At the same time, its PAC-G offering is made even more legible domestically in France."* In return, the program will be able to include new interactions with French experts. *"The CFF areas dealing with the reliability of technologies linked to connectors and assembly and the reliability of mechatronic systems, also enable us to more clearly identify what the end-users need along our value chain"*, says Ennio Capria, Nanoelec/Carac Program Director. ◊

INSTRUMENTATION

A gateway to large-scale instruments dedicated to electronics industry needs

A QUICK AND EASY ACCESS TO SOME OF THE WORLD'S MOST ADVANCED CHARACTERISATION FACILITIES.

PAC-G provides a single point of access to large-scale facilities such as synchrotron and neutron-based sources through a cost-effective and rapid service tailored to innovation in electronics.

PAC-G gives the electronics industry quick and easy access to some of the world's most advanced characterisation facilities. PAC-G also provides an extremely broad portfolio of individual, but complementary characterisation techniques.
"Whether dealing with product quality issues or in order to understand the properties of innovative materials, access to the PAC-G resources in 2023 enabled us to more clearly grasp the benefits of the large instruments for our industrial subjects, whenever more standard equipment shows its limitations", explains Damien Bachellerie, Materials & Dielectrics expert in the Innovation & Technology - Energy Management Business division at Schneider Electrics. *"For example, on the ESRF/ID18 beamline, we demonstrated the pertinence of micro-tomography for a detailed understanding of the structures of materials within future complex components bringing digital into the world of medium voltage."* ◊

Injection of system faults

AT CNRS/LPSC, THE GENESIS ACCELERATOR IS PRODUCING NEUTRONS OF 14 MEV.

A view of the deuterium ions source on the Genesis accelerator14[(14)]. A neutron beam (14 MeV) is generated by nuclear reaction of deuterium nuclei on a tritium target. The Genesis installation is mainly used to test the effects of a single event in the field of microelectronics, on diamond or silicon wafers. Access to this unique instrument is included in the PAC-G service for industrial stakeholders.

Iroc Technologies partners Nanoelec/Carac for components testing services, not only with thermal neutrons at ILL/Tenis, but also with the 14 MeV neutrons at Genesis, in particular for system faults injection protocols. *"In 2023 we were able to test dozens of circuits for the main semiconductor players and more precisely in the medical sector. We also contributed to continuous improvement of the resources at PAC-G"*, explains Issam Nofal, CEO of Iroc Technologies, whose customers are major international foundries and leading semiconductor companies, in Europe as well as in the United States and Asia. "*Access to the PAC-G instruments enables Iroc Technologies to maintain its globally recognized independence in circuit testing"*, says Issam Nofal.

In parallel with the irradiation activities, 2023 was to a large extent devoted to upgrading of the control and command system for the Genesis accelerator.

© F.LEGRAND/CEA

14. At the subatomic physics and cosmology laboratory in Grenoble (CNRS – UGA)

ECOSYSTEM

In Europe, characterisation platforms complement each other

A MARKETING SURVEY CONFIRMS THE COMPLEMENTARY NATURE OF THE CHARACTERISATION PLATFORMS IN EUROPE.

In 2023, the Nanoelec/Carac program, in collaboration with the CEA, carried out a survey to analyze the offerings and services proposed by the large research instruments within the international ecosystem. *"The aim was to evaluate the position of PAC-G, and to contribute to the thought being given to its future development"*, explains Hugo Baylacq, who managed the survey.

"We questioned the industrial relations managers in several European installations[15]: two synchrotrons and one neutron source. We more specifically analyzed how industry can access the instruments, the short and medium-term development prospects, and the means available for specifically performing irradiation testing of electronic components."

Although initiatives similar to PAC-G were identified, none of them is directly comparable; our offering stands out in the diversity of its services, its multi-discipline approach, it single access point and the possibility of creating long-term partnerships.

The survey also identified infra-structures capable of performing irradiation testing of electronic components, complementing the PAC-G offering. ◊

15. DESY, ISIS, PSI

Below,
PAC-G IS A DEDICATED GATEWAY GIVING THE MICRO- AND NANO-ELECTRONICS INDUSTRY QUICK AND EASY ACCESS TO SOME OF THE WORLD'S MOST ADVANCED CHARACTERISATION FACILITIES

ONE OF THE EIGHT POSTERS CREATED IN 2023 BY THE STUDENTS OF THE BRASSART-GRENOBLE SCHOOL FOR TECH&FEST ON THE TOPIC **"LA MICROÉLECTRONIQUE POUR VIVRE DANS UN MONDE MEILLEUR"** (MICROELECTRONICS FOR LIVING IN A BETTER WORLD).
POSTER BY BRUNILDE DUCROCQ, "GRAPHIC DESIGN" STUDENT

Responsible integration of digital devices in SME processes & products

FLORENT BOUVIER

PROGRAM MANAGER AT MINALOGIC AND CO-DIRECTOR OF NANOELEC/ TECHNOLOGY DISSEMINATION PROGRAM, IN CHARGE OF THE EASYTECH INITIATIVE

CHRISTOPHE VAUTEY

MANAGER OF COLLABORATIVE HUBS AT CEA/Y.SPOT AND CO-DIRECTOR OF NANOELEC/DISSEMINATION PROGRAM, IN CHARGE OF THE SYSTEM LAB INITIATIVE

As far as the digital transition is concerned, companies sometimes lack the information and the in-house skills needed to integrate new technologies. However, these technologies are also opportunities to expand their offering and strengthen their commercial position.

With the Technology Dissemination program, the partners in Nanoelec are promoting and accelerating the use of emerging devices and new technologies in a variety of application fields; they are drawing more particularly on R&D skills in imaging, artificial intelligence, embedded software and electronic systems design.

The program comprises two initiatives:

➔ The aim of the System Lab (Addvisia) initiative is to exploit innovative imager components developed by the major industrial partners involved in R&D programs at Nanoelec. New applications and new use cases were explored in 2023, we present here several use cases concerning sport health and environment domains.

➔ In the Easytech initiative, we make advanced electronic blocks and embedded software accessible to SMEs and mid-cap businesses, including those whose core business is anything but digital. The aim is to enable them to take part in the digital transition, to improve the added value of their products or their manufacturing processes. With the first implementation in 2023 of Defi-Ino process at the initiating phase of Easytech projects, we are looking to develop an environmental diagnostic offering for SMEs, mid-caps and start-ups wishing to work with us. Our priority is to help companies cope with the environmental issues of public innovation policies and to provide them with competitive advantages.

PROMOTING THE ADOPTION OF EMERGING TECHNOLOGIES IN NEW APPLICATION FIELDS IS THE MOTIVATION BEHIND THE NANOELEC/ TECHNOLOGY DISSEMINATION PROGRAM

TECHNOLOGY DISSEMINATION PROGRAM AT A GLANCE

→ VISION

Sovereignty in the electronics industry requires efficient dissemination of innovative components and their adoption by national and European integrators and end-users

→ AMBITION

To identify weak signals from the market and to accelerate the time to market of technologies developed by Nanoelec partners with fast prototyping and testing and access to emerging markets

→ MISSION

- To help component and software manufacturers better understand the needs/ possibilities of new applications
- To provide companies, notably SMEs, with information to plan ahead for the arrival of new technologies
- To contribute to the ambition of re-industrializing France and Europe
- To strengthen investor confidence in IRT industrial partners

→ PARTNERS

Captronic/
Jessica France
CEA
GEM
Grenoble-INP
Lynred
Minalogic
Prophesee
STMicroelectronics

Easytech

Easytech is one of the Nanoelec IRT's technological dissemination tools. It focuses on the dissemination of technology blocks and the resulting extension of the product offering, starting primarily from the needs expressed by SMEs dictated by the Market Pull approach. It helps SMEs, the main targets of the program to diversify and improve their existing product or their manufacturing process, by adding intelligence. The targets of the tool are SMEs/mid-caps, in all activity sectors, which have an ambitious project to develop their activity based on innovation in the field of microelectronics. Easytech also includes an environmental impact analysis proposed on the starting phase for all projects in order to support SMEs and startup in the field of sustainability of the products and services. Since 2012, 322 Easytech projects have been carried out, 70% of them with companies based in the Auvergne Rhône Alpes region.

A number of Easytech projects carried out in recent years have resulted in industrialization phases. In 2022 and 2023, four companies were accompanied by Easytech and won the "Première usine France 2030" label (leading plants in France): Limatech, Dracula Technologies, BeFC and CIXI. New funding was raised in 2023, including for BeFC and SiPearl, by companies which had developed a prototype, proof of feasibility or a demonstrator, under Easytech projects.

Florent Bouvier

EASYTECH

Automatic detection of buried networks

GRENOBLE INP-UGA AND MIMO DETECT CHARACTERIZE GENERIC CONFIGURATIONS OF BURIED NETWORKS.

Every year, during technical maintenance work in Europe, nearly 100,000 network damage incidents occur, sometimes leading to potentially fatal accidents. The startup Mimo Detect was created in 2021 and is developing a new tool capable of automatically detecting underground networks, displaying them in real-time on a screen, with 3D visibility. *"An Easytech project with Grenoble INP-UGA, enables us to consolidate our technology"*, explains Jean-David Bigoni, CEO of Mimo Detect. *"Among the necessary developments, the possibility of rapidly identifying whether or not pipes are present in a "standardized" environment is a fundamental result which should allow rapid deployment and reliable positioning results."* Electromagnetic simulations on RF signal/pulse propagation in stratified environments have been performed. They were able to characterize different generic configurations for networks present in the ground. *"We demonstrated a proof of concept (POC) type technical feasibility of an RF system guaranteeing X-ray or scanner type visualization of the buried pipe, with 3D positioning precision"*, explains Jean-David Bigoni. ◊

MIMO DETECT IS DEVELOPING THE FIRST GROUND RADARS DESIGNED TO DETECT BURIED PIPELINES. WITH EASYTECH, THE COMPANY CONSOLIDATES ITS 3D POSITIONING TECHNOLOGY

EASYTECH

Predictive maintenance for industrial microwave ovens

ANTICIPATING MAGNETRON AGEING FOR NEW APPLICATION MARKETS.

As part of the Easytech initiative, G2ELab[1], in collaboration with Captronic, conducted a study for Sairem, a company based in Lyon, to reduce the end-of-life impact of magnetrons used in industrial microwave generators[2]. *"For predictive maintenance we are aiming to be able to anticipate the end-of-life of these high-power components integrated into industrial microwave generators, automatically and sufficiently early"*, explains Olivier Sockeel, who managed the study at Sairem.

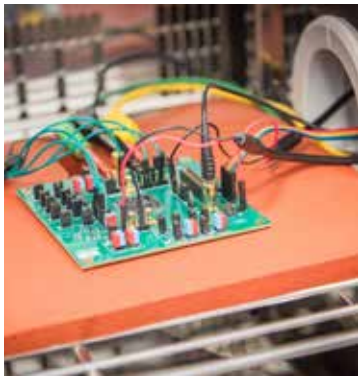
The Sairem company was created in 1978, and specializes in developing industrial microwave and radio frequency generators.

"These methods of heating have been commonly used since the 70s for food products (cooking and tempering of frozen products)", explains Olivier Sockeel, from Sairem. *"More recently, also for new industrial applications such as pasteurization, pest control, drying, additional heating of certain ingredients, but also the production of certain compounds such as hydrogen or synthetic diamonds."* ◊

1. The Grenoble Electrical Engineering Laboratory (G2Elab) covers a spectrum of scientific research from materials and components to the design and control of electrical energy systems (UGA, CNRS, Grenoble INP-UGA).

2. A magnetron is a device which converts the kinetic energy of electrons into electromagnetic energy, in the form of microwaves. It is a vacuum tube without grid in which the electrons emitted by a cathode move towards an anode but are deflected by a magnetic field into a spiral trajectory.

To the right,
MAINTENANCE OF HEAD OF THE SAIREM LATEST GENERATION OF MICROWAVE GENERATORS TO BE OPTIMIZED THROUGH AN EASYTECH PROJECT
© SAIREM



Above,
AN DEDICATED INTEGRATED CIRCUIT AS A TEST VEHICLE READY TO BE TESTED AT CEA TO STUDY BTI (BIAS TEMPERATURE INSTABILITY) AGEING MECHANISMS
© O.DEVISE/CEA 2024

EASYTECH

Designed-in electronic circuit optimization

CEA IS CORRELATING ACTUAL MEASUREMENTS OF ELECTRICAL FAULTS IN ELECTRONIC CIRCUITS WITH ANIAH DIGITAL TWIN.

The importance of embedded electronics has constantly grown with the digitization of all equipment. This digitization is also the result of the increased complexity of the functions made possible by electronics. *"The subject of functional safety is becoming crucial and extremely complex to prove"*, says Vincent Bligny, founder of the Aniah startup which intends to take up this challenge *"thanks to a software which enables 100% of the world's design engineers to detect 100% of the electrical errors in their integrated circuits."*

The Aniah solution enables the reliability of an integrated circuit to be studied, with the aim of modeling its lifetime and identifying the areas of weakness which do not correspond to the circuit's defined mission profile. *"Under Easytech with CEA, we are working on correlating the estimates provided by the solution with reliability test bench measurements, in particular*

→

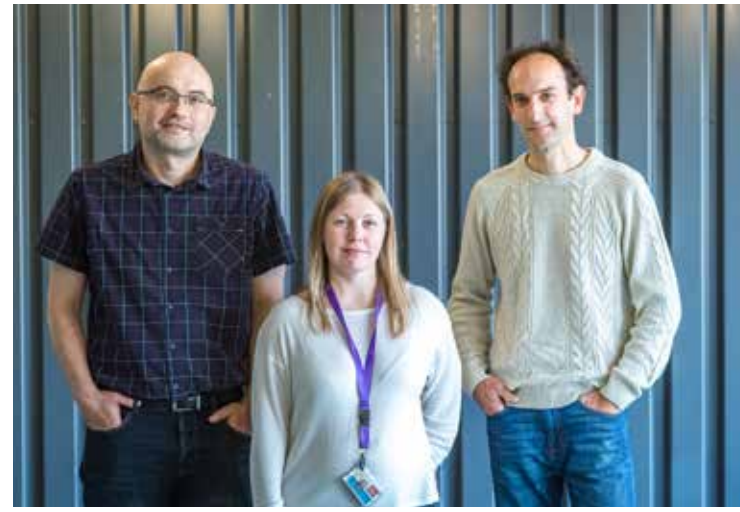
to study BTI (Bias Temperature Instability) ageing mechanisms", adds Vincent Bligny.

"The degradation of a generic electronic component (ring oscillator) included in CEA's standard test vehicle is recorded over several days at 80°C," explains Olivier Guille (CEA-Leti) who carried out the measurements. *"These temperature conditions enable accelerated aging to be applied to the component. We then use the measurements from the experiment to calibrate the estimates of Aniah's EDA[3] tool"*, adds Valentin Gherman, who designed the experimental protocol.

Vincent Bligny adds that *"the project also includes an exploratory side looking at potential applications of our solution to meet current eco-design standards."*

In fact, Chiara Sandionigi (CEA-List) has proposed a new metric that relates the reliability of the component under test to the environmental impact of its manufacture and use. *"We can compare different design choices by assessing their joint impact on the environment and the final reliability of a component during design"*, she explains." ◊

A new metric that relates the reliability of the component under test to the environmental impact of its manufacture and use.



3. EDA stands for Electronic Design Automation.

Top photo,
DEGRADATION OF A GENERIC ELECTRONIC COMPONENT (RING OSCILLATOR) INCLUDED IN CEA'S STANDARD TEST VEHICLE IS RECORDED OVER SEVERAL DAYS AT 80°C

Down photo,
VALENTIN GHERMAN, CHIARA SANDIONIGI & OLIVIER GUILLE (CEA) WERE COMMITED TO WORK WITH ANIAH STARTUP IN THE FRAME OF AN EASYTECH PROJECT

EASYTECH

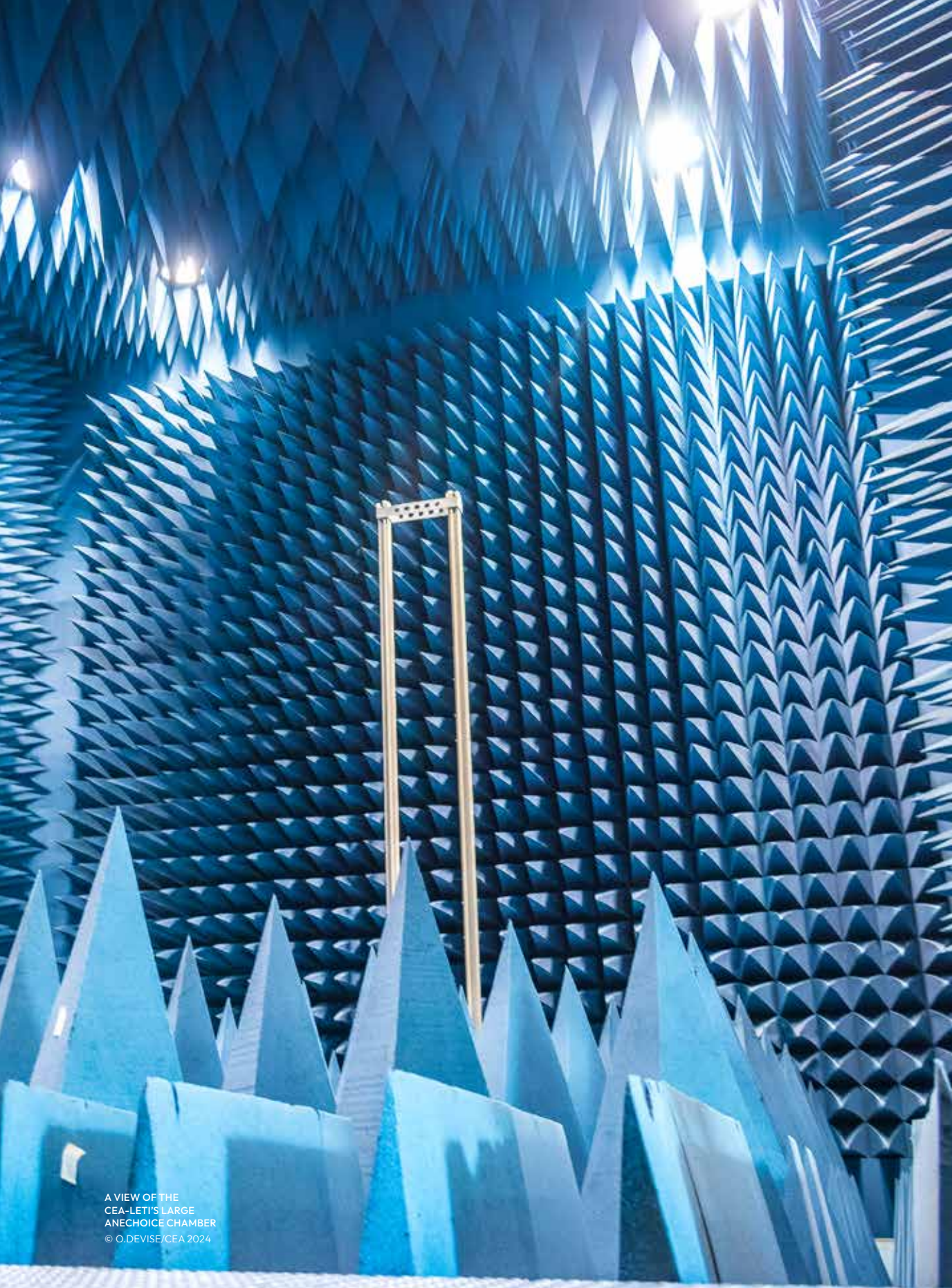
Predictive maintenance of mechanical parts

HEF DURFERRIT AND CEA-LETI ARE DEVELOPING CONNECTED SOLUTIONS TO BRING DOWN THE COST AND MAINTENANCE TIMES FOR ON-SITE MACHINERY.

The HEF Durferrit company has developed steel or composite bushings for site machinery transmission shafts subjected to high loads. *"These bushings are wearing parts at the heart of the transmission, where they reduce friction"*, explains Pierrick Pavallier, Easytech project sponsor at HEF. *"We are seeking to instrument them for real-time wear monitoring. We hope to be able to predict their replacement without having to remove them for diagnosis. Maintenance operations are costly and require that a machine be immobilized for several days."* Prototypes of bushings incorporating a wear sensor that can be remote-monitored have been produced by CEA-Leti. *"They were first of all tested on a dedicated test bench and are currently being installed on a mining excavator"*, says Christophe Delaveaud, Head of the Antenne, Propagation et Couplage Inductif Laboratory at CEA-Leti, where the study was carried out. ◊

Top photo,
CEA-LETI ENGINEER MARWAN JADIDI PREPARES TO DRAW UP THE 3D RADIATION DIAGRAM OF THE RING IN PLACE IN A REALISTIC METAL MODEL OF AN EXCAVATOR CONNECTING ROD, IN CEA-LETI'S LARGE ANECHOIC CHAMBER
© O.DEVISE/CEA 2024

Down photo,
PROTOTYPE OF THE RING DEVICE DEVELOPPED AT CEA-LETI FOR HEF DURFERRIT TO MONITOR MECHANICLA RODS IN HEAVY MACHINES
© O.DEVISE/CEA 2024



A VIEW OF THE CEA-LETI'S LARGE ANECHOICE CHAMBER
© O.DEVISE/CEA 2024

4. This technological feat is achieved using an innovative infrared sensor coupled with artificial intelligence functions.

Below,
TINY AND SELF-POWERED DEVICE FOR MASSIVE ENERGY-SAVING IN BUILDING SECTOR
© ORIOMA

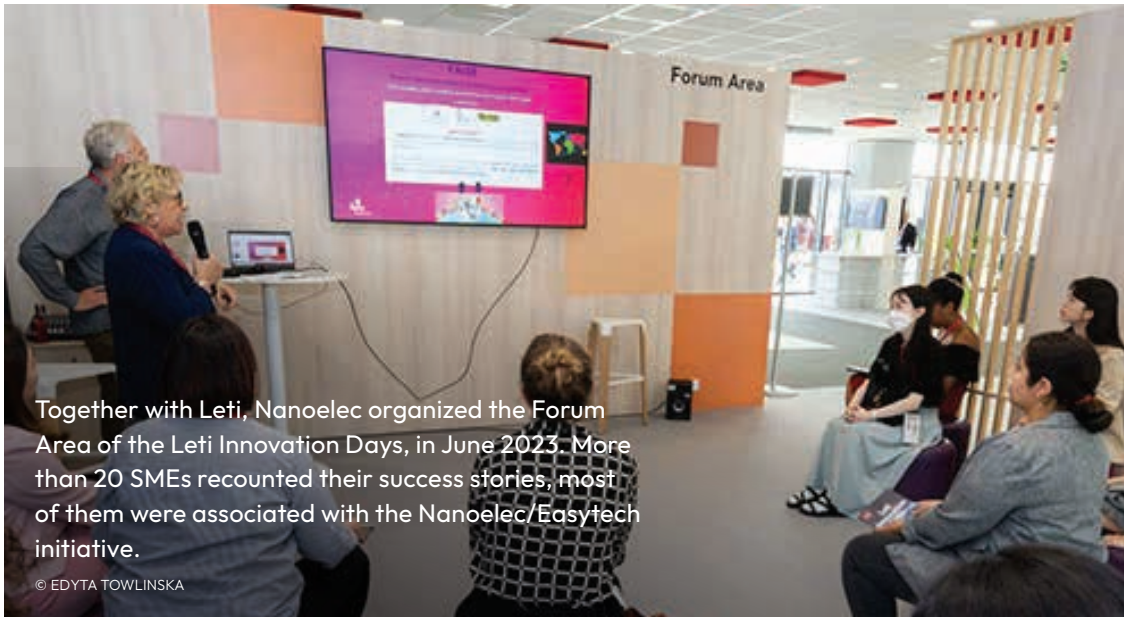
EASYTECH

A frugal thermal detector to warn of abnormal heating in industrial processes

ORIOMA AND CEA-LETI TO DEVELOP AN ABNORMAL HEATING DETECTION ALGORITHM.

"At Orioma, we are developing a compact camera needing no outside power, explains Serdar Manakli, one of the company's co-founders. Orioma, a start-up co-founded and accompanied by the SATT Linksium, received an award at the i-Lab 2022 competition. Orioma's technologies come from CEA-Leti and the TIMA laboratory (CNRS/UGA/Grenoble INP). *"Our camera can operate for 15 years with no battery, cable, or maintenance."* [4]
Started in 2022, a Easytech project associating Orioma and CEA-Leti aims to develop an abnormal heating detection algorithm *"for example to monitor the correct working of an industrial process and sound the alert if necessary"*, Serdar Manakli says. In 2023, the implementation of the algorithm was trialed on various types of off-the-shelf microcontrollers. The ultimate goal is to be able to run compact thermographic analysis efficiently with the Orioma disruptive camera, while retaining the advantages and energy frugality of the system. *"Our goal is to be the global reference for energy-independent connected objects within the next 5 years"*, Serdar Manakli concludes. ◊

To monitor the correct working of an industrial process and sound the alert if necessary.



Together with Leti, Nanoelec organized the Forum Area of the Leti Innovation Days, in June 2023. More than 20 SMEs recounted their success stories, most of them were associated with the Nanoelec/Easytech initiative.
© EDYTA TOWLINSKA

System Lab/Addvisia

The Addvisia technology platform initiative, creates a community of interest around the topic of multimodal and multispectral imaging from STMicroelectronics, Lynred and Prophesee, in order to explore the full potential of combined imagers and identify new applications. This modular platform brings together technology suppliers, integrators and users around common objectives: indentifying new disruptives use cases and better understanding why and how imagers can be combined for new uses, in an agile experimentation environment. In 2023, the platform was implemented for numerous use cases, including snowpack analysis, observation of soil core sampling for environmental analysis, trajectory analysis and physiological effort monitoring.

Above,
MULTIMODAL DISPLAY OF A DRONE IN FLIGHT USING THE ADDVISIA PLATFORM. NOTE THE WEALTH OF INFORMATION OBTAINED ON HOT SPOTS, AREAS IN MOVEMENT, TOTAL DIMENSIONS.

In 2023, a major overhaul of the Addvisia technical platform was made to take account of feedback from the partners, along with acquired experience, and to anticipate new use cases. The mechanics of the support and the alignment of the sensors with their optical equipment were completely redesigned to facilitate the integration of new sensors, improve the mechanical and optical robustness of the assembly and drastically reduce its weight. The platform is endowed with new mechanical functions to allow the addition of extra functions in front of the cameras. We have also integrated new sensors, along with the software upgrades needed for the platform to work correctly, in particular with regard to the problem of time synchronization of the various images of a given scene.

Christophe Vautey

The Addivisa compact multispectral camera is easy to setup in any situation.

SYSTEM LAB

Displaying strata in the snowpack

TO BETTER UNDERSTAND BREAK'S PROPAGATION AT THE ORIGIN OF AN AVALANCHE AND RELATED PHYSICAL PRINCIPLES.

Propagation Saw Tests (PST) assess snowpack stability and avalanche risk. Using SWIR imaging and event-based sensors, researchers capture detailed, non-visible spectrum imagery and high-speed dynamic changes. This innovative approach reveals hidden snowpack features and improves understanding of weak layers and rupture propagation, enhancing knowledge about physical principles and how those weak layers work.

Different tests were perform with Data Avalanche[5] and University Savoie Mont-Blanc in the field with an autonomous version of the Addvisia platform. ◊

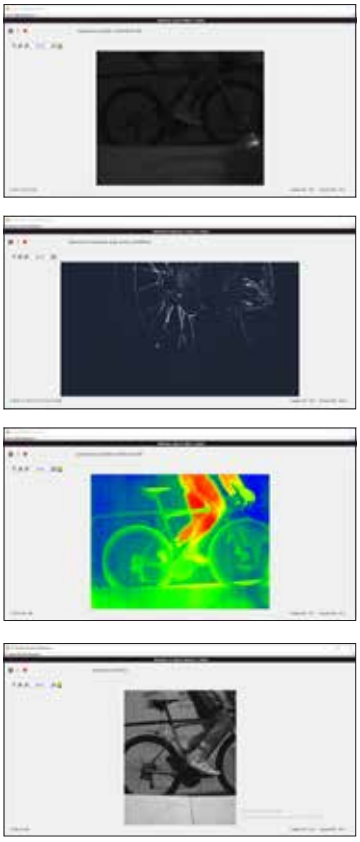
5. Association for the improvement and sharing of knowledge about avalanches

Below,
INSTALLATION OF THE ADDVISIA PLATFORM ON A CROSS-SECTION OF THE SNOWPACK
© DR

SYSTEM LAB

Revealing thermoregulation by vascularization of the skin

ADDVISIA COULD BE USED TO CUSTOMIZE WARM-UPS FOR HIGH-LEVEL ATHLETES.



The industrial partners of System Lab (STMicroelectronics, Lynred and Prophesee) were looking to experiment with Addvisia, to evaluate its ability to capture mechanical (friction, data), thermal and physiological phenomena through imaging. With the +2Sports association, which specializes in the preparation of high-level cyclists, the System Lab operational team at CEA used the Addvisia platform to film a cyclist training on a treadmill. *"It was possible to easily and dynamically retrieve the mechanical and thermal behavior of the bike's components during the session: thermal signature of the brakes, analysis of the transmission and friction of the tires"*, explains Nicolas Puget, engineer at CEA Y.Spot. *"During the session, we revealed a physiological phenomenon: contrast zones gradually appeared on the parts of the athlete's body during thermal imaging during training, revealing muscular warm-up and the athlete's blood flow network. These changes in surface contrast are caused by the appearance of thermoregulation by vascularization of the skin."* These observations could have potential for quantification and customization of high-level athlete warm-ups, as well as for other sports or medical applications. ◊

Above,
EVENT-BASED AND LWIR IMAGES OBTAINED DURING THE FIRST TRAINING SESSION
© DR

To the right,
INSTALLATION OF THE PLATFORM DURING THE FIRST TRAINING SESSION
© DR

When the ball moves at close to 200 km/h, conventional imaging is not fast enough to track its movement in relation to the lines on the court.

On the left,
RECONSTITUTION OF TENNIS BALL TRAJECTORIES AFTER SERVING – BALL IN AND BALL OUT
© S.MARTIN/CEA

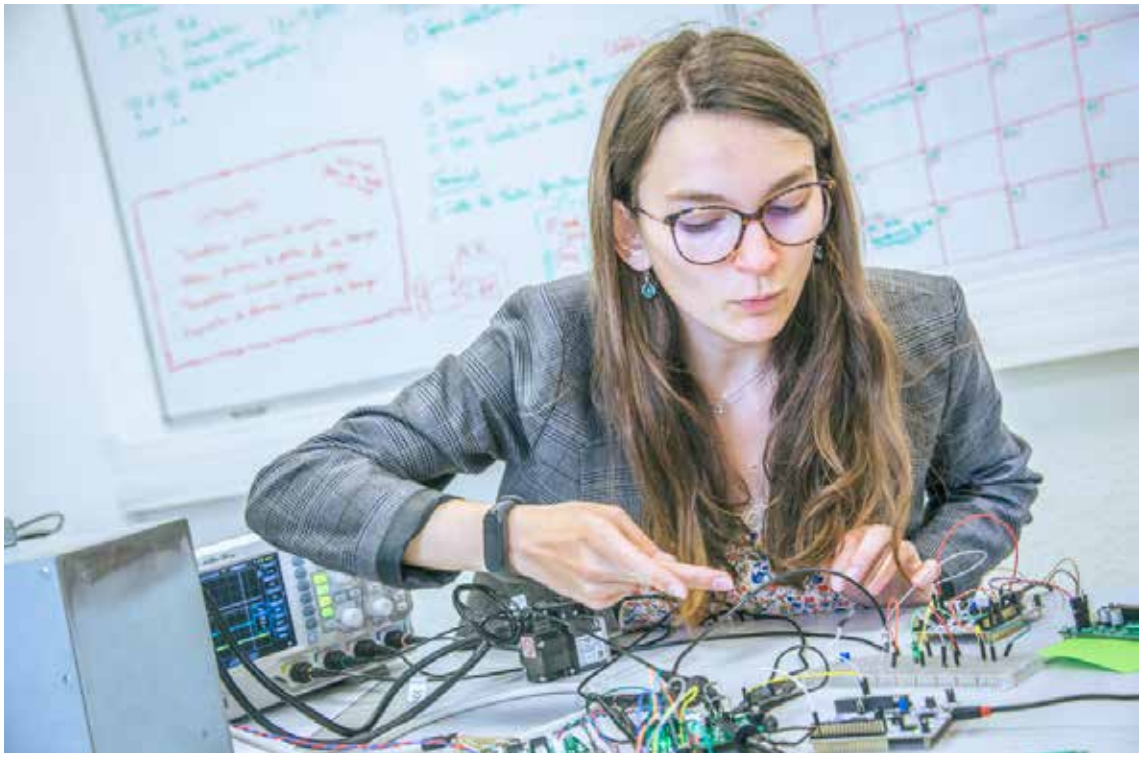
On the right,
INSTALLATION OF THE ADDVISIA PLATFORM ON A TENNIS COURT
© S.MARTIN/CEA

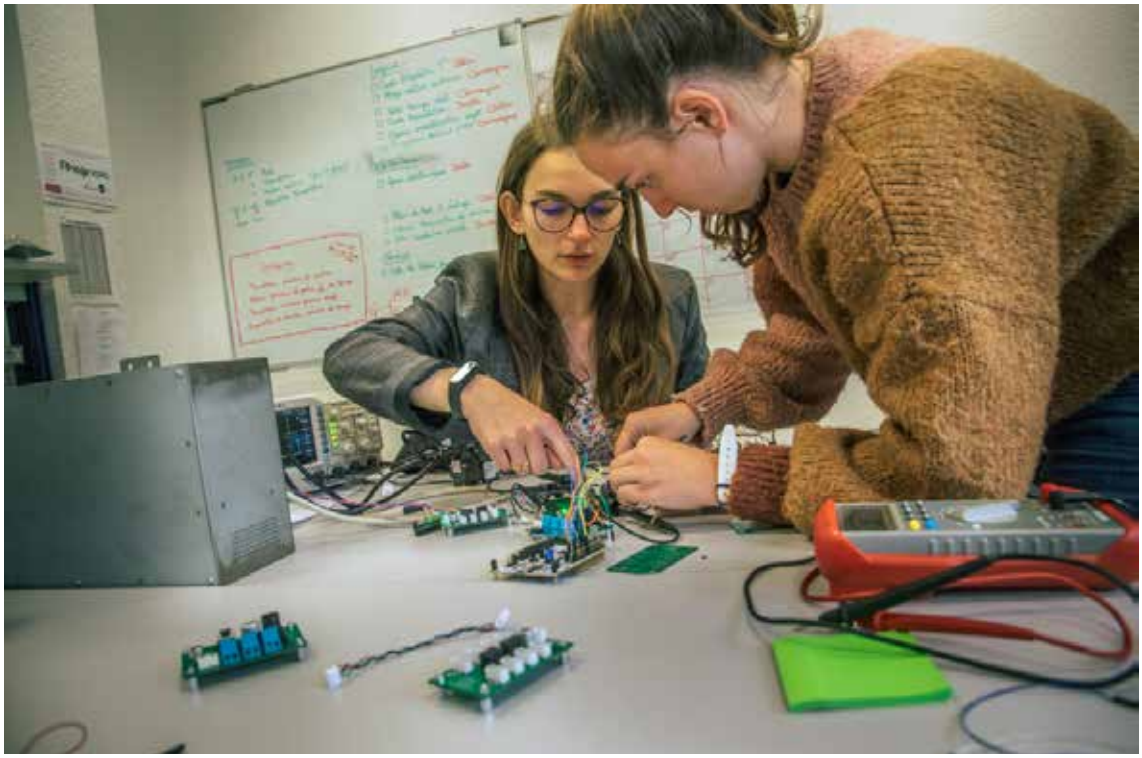
SYSTEM LAB

Umpiring & movement analysis in tennis

COMBINING EVENT-BASED & VISIBLE CAN TRACK BALLS AT 200 KM/H.

To demonstrate the benefits and feasibility of image merging, the Addvisia visible and event-based imagers were used on a tennis court during practice sessions by ranked young players, capable of producing ball speeds representative of high-level sport. *"When the ball moves at close to 200 km/h, conventional imaging is not fast enough to track its movement in relation to the lines on the court"*, explains Sébastien Martin, CEA-Leti engineer for System Lab. *"The images collected were processed to reconstruct the ball's trajectory. It is then possible to design an automatic umpiring system using sensors."* The experiment also demonstrated the benefits of event-based imaging, with the aim of providing a detailed analysis of a champion's high-speed movements, which would help improve their performance and posture. ◊





ENGINEER STUDENTS AT GRENOBLE IPN-UGA/ESISAR, FOR EASYTECH INITIATIVE

ONE OF THE EIGHT POSTERS CREATED AT THE END OF 2023 BY THE STUDENTS OF THE BRASSART-GRENOBLE SCHOOL FOR THE TECH&FEST FESTIVAL ON THE TOPIC **"LA MICROÉLECTRONIQUE POUR VIVRE DANS UN MONDE MEILLEUR"** (MICROELECTRONICS FOR LIVING IN A BETTER WORLD).

POSTER BY HERICK RIBEIRO DO NASCIMENTO, "GRAPHIC DESIGN" STUDENT

Human Capital & Training Design

Sustainable development as a driver of innovation

SYLVIE BLANCO

SENIOR PROFESSOR OF TECHNOLOGY AND INNOVATION MANAGEMENT AT GRENOBLE ECOLE DE MANAGEMENT (GRENOBLE GRADUATE SCHOOL OF BUSINESS), CO-DIRECTOR OF THE NANOELEC/HUMAN CAPITAL & TRAINING DESIGN PROGRAM

PANAGIOTA MORFOULI

PROFESSOR AT GRENOBLE INP-UGA, CO-DIRECTOR OF THE NANOELEC/HUMAN CAPITAL & TRAINING DESIGN PROGRAM

The general objective of the Human Capital and Training Engineering program is to respond in an agile and proactive way to the skills needs of the partners, in direct relation with the R&D and technology diffusion activities of the consortium, in particular the industrial companies. To this end, the Elise-LMS (Learning management system - Experiential Learning of Innovation for Sustainable Ecosystems) has been designed and prototyped between 2021 and 2023. The training content created covers skills from technology to market, on the core themes of Nanoelec's. Elise is based on experience-based teaching and co-development of pedagogical materials implemented on an LMS-type platform, involving academic institutions and industry, engineers and managers, initial and continuing training. This system responds to the skills needs of the Nanoelec ecosystem, which is characterized by its high technological intensity, the wide scope of its applications and by its commitment to a sustainable impact.

The program is based on three complementary building blocks:

➔ A common core of Nanoelec fundamental skills integrated into capsules,

➔ Experience-based sessions using immersive lab-like spaces and demonstrators for hybrid collaborative teams involved in the Institute's work,

➔ The creation of learning communities engaged in missions for the sustainable impact of electronics applications.

In 2023, the "Sustainable Electronics" cycle of the program focused on the Digital Product Passport; it included capsules, a student challenge and a professional seminar.

ENGINEER STUDENT AT GRENOBLE INP-UGA DISCUSSING THE TRENDS ON SUSTAINABILITY FOR THE FUTURE OF DIGITALAZATION
© P.JAYET

CHIF PROGRAM AT A GLANCE

→ VISION

The competitiveness of the electronics industry is linked to the development of interdisciplinary and agile collaborative capabilities

→ AMBITION

Design and experiment with an integrated and customized learning and training system that strengthens the human capital, and the dynamic innovation capabilities of the Institute and its academic and industrial partners

→ MISSION

Design and develop new training module contents and formats in three areas: fundamental skills, experiential learning, and learning communities to address emerging challenges

→ PARTNERS

Grenoble INP-UGA
Grenoble Ecole de Management (GEM)
STMicroelectronics
Schneider Electric

FUTURE GENERATIONS

Electronics industry attractiveness

GRENOBLE INP-UGA QUESTIONED NEARLY 450 EUROPEAN STUDENTS ABOUT THEIR PERCEPTIONS OF THE ATTRACTIVENESS OF THE MICROELECTRONICS SECTOR.

In recent years, both industry and schools have noticed a growing lack of interest in the electronics and microelectronics sector and its training courses.

"In order to understand this phenomenon and if possible, to make these professions more attractive, we conducted a survey in early 2023 among future engineers in France and internationally", explains Panagiota Morfouli, professor at Grenoble INP-UGA and co-director of the Chif program, who has designed the survey[1] in collaboration with Estelle Belin-Di Stephano, Nanoelec educational engineer at Grenoble INP-UGA.

The results of this survey were one of the main contributions to the discussions and reflections during two workshops and the territorial forum on the attractiveness of the electronics industry, organized by Nanoelec and Minalogic in May 2023.

The main points are:

➔ Among the reasons that convinced them to join the electronics or microelectronics sector, they mentioned a "revolutionary" sector, with a wide variety of jobs and applications, good remuneration and a strong societal impact. However, they would like companies to pay more attention to sustainability.

➔ In terms of what puts them off, they mentioned the "difficulty" of these technologies, the "difficult" and "time-consuming" missions, the distance from the end product, and the ethical and environmental issues.

➔ When looking for their future job, the students who participated in this survey will focus on the size of the company (start-up and large group), their experience within the company, the role entrusted to them, the company's values and the sector of activity. ◊

1. 437 students replied to survey, including 348 from France and 89 from abroad, most of them being students at Grenoble INP-UGA/ Phelma

Photo,
IN MAY 2023, AT THE TERRITORIAL FORUM ORGANIZED BY NANOELEC AND MINALOGIC, LORENA ANGHEL, PROFESSOR AT GRENOBLE INP-UGA, GAVE A DETAILED PRESENTATION OF THE SURVEY OF 437 EUROPEAN STUDENTS ON THE ATTRACTIVENESS OF THE ELECTRONICS SECTOR
© P.JAYET/CEA

From the basic principles of the LCA to the actual ecodesign of electronic products, from the point of view of environmental impact, which can take into account manufacturing, use and end-of-life.

Above,
VIDEO SEQUENCE ON LIFE CYCLE ASSESSMENT IN THE CAPSULE "RATIONAL ECO-DESIGN OF MICROELECTRONIC PRODUCTS"

BASIC KNOWLEDGE CAPSULE

Rational eco-design of electronics

A CAPSULE FOR ELECTRONICS PROFESSIONALS.

The ISO 14040 standard specifies the principles and framework for conducting Life Cycle Assessments (LCA) of a product. In a new self-learning capsule, the Chif program presents the basic aspects of the methodology and summarizes the good practices to be adopted when designing more sustainable devices, equipment and systems.

"The objective is to be able to apply the basic concepts of the LCA methodology in a critical and operational way in order to assess the environmental impact of an electronic product", explains Ernesto Quisbert-Trujillo, researcher at G-Scop (Grenoble INP-UGA), who is in charge of selecting the contents of this capsule. *"In the first sequence, the student is introduced to the concept of the life cycle and the basic principles of the LCA, from initial inventory to impact assessment. The second part of the capsule deals with the actual eco-design of electronic products, from the point of view of environmental impact, which can take into account manufacturing, use and end-of-life."*

The key concepts are explained and illustrated with three key components: a formal definition, a picture and an examination in the context of electronics. Self-assessments at the end of each section allow the student to check what they have learned. ◊

Each year, we create new teaching scenarios that bring together learning communities involved in missions for the sustainable impact of electronics applications.

SYLVIE BLANCO

GROUP OF STUDENTS WORKING ON THE ATTRACTIVENESS OF THE MICROELECTRONICS SECTOR IN GRENOBLE INP-UGA/PHELMA
© P. JAYET/CEA

To prepare students in Grenoble to learn about sustainable electronics and to develop a critical and responsible commitment, we proposed this year that they work on the development of the *Digital Product Passport*.

PANAGIOTA MORFOULI

BASIC KNOWLEDGE CAPSULE

Eco-design for Power Electronics

REDUCE THE PRODUCT'S ENVIRONMENTAL FOOTPRINT AND PROMOTE CIRCULARITY.

An all-new teaching capsule introduces student to tools and strategies for eco-designing power electronics (PE). It covers the basics of implementing a PE design process, before adding an eco-design section, including an introduction to Life Cycle Assesment as it applies specifically to the industry.

"With this capsule, the student will be able to select approaches to integrate into a power electronics design stream, not only to reduce the environmental footprint of the product during its manufacture and use, but also to promote circularity", says Jean-Christophe Crébier, CNRS researcher at G2ELab[2] who oversaw the capsule's design and content with Luis-Martin Lobejon, research engineer at Grenoble INP-UGA/Ense3. ◊

2. Electrical engineering laboratory in Grenoble (G2Elab)

MODULAR POWER ELECTRONICS CONVERTER PROMOTING CIRCULARITY
© G2ELAB CNRS/ UGA/G-INP

EXPERIENTIAL LEARNING COURSE

Building digital trust

WITH THE SUPPORT OF NANOELEC, ESISAR RENEWS ITS "SECURE AND COMMUNICATING EMBEDDED SYSTEMS" (SES) COURSES.

"Following a training development meeting attended by industrial companies linked to the electronics sector, we decided to develop our courses with SES learning, in order to better meet the needs of industry and young people", explains Romain Siragusa, project sponsor at Esisar/ Grenoble INP – UGA, specializing in cybersecurity of smart systems. *"The adoption of a new teaching template requires a profound transformation of the teaching of electronics, aiming at a more coherent teaching of the cybersecurity of embedded systems and artificial intelligence."* Since the start of the 2023 school year, the new template has been applied to the third year course, and work is continuing to apply it to the fourth and fifth years.
A number of teaching demonstrators have been created around the cybersecurity of connected objects, as well as two entirely new courses: "Managing Attacks and Countermeasures" and "Preventing Risks and Anticipating Regulatory Requirements (standards)". *"We are now ready to meet the industry's needs for secure and communicating embedded systems, both in terms of hardware and software security, for communicating applications with the security of wireless networks, the vulnerability of web applications, etc.,"* explains Romain Siragusa. ◊

EXPERIENTIAL LEARNING COURSE

Innovative business models

THE CHALLENGES OF BUSINESS MODEL INNOVATION WERE THE SUBJECT OF A CAPSULE AND A COURSE DEVELOPED BY GEM IN 2023.

Transformation required by the sustainable development goals, is facilitated by the digitization of products, services and processes.

The Kibis capsule and workshop addressed the challenges of business model innovation and the resulting organizational transformation. This transformation, which is required by the sustainable development goals, is facilitated by the digitization of products, services and processes.

"Defined as the process of integrating a new business logic into an established company in order to improve profitability or take advantage of new business opportunities[3], business model innovation is complex and involves making decisions in a situation of high uncertainty", explains Sylvie Blanco who designed the entire Kibis teaching package within Nanoelec. For more than a decade, however, innovation in business models has been recognized as necessary for the success of companies in the face of digital and sustainable transformations, or even disruptions of their markets and their industries[4].

Two versions of the Kibis workshop are conducted in the first semester of 2023: in the intrapreneurial mode with Master's 2 students of the GEM grande école program working on real projects of market leaders; in the executive sponsor mode with an Executive MBA group, in collaboration with two companies (ARaymond and HP). *"These pilot training programs have provided valuable lessons on how to learn about and teach business model innovation, especially with this Kibis tool which is able to address the issue of actual implementation, going beyond the simple modeling of new business models"*, emphasizes Michele Coletti, Associate Professor at Grenoble Ecole de Management. A Kibis teaching capsule has also been developed on a specific use case: it concerns dynamic pricing (connected labels + smart cameras: IoT, AI, RFID) to help reduce food waste in supermarket-type retail outlets.

Agility is a key competence for Wise NRJ, a consulting firm for smart buildings and collective self-consumption[5]. *"The experience of working with GEM through the Kibis method, developed under Nanoelec, is for us a means of combining field expertise, and a business reality, with external perspectives from different geographical, generational and professional backgrounds"*, explains Eric Jouseau, CEO of Wise NRJ.

The preparatory work allowed the company's management teams to "take a step back" from their day-to-day commitments, by trying to formalize their approach in terms of a business model and to simply reformulate their offering. *"We were then able to see how our company's project, its purpose, its objectives and its methods, were perceived by students from a very different geographical backgrounds"*, says Eric Jouseau. *"The students' work brought out some very interesting ideas about the possible means of growth available to us: from our market re-segmentation, to different possible capital strategies, to reformulating the offer from the customer point of view such as providing them with total financing[6]."* ◊

3. Trapp M. Voigt K.I. Brem A. (2018), Business models for corporate innovation management: introduction of a business model innovation tool for established firms, International Journal of Innovation Management, 22(1), 24 pages. DOI: 10.1142/S136391961850007X

4. Teece D.J. (2010). Business models, business strategy and innovation, Long Range Planning, 43(2-3), 172-194

5. Wise NRJ provides consultancy and engineering linked to the energy, environmental and digital transition of buildings and regions

6. Reduce the initial input from the customer and finance the overall project directly with the savings and income generated

LEARNING COMMUNITY FOR RESPONSIBLE MICROELECTRONICS

Anticipate the introduction of digital product passport

IN FEBRUARY 2023, 52 STUDENTS FROM GRENOBLE INP-UGA AND GRENOBLE-ECOLE DE MANAGEMENT, TOGETHER WITH EXPERTS, PARTICIPATED IN A WORKSHOP ON DIGITAL PRODUCT PASSPORTS AS PART OF THE EU'S SUSTAINABLE PRODUCTS INITIATIVE. ESTELLE BELIN-DI STEPHANO, EDUCATIONAL ENGINEER AT GRENOBLE INP-UGA/PHELMA FOR THE HUMAN CAPITAL & TRAINING DESIGN PROGRAM AT NANOELEC, GAVE AN OVERVIEW.

ESTELLE BELIN-DI STEPHANO

EDUCATIONAL ENGINEER AT GRENOBLE INP-UGA/PHELMA, IS PART OF THE HUMAN CAPITAL & TRAINING DESIGN PROGRAM AT NANOELEC

WHAT IS A DIGITAL PRODUCT PASSPORT?

E.B. In March 2022, the European Commission introduced a proposal that aims to make almost all physical goods more sustainable and energy efficient throughout their lifecycle. One of the goals of the Ecodesign for a Sustainable Economy initiative is to create a digital passport for every product[7].

HOW WILL IT WORK?

E.B. The passport will provide information on the environmental impact of the products according to sustainable development criteria. It aims to make it easier to repair, recycle, reuse and resell a product, and to increase transparency about the environmental and societal impact of the product throughout its life cycle.

WHICH PRODUCTS DOES IT COVER?

E.B. It is a priority for the following industries: electronics and electric vehicle batteries. The goal is to have access to increasingly sustainable and recyclable products in order to reduce their carbon footprint, and to increase consumer awareness of their choices.

HOW DID YOU GET STUDENTS AND INDUSTRY EXPERTS TO WORK TOGETHER?

E.B. The two half-day workshops took place on February 10 and 24, 2023. The sessions were organized in collaboration with experts from STMicroelectronics, CEA-List, Akileo, and students from Grenoble INP UGA, GEM. As part of a Nanoelec program, the students worked on the digital passport for a Nucléo circuit board. This small electronic board contains a processor and a memory to program and control, for example, actuators using event-sensing sensors.

WHAT METHOD DID THEY USE?

E.B. The students were divided into small groups, and were assisted by business professionals. They had to design the digital passport of a Nucléo circuit board, a secondary board and its sensors (i.e., for humidity, temperature, optics, etc.), and the communication modules (i.e., Bluetooth, 4G, Wi-Fi, etc.). The product was customized for one of the following five applications: voice recognition, mini weather station, bicycle radar, programmable lighting, and water quality control. ◊

7. Funded by the European Commission as part of the Digital Europe Program, CIRPASS is a collaborative initiative that prepares the ground for the gradual oversight and deployment of a standardsbased Digital Product Passport (DPP) in accordance with the requirements of the Proposal for Eco-design for Sustainable Product Regulations (ESPR), and with an initial focus on electronics, batteries, and textile sectors.

Above,
52 STUDENTS FROM GRENOBLE INP-UGA AND GRENOBLE-ECOLE DE MANAGEMENT, PROFESSORS AND EXPERTS, SPENT TWO DAYS WORKING ON THE CONCEPT OF THE DIGITAL PRODUCT PASSPORT.
© GRENOBLE INP-UGA

On the right,
CO-CREATION OF VALUE FOR AN E-PASSPORT, A EUROPEAN COMMISSION PROJECT; STUDENTS AND INDUSTRY FROM THE GRENOBLE ECOSYSTEM WORK TOGETHER ON A NUCLÉO CIRCUIT BOARD FOR STMICROELECTRONICS.
© LUDIVINE SANGIORGIO/ GRENOBLE INP-UGA

LEARNING COMMUNITY FOR RESPONSIBLE MICROELECTRONICS

A new sustainable electronics magazine

ABOUT A HUNDRED STUDENTS FROM GRENOBLE-ECOLE DE MANAGEMENT (GEM) HAVE PARTICIPATED IN DEVELOPING A CONCEPT FOR A MAGAZINE DEDICATED TO SUSTAINABLE MICROELECTRONICS. ISABELLE SAURET, COORDINATOR OF THE PROJECT AT GEM, EXPLAINS.

ISABELLE SAURET

PROJECT MANAGER AT GEM AND FOR NANOELEC

© DR

SIXTEEN "COVER PAGE" PROPOSALS AND PRESS RELEASES WERE PRODUCED AS PART OF Y. PICTURING TO ACCOMPANY THE LAUNCH OF ISSUE N°1 OF A BRAND NEW MAGAZINE ON SUSTAINABLE ELECTRONICS. HOW DID THE PROJECT EVOLVE?

I.S. Y.Picturing was launched as a challenge for the new school year challenge at GEM (Grenoble Ecole de Management), inviting more than six hundreds students to participate. Their task was to create a concept for a new magazine dedicated to sustainable microelectronics. They had to design the cover page of the magazine and write the press release for the launch of the new publication.

WHICH STUDENT PROFILES DID YOU TARGET?

I.S. Bachelor students were put to work. Each group of participants consisted of forty students. They worked in 'hackathon' mode for five days. Their enthusiasm far exceeded our expectations and this experiment illustrates the importance of giving students the opportunity to think creatively and raise their awareness of technological issues, in order to increase their capacity to meet the challenges of societal transitions.

WHAT AVENUES OF REFLECTION ARE OPENED UP BY THIS WORK?

I.S. The students have shown us that pictorial expression as a means of reflection. It opens up avenues of research that we had not previously considered. For example, they indirectly suggest working on the emotional impact of communicating about sustainable electronics, both to young people who might choose careers in the sector and to the general public. For these audiences, the idea is to better measure their reactions, their attitudes and their behaviors toward a technology that is becoming both more ubiquitous and more pervasive.

WHAT WAS THE MAIN MOTIVATION BEHIND THE PROJECT?

I.S. We wanted to stimulate reflection and create a community around the theme of sustainable microelectronics. The project takes its name from the "Grenoble Y", which refers to the Y-shaped area formed by the developed valleys of the Isère River, including the Voreppe Gap and the Grésivaudan Valley, and the Drac River, with the city of Grenoble in the middle.

THE SPECIFIC TOPIC FOR THIS VERY FIRST IMAGINARY ISSUE OF THE Y.PICTURING MAGAZINE WAS THE DIGITAL PRODUCT PASSPORT. WHAT DID THE STUDENTS DO WITH IT?

I.S. Participants were asked to come up with a teaser that would attract the attention of journalists, while thinking about what kind of articles could fill the pages of the magazine. A total of sixteen projects were submitted. Project evaluators noted that the students expressed a need for more in-depth training on the complex aspects of the technology.

WHO IS THE TARGET AUDIENCE OF THE Y. PICTURING MAGAZINE?

I.S. The imaginary magazine Y. Picturing is aimed at the general public, first of all at those who are interested in technology. The goal is to engage people from all walks of life in thinking about sustainable microelectronics and to raise their awareness of the issues and challenges involved. ◊

Above,
GROUP 1: "THE DIGITAL PASSPORT FOR ELECTRONIC PRODUCTS, A SOLUTION FOR MORE RECYCLING? " FROM LEFT TO RIGHT: MANON GUEGUEN, MARGOT JEDRESKI, MAXIME GUITARD, JESSICA DIAS; THE TEAM ALSO INCLUDES GEFFREY SAUTRON, SOLÈNE FOURCHES & JADE LUBERDA
© GRENOBLE INP-UGA

On the right,
GROUP 2: "HE'S BEEN CHEATING ON ME SINCE CONCEPTION." FANTINE BODIER, HUGO HOURY & CLÉMENT JANOT
© LUDIVINE SANGIORGIO/ GRENOBLE INP-UGA

To complete the “Sustainable Electronics” cycle of the Digital Product Passport (DPP), GEM and Grenoble INP-UGA organized a master class between professionals (CEA, GEM, Grenoble INP-UGA, Lynred, Pyxalis, Schneider Electric, STMicroelectronics) in January 2024. *“We adopted a collective process to prepare an influential communication aimed at decision-makers to encourage the commitment of resources to promote the DPP and, more generally, a more sustainable and more responsible approach to microelectronics”*, explains Sylvie Blanco, professor at GEM and co-director of Nanoelec/Chif, who designed the teaching engineering for the session.

© ISABELLE SAURET/GEM


Questions sur l'apport technique 1

LEARNING COMMUNITY FOR RESPONSIBLE MICROELECTRONICS

Interactive displays and the rebound effect

MORE THAN SEVENTY STUDENTS FROM GRENOBLE INP - UGA AND GRENOBLE ÉCOLE DE MANAGEMENT WORKED ON THE TOPIC OF INTERACTIVE SCREENS AND THE REBOUND EFFECT LINKED TO THE DIFFUSION OF TECHNOLOGIES.

On February 6 and 7, the annual edition of the Chif program's "Sustainable Electronics" workshop brought together experts from CEA, STMicroelectronics, Aledia, Pyxalis and the G-Scop laboratory (Grenoble INP-UGA), as well as students from Grenoble INP-UGA/Phelma and Grenoble École de Management.

"This year, the students worked on the topic of interactive displays and the rebound effect", explains Sylvain Engels, Professor at Grenoble INP - UGA and Digital Team Manager at STMicroelectronics, about the student's work.

"For this workshop, the focus was on large displays such as interactive whiteboards, information kiosks or control terminals", says Laura Mazzarella, Nanoelec/Chif pedagogical engineer at Grenoble INP-UGA/Phelma who designed the workshop with Estelle Belin di Stephano, also a pedagogical engineer. *"Interactive displays are now everywhere: smartphones, tablets and so on. The students had to think about the environmental and societal impact of these devices as well as the rebound effect that may be associated with their proliferation and increased use."*

The rebound effect is a phenomenon that occurs when the expected energy savings from using a more energy-efficient resource or technology are not realized, because they lead to overconsumption.

"Improving energy efficiency does not necessarily lead to energy savings: in fact, energy consumption has exploded in recent decades, despite significant progress in energy efficiency", said Bruno Gayral, a CEA researcher who briefed the students at the beginning of the workshop.

PROFESSIONALS AND STUDENTS JOIN FORCES TO MEET THE CHALLENGE OF SUSTAINABLE ELECTRONICS CHALLENGE DURING THE INTERACTIVE SCREENS AND REBOUND EFFECT WORKSHOP ORGANIZED BY CHIF IN FEBRUARY 2024

"For example, the development of more efficient and sustainable LEDs is leading to new uses of this light such as hydroponics and indoor agriculture, luminous architectural designs, multiplying the number of screens, etc."

The students were divided into 13 groups of 5 to 6 people. Each group had to work on a specific area of application: education, entertainment, business.

After summarizing the bibliographical resources presenting the advantages and disadvantages of the use of interactive displays, they proposed and presented solutions capable of reducing the environmental and social impact of these displays, taking into account of the rebound effect. *"The enthusiasm of the students and their proposals, which seem to have merit, are two aspects that really stayed with me"*, says Sylvain Engels. *"The presentations produced in less than 24 hours were really of very high quality. I will continue to follow this group, which has asked to take the exercise a little further to explore the potential of their idea."* ◊

PUBLICATION

A data-driven approach for comprehensive LCA and effective eco-design of the IOT

THE IMPACT OF A SYSTEM CAN BE INFLUENCED BY THE COMPLEX INTERACTIONS BETWEEN EDGE DEVICES AND CLOUD RESOURCES.

The reference flow and the impact contributors of a system could be influenced not only by the local data transit, but also by the complex interactions between edge devices and cloud resources.

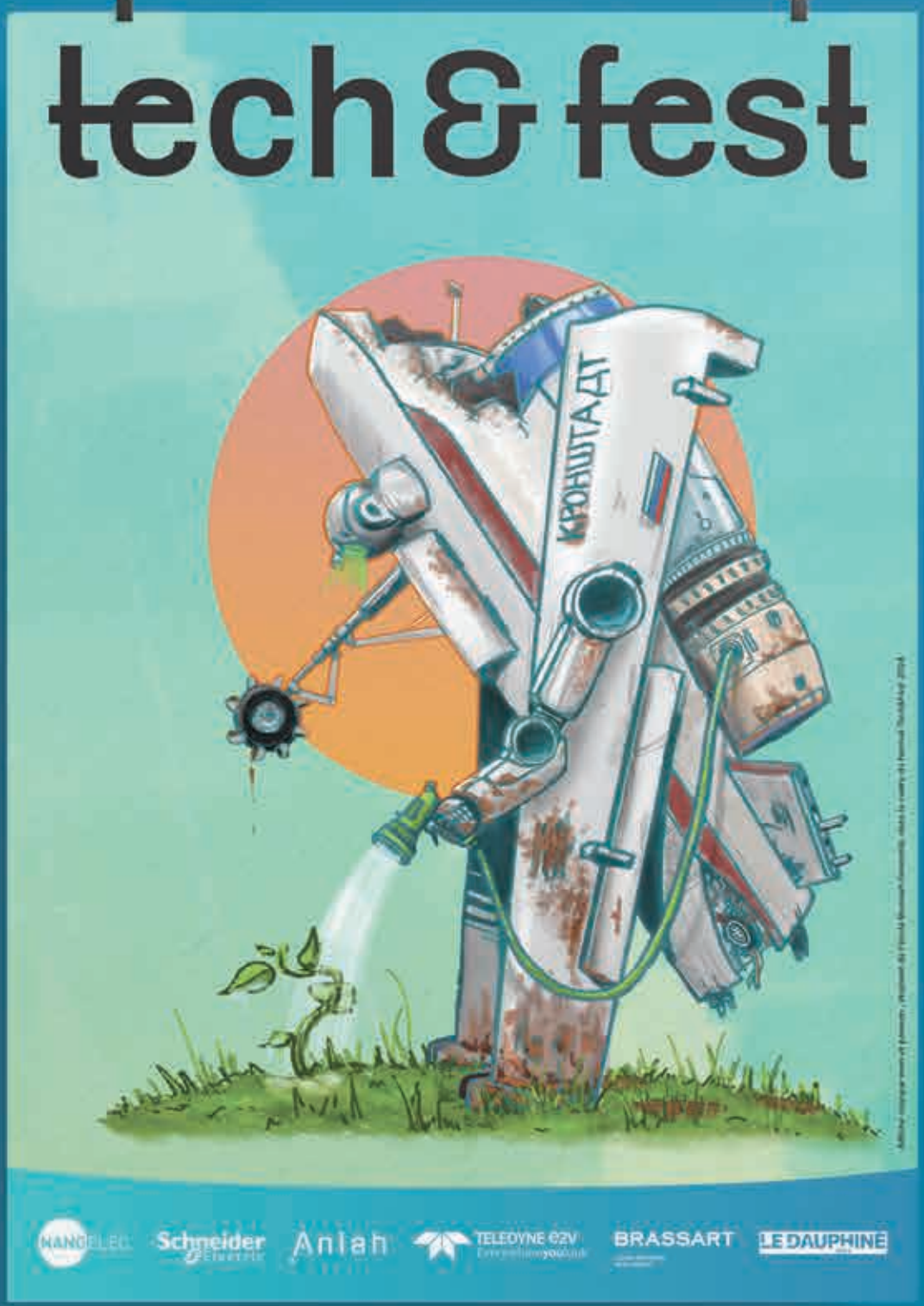
As we reach the limits of our current technologies and the number of connected devices increases, scientists are putting more effort into estimating and reducing the environmental impact of the Internet of Things. Unfortunately, the recent literature on Life Cycle Assessment (LCA) and the eco-design of IoT systems suffers from a major shortcoming: it does not place sensor data at the center of the problem.

Ernesto Quisbert-Trujillo, now a researcher at the G-Scop laboratory (Grenoble INP-UGA), presented his work on methodologies for assessing the frugality of IOT-type connected devices, through the specific case study of a sensor designed to control water consumption in a domestic environment[8]. *"All our results are discussed with the aim of contributing to the state of the art in terms of the environmental impact of the use of complete IoT systems and their sustainable design"*, emphasizes Ernesto Quisbert-Trujillo. His paper, co-authored with Panagiota Morfouli, full professor at Grenoble INP-UGA, was published under the Nanoelec/ Human Capital & Training Design program.

The paper explicitly aims to highlight the essential role of sensor data in the modeling of reference flows, demonstrating its relevance for proper environmental assessment and practical eco-design. *"Ultimately, we verify the importance of sensor data theoretically and empirically, and we conclude that the reference flow and the impact contributors of a system could be influenced not only by the local data transit, but also by the complex interactions between edge devices and cloud resources"*, emphasizes Ernesto. ◊

Photo,
JUST A FUNNY ILLUSTRATION TO UNDERLINE THAT OVER-EQUIPPING OF DIGITAL SENSORS TO CONTROL WATER CONSUMPTION CAN BE COSTLY IN TERMS OF ENVIRONMENTAL IMPACT.
© ROBERT ALLMANN/ PIXABAY

8. Quisbert-Trujillo, E., & Morfouli, P. (2023). Using a data driven approach for comprehensive Life Cycle Assessment and effective eco design of the Internet of Things: Taking LoRa-based IoT systems as examples. Discover Internet of Things, 3(1), 20. https://doi.org/10.1007/s43926-023-00051-4



POSTER CREATED BY ETHAN SANCHEZ, A GRAPHIC DESIGN STUDENT AT THE BRASSART SCHOOL IN GRENOBLE, FOR THE POSTER COMPETITION **"LA MICROÉLECTRONIQUE POUR VIVRE DANS UN MONDE MEILLEUR" (MICROELECTRONICS FOR LIVING IN A BETTER WORLD)** ORGANIZED BY NANOELEC, WITH THE SUPPORT OF SCHNEIDER ELECTRIC, ANIAH, TELEDYNE E2V, FOR THE TECH&FEST 2023 FORUM.

Sustainable development

THE SUSTAINABLE DEVELOPMENT ACTIONS INITIATED AND CARRIED OUT BY THE ACADEMIC AND INDUSTRIAL PLAYERS IN THE ELECTRONICS SECTOR AS PART OF NANOELEC MEET AT LEAST 10 OF THE UN'S OBJECTIVES. HERE ARE A FEW EXAMPLES. THEY CONTRIBUTE TO MEETING TODAY'S NATIONAL AND EUROPEAN COMPETITIVENESS CHALLENGES, AND TO MAKING THE SECTOR EVEN MORE RELEVANT TO TOMORROW'S WORLD.

Photo,
EVERY YEAR, NANOELEC CELEBRATES MARCH 8TH AND JUNE 23RD WITH ROUND-TABLES AND FORUMS QUESTIONING THE ROLE AND THE PLACE OF WOMEN IN OUR BUSINESS
© P. JAYET/CEA 2023

Smart Pixel

A Life Cycle Analysis of Smart Pixel flow under development as part of the Nanoelec/Displed program was presented at Display Week 2023[1]. Since there are no component scale databases for microelectronics, or the literature is outdated and does not reflect current trends, this life cycle assessment (LCA) provides new and previously unseen results. Data are included in the very first demonstration of a calculation tool dedicated to optimizing the key parameters of the environmental footprint of the associated process flow. ◊

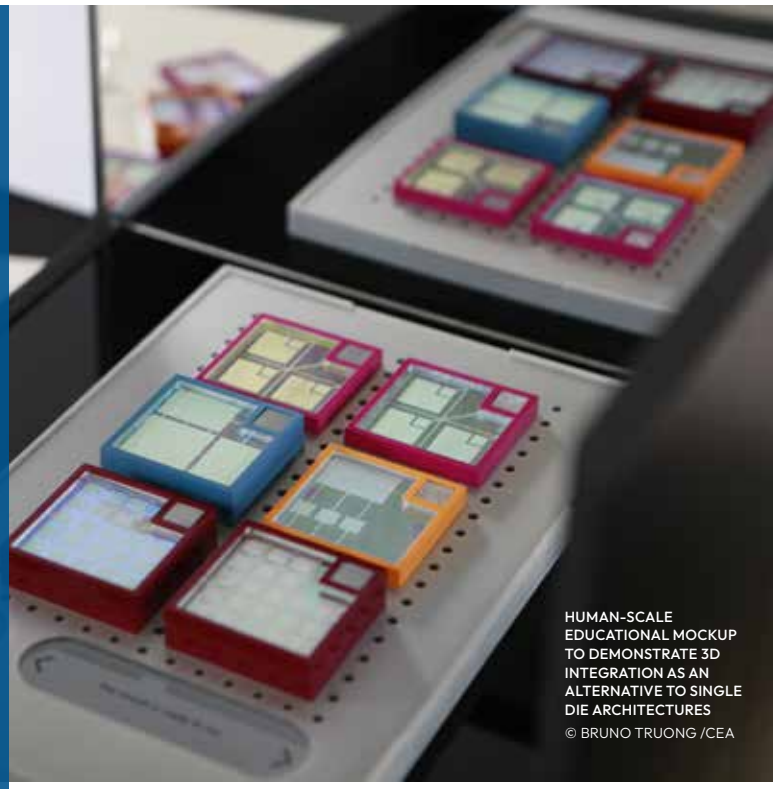
Responsible technology dissemination

With the first implementation in 2023 of the Defi-Ino process at the initiating phase of Easytech projects, we are looking to develop an environmental diagnostic offering for SMEs, mid-caps and start-ups wishing to work with us. Our priority is to help companies cope with the environmental issues of public innovation policies and to provide them with competitive advantages. The proposed diagnostic is quick and inexpensive. It does not replace an actual environmental assessment, nor a life cycle assessment (LCA). Instead, it aims to be a simple evaluation, which could encourage companies to commit to a more detailed study and to change their environmental responsibility culture. ◊

1. Holo, Antonin, Dubarry, C., Lopes, J.-C., Dupont, M., Chabaud, S., & Templier, F. (12-17 May). MicroLED Display Life Cycle Assessment. Display Week, San Jose, USA

Increased versatility & low power consumption for heterogeneous systems

CEA's advanced packaging research leverages expertise in 3D and heterogeneous integration, especially as part of the Nanoelec/Smart Imager program. We have the full range of technologies needed to break up monolithic circuits into modules, or chiplets, and package them in vertically stacked circuits using 3D integration techniques. Due to the increasing costs of advanced nodes and the difficulties of shrinking analog and circuit input-output signals (IOs), alternatives to single die architectures are becoming mainstream. Chiplet-based systems using 3D technologies are compatible with scalable modular architectures, and with technology partitioning based on reusable IP blocks. Moreover, 3D interconnects increase chip-to-chip bandwidth and limit overall power consumption. Industries across the whole range from automotive to health, will soon be relying on advanced packaging to deliver simpler, faster, and cheaper chip designs that integrate more functions while offering greater performance and versatility. ◊



HUMAN-SCALE EDUCATIONAL MOCKUP TO DEMONSTRATE 3D INTEGRATION AS AN ALTERNATIVE TO SINGLE DIE ARCHITECTURES
© BRUNO TRUONG /CEA

Human at the heart, technology at the edge

In 2023, as part of the Nanoelec/Pulse program, CEA-Leti was selected to coordinate a new project called Earashi: a new cascade funding mechanism that aims to improve working conditions (health and safety), trust, and acceptance of collaborative embodied AI in robotic systems. The goal is to support industrial activities, especially start-ups and SMEs, in the development and uptake of advanced eco-responsible digital technologies (in particular AI, data and robotics) that will help workers in their daily activities and improve their working conditions (safety, health and well-being), leading to a productivity increase. ◊

Reducing e-waste

The European EECONE project, in which CEA is involved via the Nanoelec/Pulse program, aims to structure the electronics ecosystem and develop technical solutions to reduce the environmental impacts of electronic technologies on a European scale. In accordance with the 6R concept (Reduce, Reliability, Repair, Reuse, Refurbish, Recycle), twelve technologies will be developed and then applied to case studies in ten use cases, ranging from integrated circuits to printed circuit board electronics and power electronics, in application areas such as automotive, consumer electronics, healthcare, ICT, aeronautics and agriculture. ◊

Training design for green electronics

The Nanoelec/CHIF program involves transforming the teaching approach to promote more dynamic content, in particular with integration of sustainable development and with transformation of teaching methods aimed at increasing learning through experience and accessibility to resources, through a wide diversity of learners on a shared platform. The achievements of 2023 include the publication of a complete module on eco-design for electronics. It includes basic notions on lifecycle and the fundamental principles of LCA (Life Cycle Assesment: inventory analysis, impact assessment, interpretation of results, etc.) along with an approach to eco-design and the development process for electronic products (rational design in the manufacturing, utilization or end-of-life phases). The CHIF program is also associate, through Grenoble INP-UGA to the EU GreenChips-EDU project: the goal is to increase the number of students pursuing studies in electronics and to enhance the professional development of individuals working within the industry. The focus of the degree programs is the development and production of sustainable and energy-efficient microchips. ◊

Attractiveness of micro-electronics

Tensions over the recruitment of qualified personnel have been acute for the past two years. Against this backdrop, Nanoelec joined forces with local industry players to support the work of the departmental industry committee, chaired by the Prefect. In particular, Nanoelec organized in 2023 a regional forum bringing together institutional players, training providers and manufacturers in the sector. Actions are being launched in coordination with the AMI/CMA FAME project and the Comité stratégique de filière électronique (National electronics sector strategy committee). ◊

Parity and equality at work

Every year, Nanoelec organizes round-tables on March 8th (World Day for Women's Rights) and June 23 (International Women in Engineering Day #INWED). This is an international awareness campaign to raise the profile of women in engineering and focus attention on the amazing career opportunities available to girls in this exciting industry. The permanent exhibition on the 2022 Nanoelec awards for women in technology is presented in the Grenoble-Alpes area. ◊

MAY 2023, DURING A NANOELEC/CHIF PROGRAM WORKSHOP: ENGINEERING STUDENTS HAD TO FIND WAYS TO DISCUSS THE CONCEPT OF "SUSTAINABLE ELECTRONICS" AND TO EXPRESS WHAT THEY EXPECT FROM OUR BUSINESS

Increasingly involved in embedded artificial intelligence

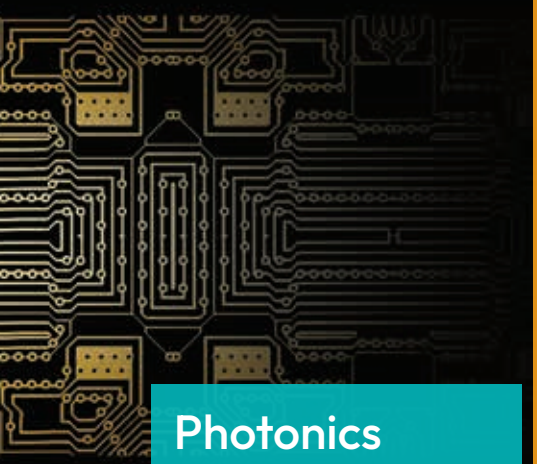
ARTIFICIAL INTELLIGENCE (AI) EXPERTISE IS INCREASINGLY IMPORTANT IN ORDER TO DIFFERENTIATE PRODUCTS DEVELOPED SPECIFICALLY FOR APPLICATIONS.

Nanoelec tackles AI from the embedded electronics standpoint: the development and generalized use of embedded AI applications is becoming essential to manage large quantities of data which require local processing at component and system levels. The aim is to make these components able to make decentralized, autonomous and reliable decisions.

Data processing must therefore be integrated close to the sensor in order to optimize the data stream and guarantee that the information remains intact and confidential. This offers a good compromise between the data streams from the sensor to the user and the energy footprints of the sensor and central computer processing smaller quantities of data.

The teams involved at Nanoelec are primarily focusing on image sensors and on the secure components and artificial intelligence systems.

Whether for designing new circuits and architectures, taking account of the environmental impacts of the technologies, or developing dedicated components, AI is identified as one of the major challenges for the electronics sector over the coming years and the Nanoelec partners have confirmed their interest in the subject.



Photonics on silicon

With the photonics on silicon platform developed at CEA-Leti, the teams mobilized in the Nanoelec/Photonic Sensors program are involved in a number of European projects to develop neuromorphic architectures dedicated to artificial intelligence applications (learning and inference) for ultra-fast detection of cancer cells (flow cytometry), security applications, image recognition and telecommunications. The circuits studied consist a pulsed laser associated with a Mach-Zehnder interferometer array controlled by BTO base phase-shifters. Developments are expected in lasers integrated on silicon and the use of non-volatile phase shifters based on phase change materials (PCM). ◊

Security of Machine Learning

Given the increasingly widespread use of neural network models, in particular in mission-critical embedded systems, the need to evaluate their security to guarantee their reliability is becoming urgent. More specifically, the models deployed in embedded platforms are physically accessible to attackers during the product lifecycle and thus vulnerable to hardware perturbations. Teams in Nanoelec/Pulse program study the threats by characterizing the vulnerabilities as well as the main defenses approaches by developing countermeasures on a wide range of hardware platforms. ◊

Autonomous vehicle

A team from Inria and its industrial partners, working within the framework of Nanoelec/Pulse, are focusing on the validation of artificial intelligence (AI) systems for mobility/vehicles. In 2023, they presented a new navigation-based metric to evaluate the similarity between occupancy grids. The study used a machine learning model that combines LIDAR data and camera data to generate semantic grids for different classes. The issue of evaluating and validating the efficiency of these technologies is one of the last major hurdles to the adoption of in-vehicle context capture technologies to enable vehicles to operate autonomously. ◊

Safe and autonomous smart hoisting

Autonomous Intelligent Vehicles (AIV) or Autonomous Mobile Robots (AMR) are now a feature of the industrial production chain. This new mobile handling technology must be able to be integrated without endangering the production line, surrounded by human employees. Following the mathematical modelling of an overhead crane, a team working under Nanoelec/Pulse defined an approach to the overhead crane control problem aimed at optimizing the parameterization of existing controllers. An AI learning pipeline for AI incorporating a digital simulator was then set up to assess and validate this approach before testing it on a physical simulator. ◊

AI for embedded intrusion detection

For several years now, CEA has been working on the use of hardware information to detect microarchitectural attacks, such as Spectre or Rowhammer, as well as attacks with an impact on the system, such as a cryptolocker. The Nanoelec/Pulse teams have developed an anomaly detection approach based on machine learning. The model is trained using only data on the normal behavior of the system to characterize it. During inference, any deviation from this normal behavior detected by the model is considered an anomaly. The results of this solution are highly promising, both in terms of sensitivity (all attacks detected) and specificity (no false alarms). ◊

Artificial intelligence of objects

The InSecTT EU program partners believe that Artificial Intelligence of Things (AIoT) is the natural evolution for both AI and IoT because they are mutually beneficial. AI increases the value of the IoT through machine learning by transforming the data into useful information knowledge, while the IoT increases the value of AI through connectivity and data exchange. Nevertheless, cybersecurity is crucial to protect data and privacy. Several platforms have been set up to evaluate and demonstrate the embedded neural network inference security technologies developed. The Nanoelec/Pulse teams focused in particular on mechanisms for authenticating the integrity of neural network inference embedded on a hardware platform based on blockchain and hardware secure components ◊

A third layer to support edge AI on the imager

Imaging is one of the three main fields that use AI. The aim is not only to achieve better image quality, but also to extract relevant data from the image, taking account of the environment, the object and the scene (potentially across a range of lighting conditions), and knowledge of the context.
The main objective of the Nanoelec/Smart Imager program is to prepare a 3D-stack technology to integrate the processing of artificial intelligence directly into an image sensor.
Research teams working on the Nanoelec/Smart Imager program are focusing on new advanced silicon technology bricks allowing 3D sensor assembly, on the design of new architectures allowing the implementation of adapted neural networks, and on the development of new design methodologies and tools simultaneously taking account of software and hardware requirements in dedicated EDA tools. ◊

Merging multimodal images

Teams involved in the Nanoelec/System Lab initiative define, develop and test cases using embedded AI technologies that are integrated into or associated with multiple image sensors. With regard to spatial coherence of images from different sources, data merging is based on artificial intelligence solutions. Artificial intelligence is usually developed specifically for a given use case in order to exploit nothing but the pertinent data. ◊

International & Europe

In an international context that underscores the challenges of sovereignty, the Nanoelec teams have decided to consolidate an international strategy around a few simple principles:

➔ Giving priority to reinforcing the positions of the consortium's current members, which already have global reach but which are faced with international competition: at least, five of our core partners have a global footprint,

➔ Continuing support for national startups capable of addressing international markets,

➔ Accelerating international partnerships, in particular in the fields of materials and production or instrumentation equipment: Nanoelec runs associated projects with major actors from Europe, North America and Oriental Asia,

➔ Finally, re-energizing Europe within the new framework programs and the Chip Act

From the scientific viewpoint, it is worth noting the presence at various major conferences in 2023: IEEE Silicon Photonics, Date for design work, ECTC for 3D integration technology, FIC for cybersecurity, Display Week, Mems & Imaging Device Summit.

European projects adopting Nanoelec's technology and know-how

Cytometry

Partners of the EU Neoteric project are developing a reconfigurable photonic circuit to detect cancer cells in a solution (cytometry) using a machine learning (ML) method. ◊

https://neoterich2020.eu/

Neuromorphic computing

The EU Prometheus project aims to manufacture a complete neuromorphic computing chip (set of interferometers using low-consumption BTO-based phase shifters for the synaptic part and pulsed lasers integrated on silicon for the neural part). ◊

https://prometheus-he.eu/

Secure hardware accelerators

For the first time, EU Neuropuls will develop secure hardware accelerators based on novel neuromorphic architectures and PUF-based security layers leveraging the benefits offered by the integration of photonics, PCMs and III-V materials. ◊

https://neuropuls.eu/

Nanomecha-nical materials characteriza-tion

NanoMECommons is an H2020 collaborative project focusing on the development of new characterization methodologies tailored to industrial needs in the nanomechanical field. ◊

https://www.nanomecommons.net/

Addressing key bottlenecks in nanoscience research

NFFA (Europe's Nano Foundries and Fine Analysis Pilot) is an H2020 collaborative project which prefigures the first distributed research infrastructure within the EU, offering access to high-level instrumentation in the field of nanosciences and nanotechnologies. ◊

https://www.nffa.eu/

Exploring radiation effects

Radnext (for RADiation facility Network for the EXploration of effects for indusTry and research) is an H2020 collaborative project aiming to launch a distributed research infrastructure within the EU devoted to the industrial and university irradiation community. ◊

https://radnext.web.cern.ch/

Digitizing European industry

DigiFed has involved over 200 SMEs and mid-sized companies from all over Europe in its innovation program to demonstrate the benefits of digital technologies in terms of hardware security and privacy, human-machine interaction and autonomy for small and medium enterprises. ◊

https://digifed.org/

Reducing e-waste

The main aim of the EECONE project is to reduce electronic waste on a European scale through a vision including the responsible management of the end-of-life of electronic products right from the development or process design stage. Led by Infineon Technologies, the project brings together 49 partners from 16 European countries covering a wide range of sectors, including STMicroelectronics and CEA through Nanoelec, one of the 15 French partners. With a budget of €35 million, EECONE is paving the way for a zero-waste electronics industry. ◊

https://www.eecone.com/eecone/home/

Ethical IC for police investigation

The EU Poliiice project ushers in a new lawful-interception, investigation and intelligence era, including technologies like 5G&Beyond, end-to-end encrypted communication and Quantum based encryption, in a dedicated legal and ethical framework strictly complying with preservation of privacy and ethical rules of operation. Within Nanoelec/Pulse, CEA has developed a new Type 1 Cyber Intelligence, which does not require physical access to the target, that extracts secrets via leaks in the microarchitecture. ◊

https://poliiice-project.eu/

Artificial intelligence of things

The EU InSecTT (Intelligent, Secure, Trustable Things) project aimed to combine the Internet of Things (IoT) with Artificial Intelligence (AI) by building trust in AI-based smart systems and solutions. InSecTT focused on the security of embedded AI. As a partner in this three-year project, CEA-Leti developed innovative solutions at Nanoelec to authenticate intelligent systems and protect them from various cyber-attacks. ◊

https://www.insectt.eu/

AMONG INITIATIVES SUPPORTED BY EARASHI EU PROJECT, A PROJECT TACKLES ONE OF THE MAIN CHALLENGES IN THE PRODUCTION MACHINES/ TOOLS SECTOR, AND SPECIFICALLY IN THE FOOD INDUSTRY. THE AIM IS TO IMPROVE WORKING CONDITIONS IN TERMS OF HUMAN SAFETY, STRESS, AND WELL-BEING SINCE WORKERS ARE RESPONSIBLE FOR CONTROLLING MACHINES AND TOOLS TO PROCESS RAW MATERIALS IN ORDER TO PRODUCE FOOD PRODUCTS

AI &robotics for human-oriented industry

The EU's Earashi project aims to support European startups and SMEs in the adoption of advanced eco-friendly digital technologies to help workers in their daily activities and improve their working conditions, leading to increased productivity, while respecting privacy and data protection. Nanoelec/Pulse offers hardware components, building blocks and expertise in cybersecurity. ◊

https://earashi.eu/

Photo,
YOUNG PEOPLE ARE LOOKING FOR JOBS THAT MAKE SENSE FOR SOCIETY, IN MICROELECTRONICS AS IN ALL OTHER FIELDS
© A.HAVRET/CEA 2024

Training design for greener chips

The overarching goal of the GreenChips-EDU project is to increase the number of students pursuing studies in electronics and to enhance the professional development of individuals working within the industry. The focus of the degree programs is the development and production of sustainable and energy-efficient microchips. ◊

https://www.unite-university.eu/unitenews/novel-education-programmes-for-sustainable-microchips-made-in-europe

Training design to address the transformational challenges facing businesses

The aim of the EU Digi-Me project is to create, develop and nurture a European community of leaders capable of designing, initiating and implementing innovations based on advanced digital technologies (AI, generative AI, augmented intelligence, digital twin, blockchain, data analytics, and IoT), in order to meet the strategic and transformational challenges facing businesses. ◊

Graphic Designers sketch our industry

IN RESPONSE TO OUR "COMMISSION", AND LIKE TRUE PROFESSIONALS, GRAPHIC ARTS STUDENTS SENT US WORKS MIRRORING THE MESSAGES CIRCULATING THROUGH SOCIETY ON THE SUBJECT OF MICROELECTRONICS.

For the very first Tech&Fest festival, in February 2024, 45 graphic arts students from the Brassart school took up the challenge thrown down by the microelectronics players in the Alps region (Teledyne E2V, Aniah, Schneider Electric) and coordinated by Nanoelec to design a poster on the subject: *"Microelectronics for living in a better world"*.

Their messages are particularly valuable in terms of the attractiveness actions taken by the sector and the employer-brand strategies. Either by conviction, or with professionalism, these 45 students chose to give a vision of the present and the future where technology and environment come together to work for a fulfilled society. You will find the best creations on your way through this report.

→ JURY

Yee Hsien Tan
Senior Industrial designer at Schneider Electric

Maxime Rumpler
VP Sales & Communication at Aniah

Eric Maze
Industrialization, methods and support manager at Teledyne E2V

Hughes Metras
Director of IRT Nanoelec

Florence Tourancheau
Director of the Brassart-Grenoble school

Laura Perrard
Co-director of the Tech&Fest/Ebra festival

Eugénie Fauny
Plastic artist

Melina Herenger
Vice-president of Grenoble-Alpes Metropole, in charge of tourism, attractiveness, innovation, the university and quality of life

Jean Lou Philippe
Director of France Bleu Isère

Damien Bouevin
Coordinator of the Nemeton biolab

Corine Lemariey
Delegate metropolitan Councilor at Grenoble-Alpes Métropole, President of the public cultural cooperation establishment (science & techniques) Territoire de sciences

Bilel Mcharek
photographer

Clément Berthet
Culture/leisure journalist, Le Dauphiné libéré newspaper

→ ORGANIZING COMMITTEE

François Legrand
Head of communication at IRT Nanoelec

Laurent Cremillieux
Partnership Ecosystem Office Lead at Schneider Electric

Maxime Rumpler
VP Sales & Communication at Aniah

Loic Bommersbach
Communication Manager at Teledyne E2V

Sandrine Maubert Deputy director of IRT Nanoelec

Benjamin Coron
BtoB Activities Director and Co-director Tech&Fest/ Le Dauphiné libéré

Florence Tourencheau
Director of the Brassart-Grenoble school

Just imagine if electronics has not gone micro-nano

Twenty-three students from the Graphic Design section worked on an **"imaginary universe free of microelectronics"**, with a visual approach primarily using photo manipulation. In their presentations, they identified very precise themes regarding developments in microelectronics and digital technologies in general. Most of the posters contain several interwoven messages.

These creations take us back to the 80s/90s, with their magnetic tapes, large radio sets, cassettes and floppy disks. The students take us into a universe where computers have green screens, TVs have very large cathode ray tubes, etc. With humor they point out the permanence of the conversational streams on the social networks, the miniaturization of smartphones by comparison with our old landline phones. ◊

Nature and technology come together

The 22 creations by the students from the Graphic Arts section are true graphic illustrations entirely created by the students. They are all based on the Solar Punk movement, which references a world in which **"Nature and technology come together"**. According to Wikipedia, Solar Punk is an "optimistic vision of the future that rejects climate doomerism" as well as social inequalities.

These creations highlight an "architecture, as receptacle for invisible digital technologies", "technological advances, a future in which towns are green and ecological". They project us into an era of successful space conquest, a society where people live well together, into a "healthy future in which technology and biodiversity are closely intertwined", with robots working market gardens, reconditioned for regenerating nature..., an era in which bio prosthetics are transparent and worn naturally, for the animal or human world. ◊

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