Last update in

Photonics technology towards edge performance sensors

NANOELEC.

Join us at IRT Nanoelec webinar

On Monday, July 6th 2020, 5pm CET

Last update in
Photonics technology
towards edge performance sensors
Live webinar July 6th 2020

NANOELEC.

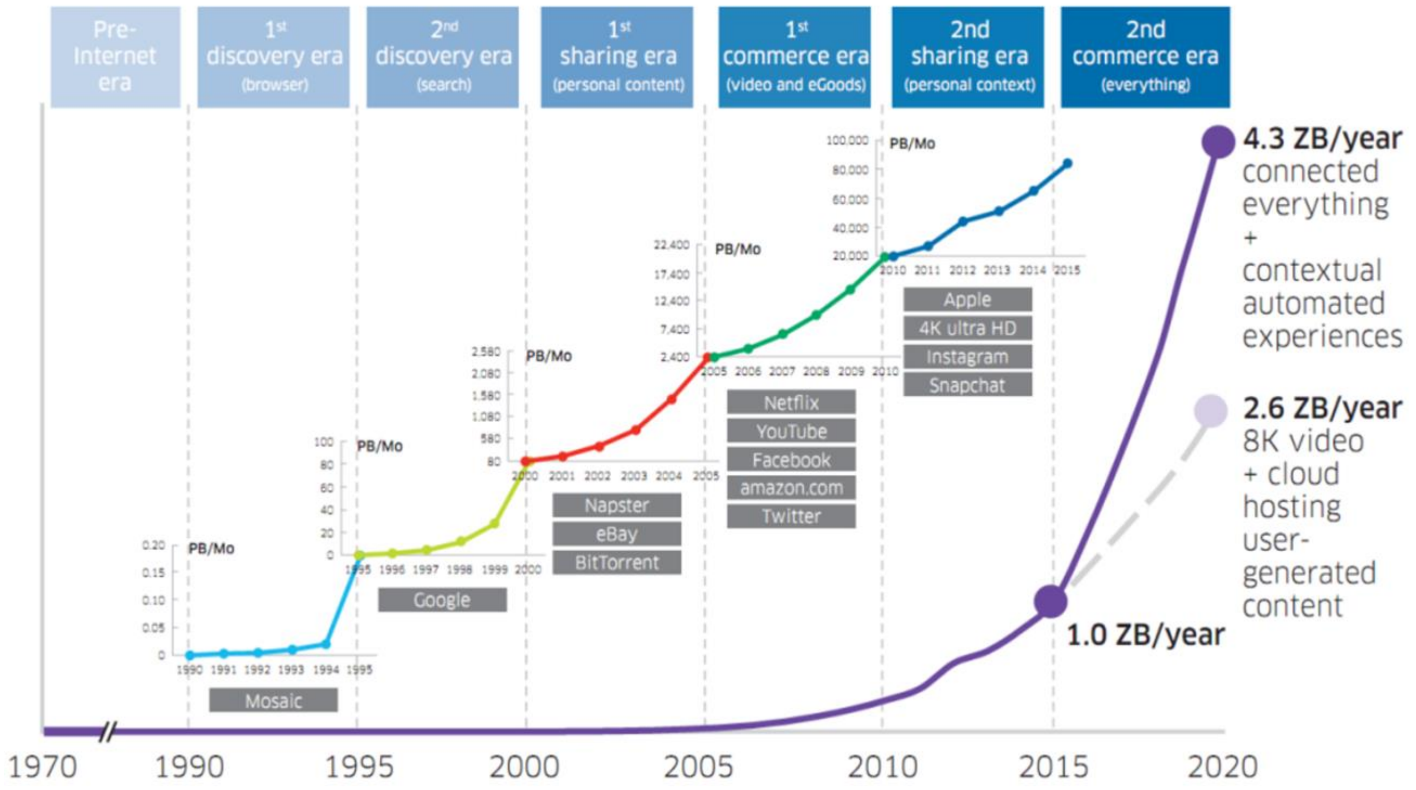
Photonic devices with reduced In, Ga content

Baron Thierry, Webinar

06/07/2020

Data exchange

Big data, Artificial Intelligence, Quantum computing …



M. K. Weldon, The Future X Network. Taylor & Francis Inc, 2016

Data transmission

Data transfer, RF
Cloud computing,
AI …

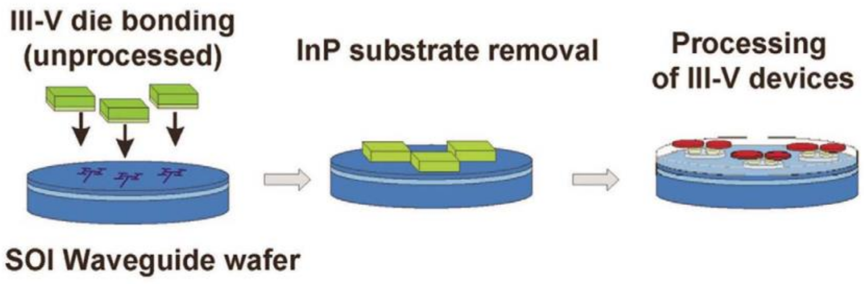
Si photonics = best of two worlds, Si platform + III-V physical properties

- **Based on hardware devices to, collect, process, store, exchange datas**
- **III-V, noble metals,… co-integration with silicon**

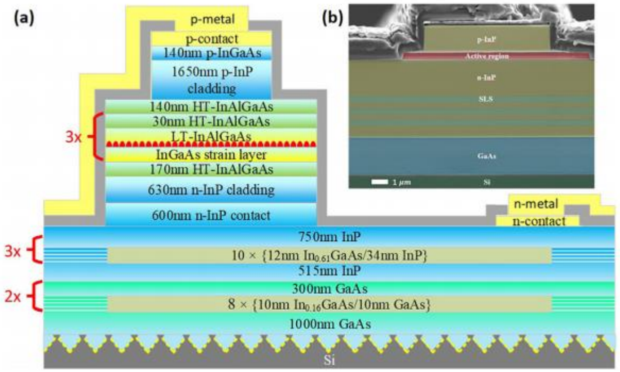
III-As,P integration in a silicon platform

- 3 major integration schematics
  - Molecular bonding
  - Regrowth on bonding template
  - Direct growth of III-V on silicon

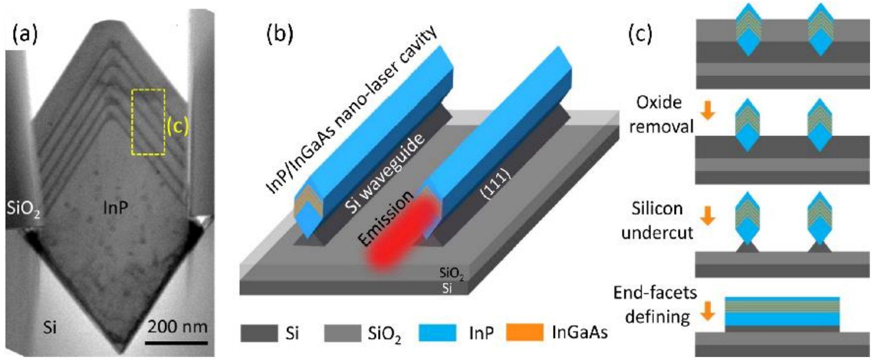
100G CWDM4 Optical Transceiver from Intel



Roelkens et al. Materials Today, Elsevier BV, 2007, 10, 36-43



Luo et al. Appl. Phys. Lett. 116, 142106 (2020)



Shi, Yuting. “GaAs nano-ridge lasers epitaxially grown on silicon.” (2020).

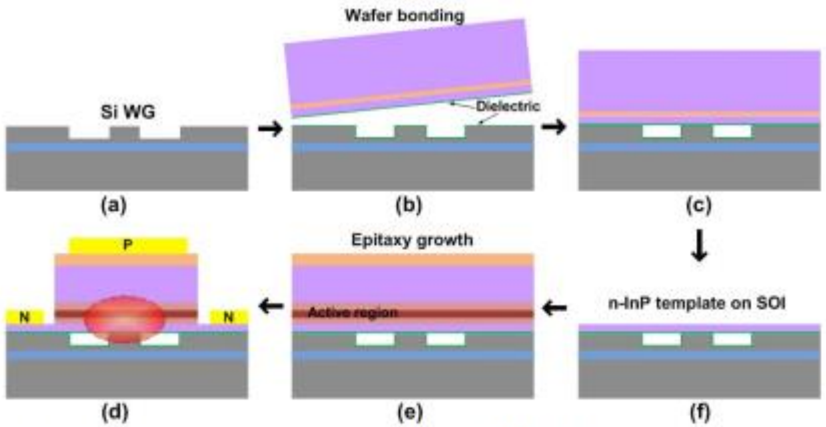


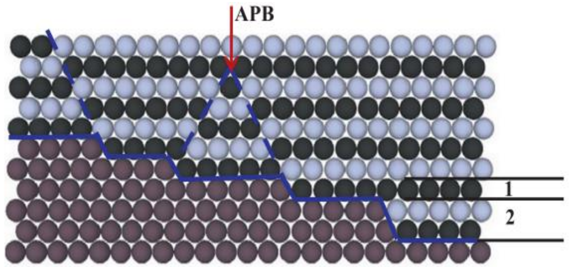
Fig. 1. Schematic process flow of III-V to Si integration.

Hu et al. Vol. 13, No. 23 / OPTICS EXPRESS 9460-9464

- III-V heteroepitaxy on standard CMOS Si substrates

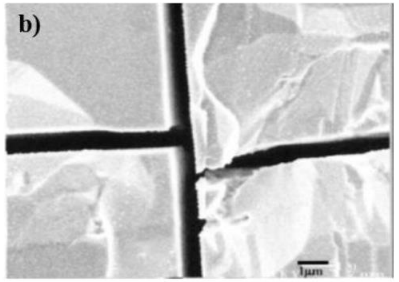
Challenges for III-V direct epitaxy on Si

Antiphase boundaries



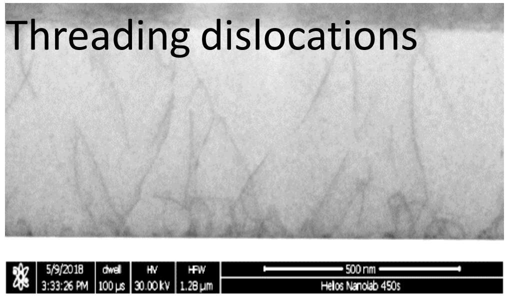
S. Lourdudoss, *Current Opinion in Solid State and Materials Science*, vol. 16, no. 2, pp. 91–99, apr 2012.

Thermal expansion coefficient

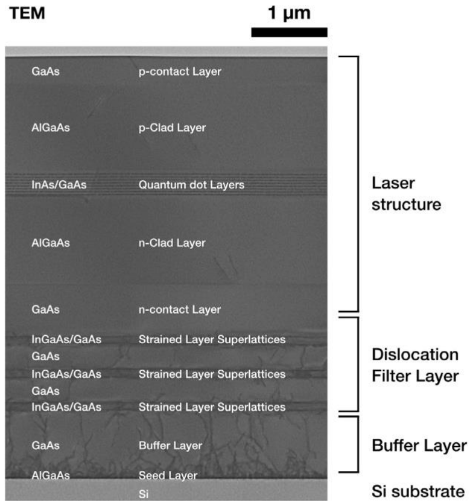


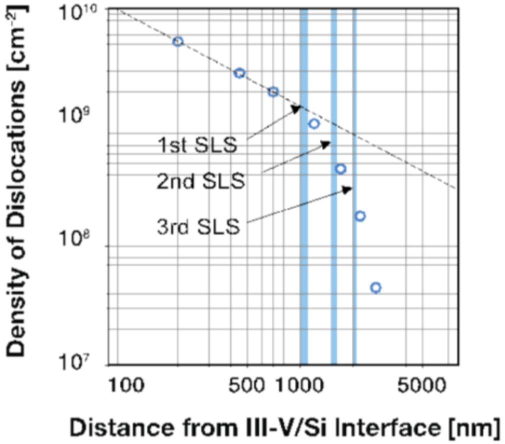
Yang, V. K et al. *Journal of Applied Physics, AIP Publishing*, 2003, *93*, 3859-3865

Lattice mismatch



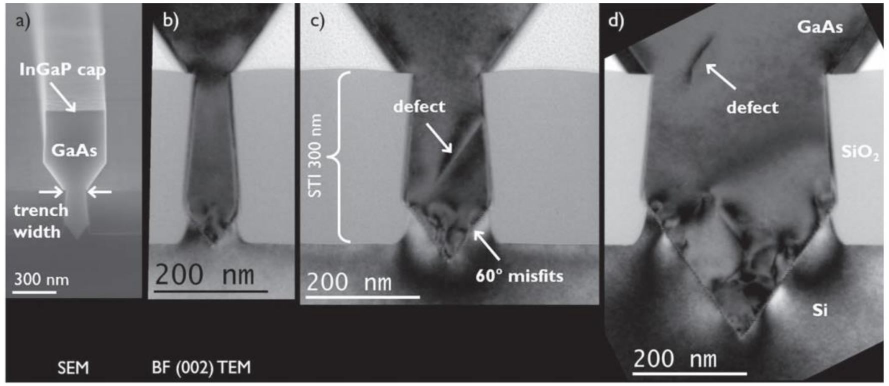
Thick buffer layer (TD in 10^7 cm^{-2} range)





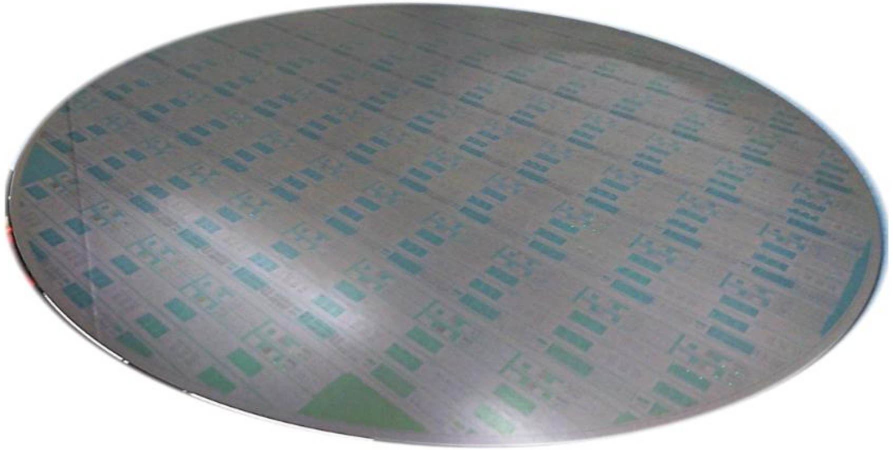
J. Kwoen et al, Vol. 26, No. 9 | 30 Apr 2018 | OPTICS EXPRESS 11568

Selective epitaxy (TD less than $3x10^6$ cm^{-2})



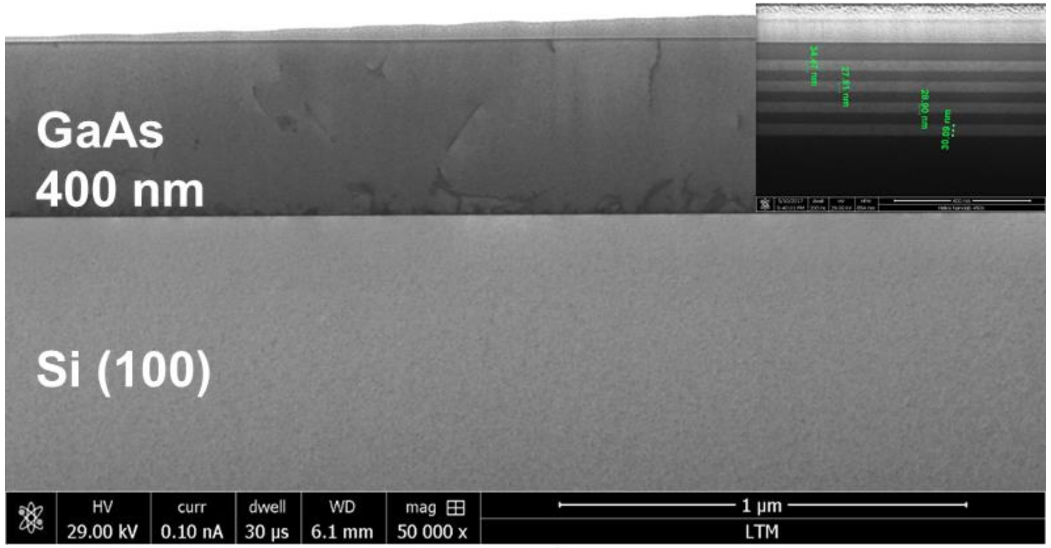
B. Kunert et al 2018
Semicond. Sci. Technol.
33 093002

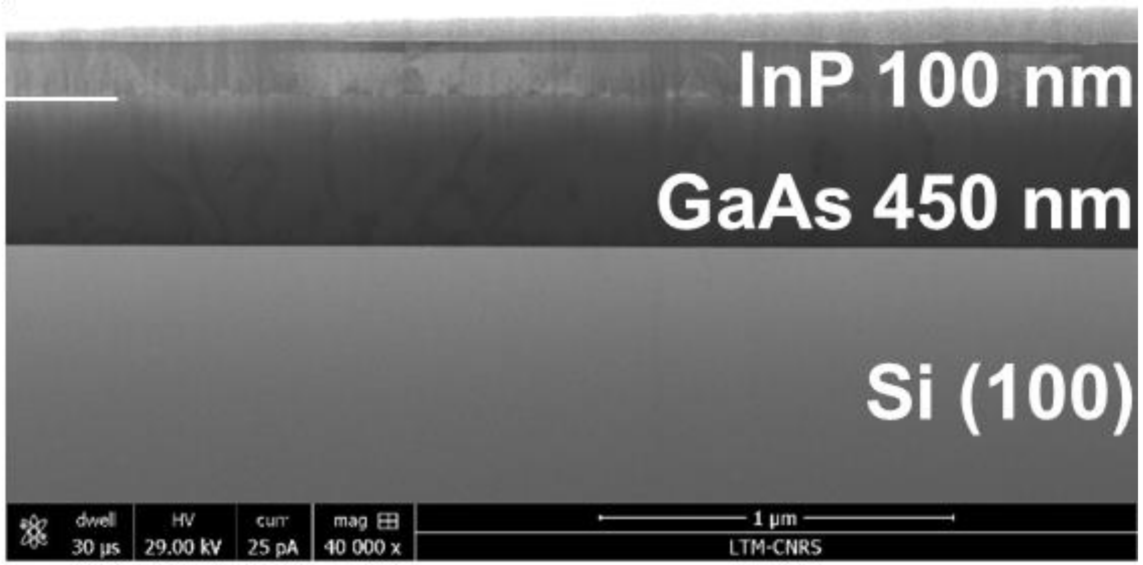
Compatibility with current fab

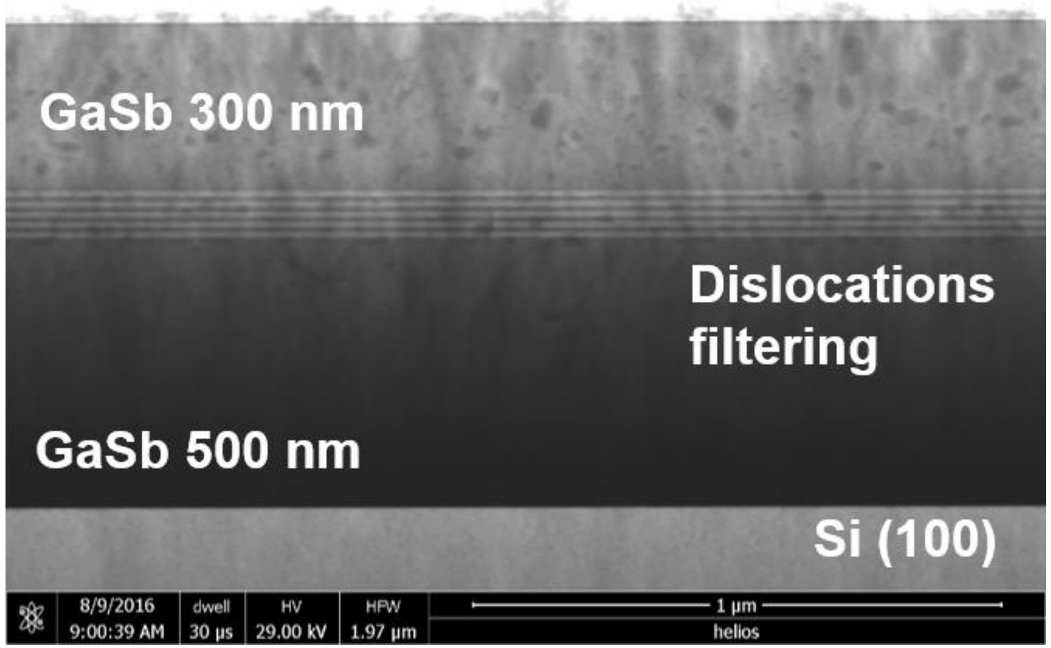


- Large scale deposition process, 300 mm Si(100) wafers
- Metalorganic chemical vapor deposition (MOCVD)
- CMOS clean room compatibility
- In-situ cleaning of the wafers

GaAs, InP, GaSb thin APB free buffer layers on Si(100)





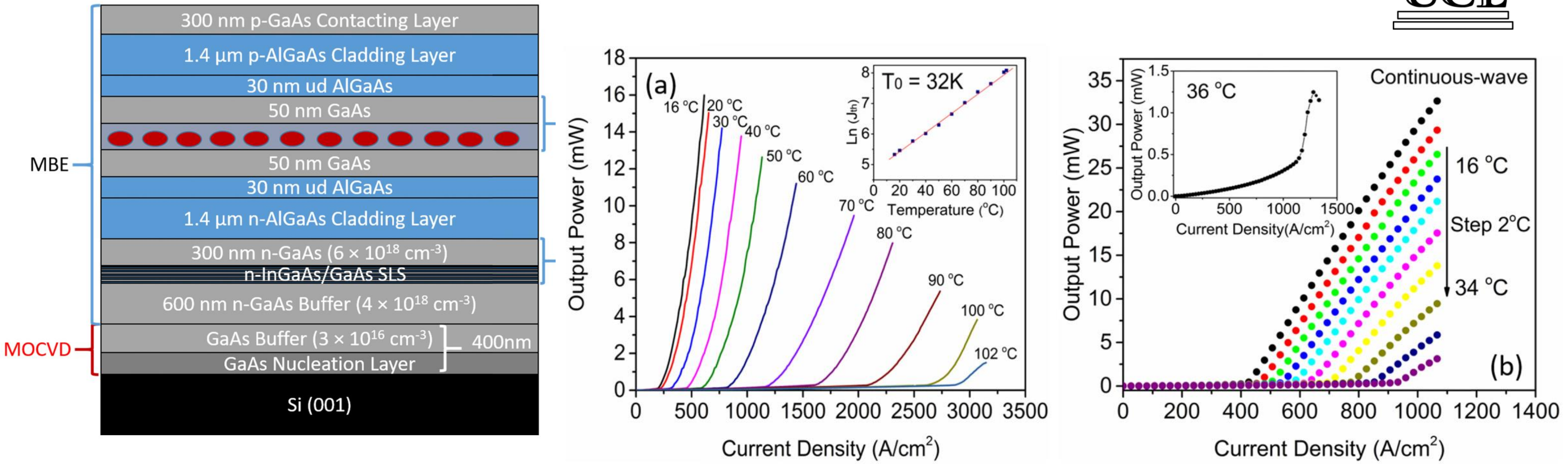


- Fabrication of thin layers (<1 µm) pseudo substrates No APB
- Gain in materials consumption
- Engineering is still necessary to decrease the structural defect density (currently in the 10^8-10^9 cm^{-2} for thicknesses between 400 nm to 1 µm)

- Devices demonstration

R. Cipro et al., APL 104(26), N°262103 (2014); R. Alcotte et al., APL MATERIALS, 4 (4), N°046101 (2016);
M. Martin et al., APL, 109(25), N°253103 (2016); J. Widiez et al., JJAP, 55 (4), N° 04EB10 (2016)

First QD laser directly grown on on-axis Si substrate collaboration UCL in 2016



S. Chen et al., Optics Express, vol 5, no. 5, 4632, 2016

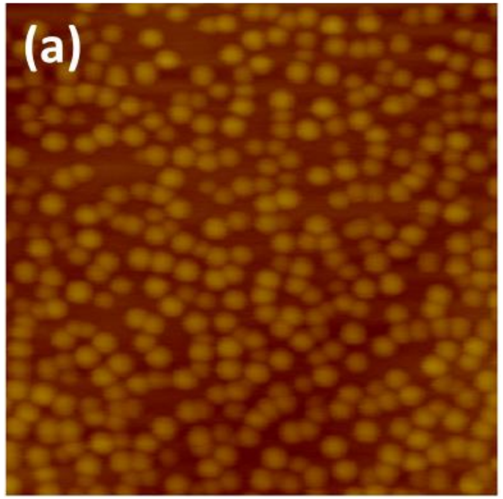
λ = 1.3 µm, electrically pumped, 400 A/cm² threshold current density

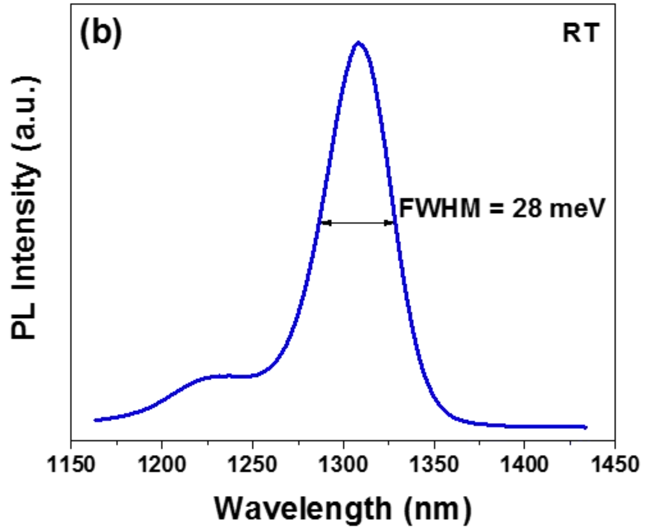
Maximum operating temperature: 34 °C (CW)

Characteristic temperature T0 32K

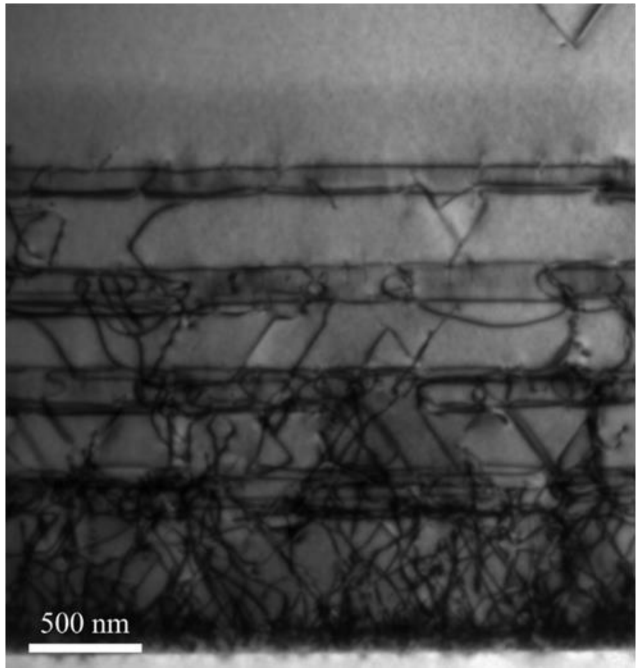
Further improvement of QD laser

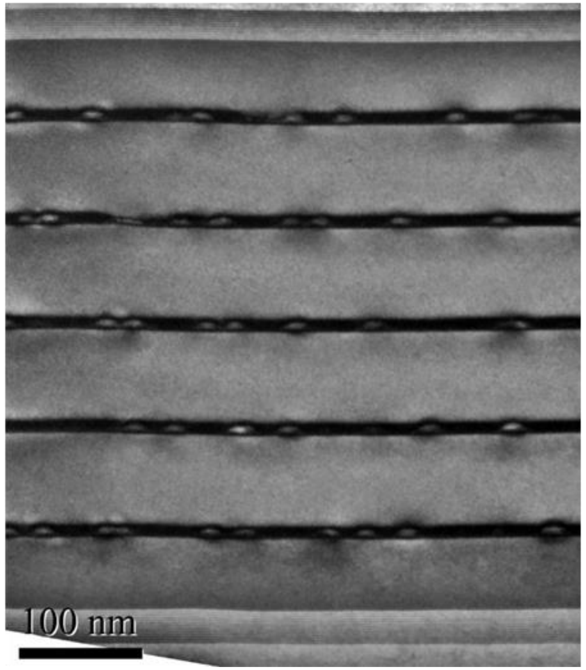
- **Optimisation of QD, FWHM 28 meV**
- **4 sets of Defect filter layer successfully reduce the threading dislocation density to 10^7 cm^{-2}**
- **Threading dislocations are most eliminated within DFLs**





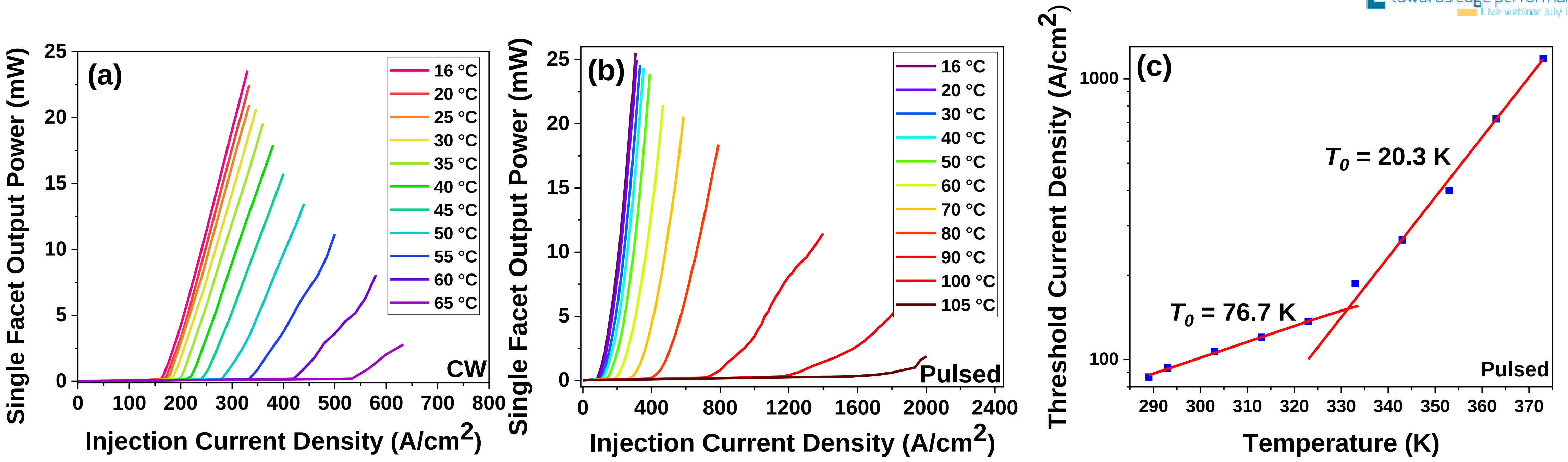
DFL 4
DFL3
DFL2
DFL1
GaAs buffer

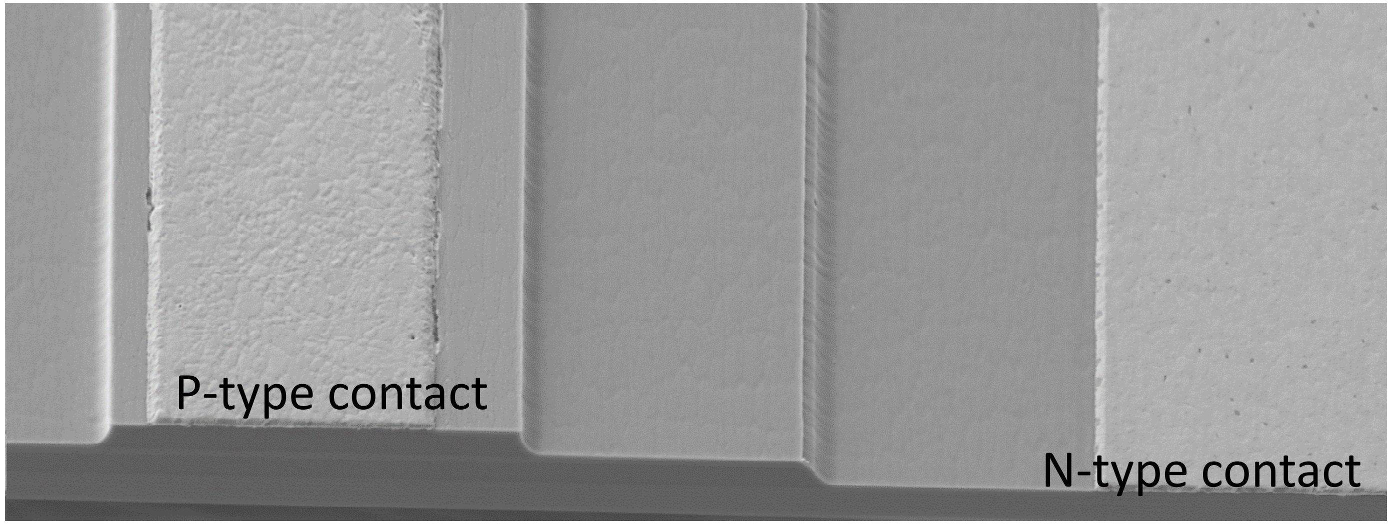




UCL

Further improvement of QD laser





As-cleaved facet

λ = 1.3 μm

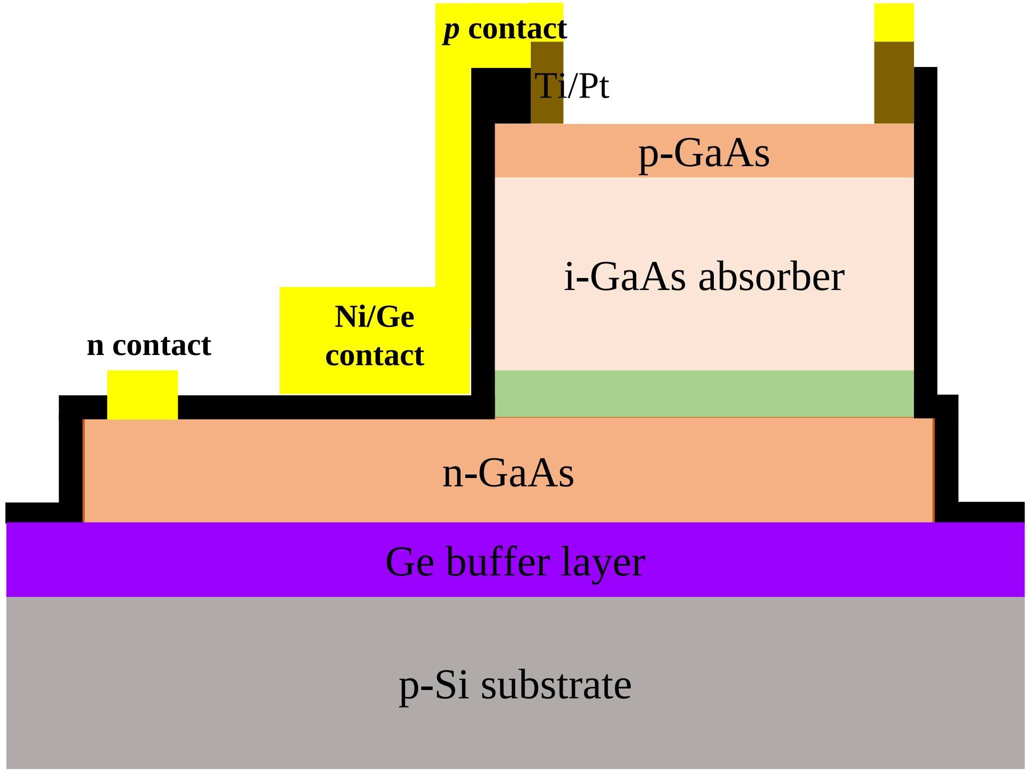
Threshold current density 164 A/cm^2 at room temperature

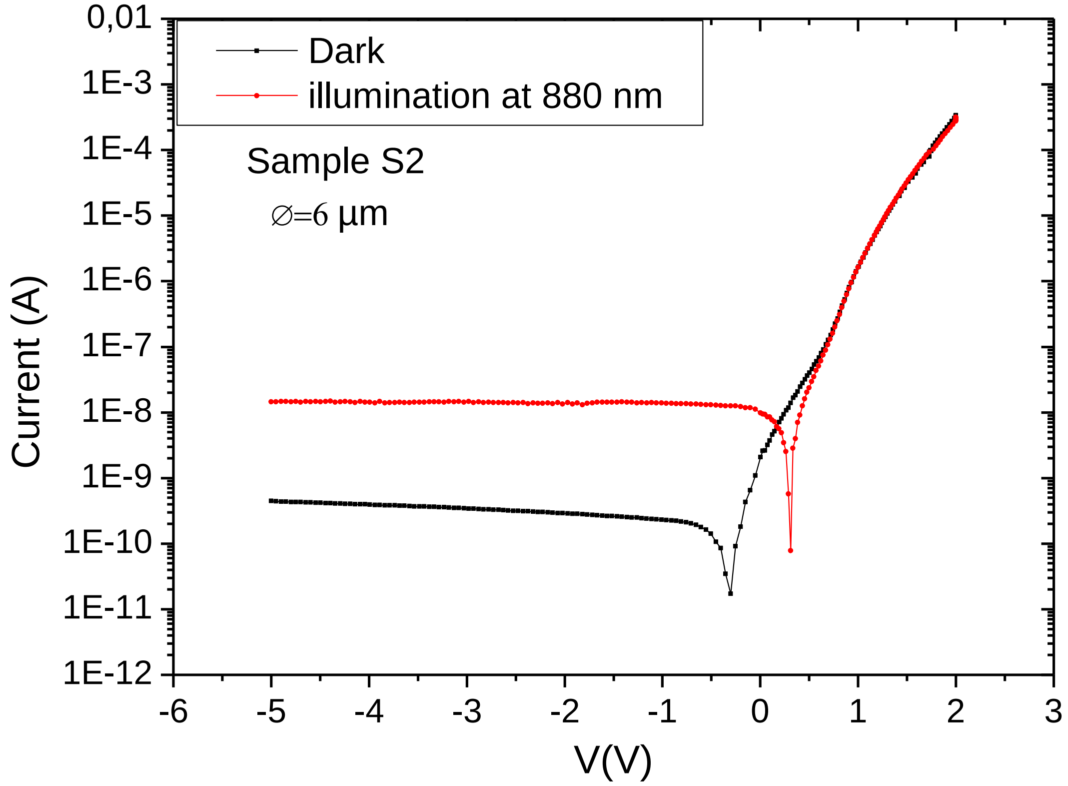
Maximum operating temperature increase to 65 at CW operation

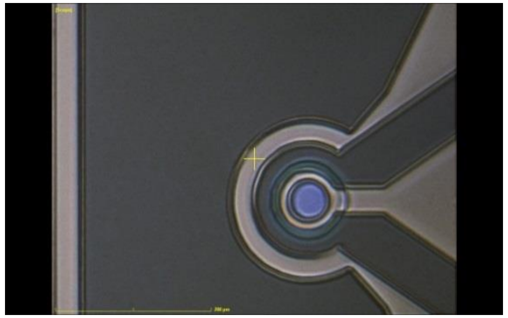
T0 76.7K

Z. Liu et al., Journal of Lightwave Technology, 2019

GaAs photodetector on Ge/Si(100)





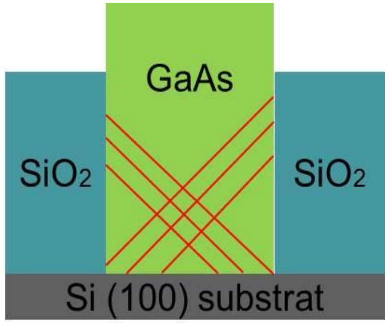


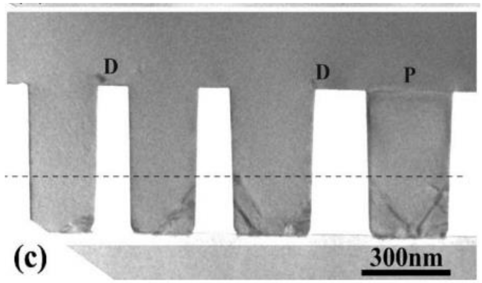
- t<1 µm
- $I_{reverse}$ depend on light illumination
- Brand new results, further characterization and optimization in progress
- Devices were done with TD $1x10^{8}$ cm^{-2}
- Current TD on Ga/Ge/Si(100) is around $2\text{-}3x10^{7}$ cm^{-2}

H. Medhi, L. Virot et al., and JM Hartmann for Ge buffer layer

Process efficiency : selective growth on Si(100)

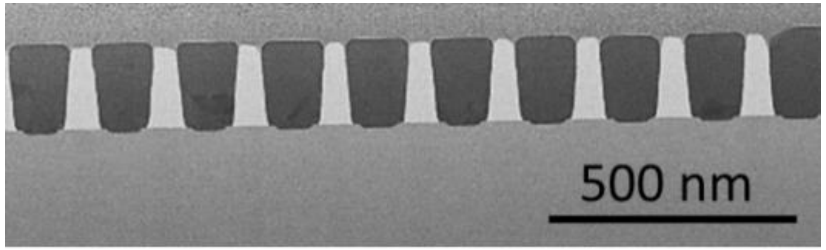
- Aspect Ratio Trapping selective epitaxy
  - Put the materials at the useful position
  - Reduce the structural defects density

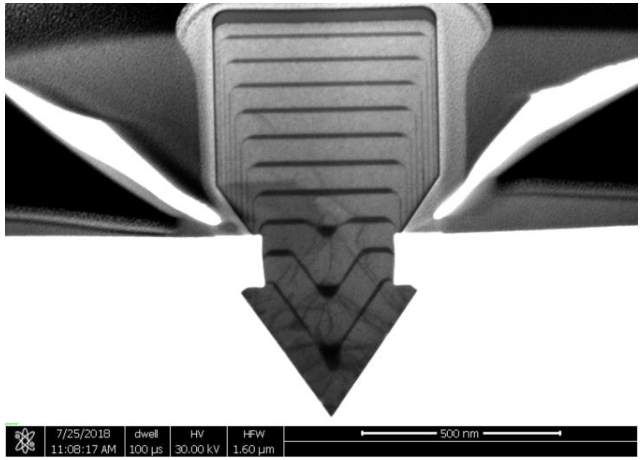


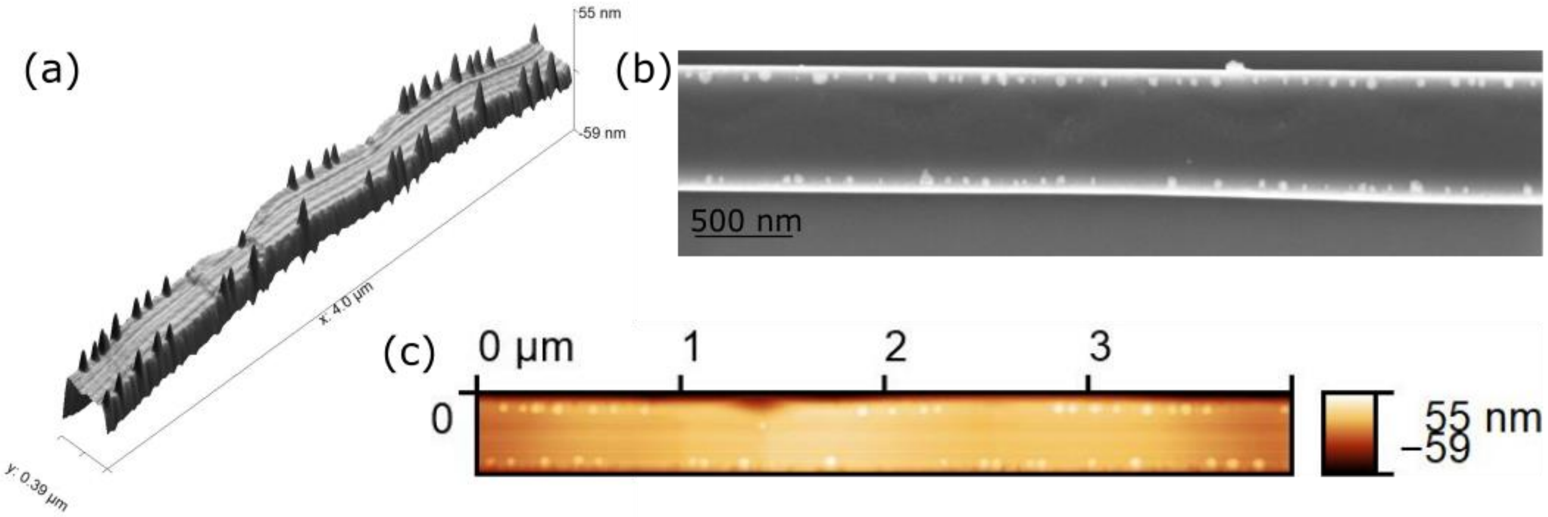


J.Z. Li et al., APL 91, 021114, 2007

- **The materials is deposited only at the desired place**
- **GaAs selective deposition, and quantum wells structures**







ML. Touraton, PhD Univ. Grenoble Alpes (2020)

Conclusions

- A lot of developments have been done recently on III-As and III-P heteroepitaxy on Si(100) substrates
- Demonstration of electrically pumped CW laser at room temperature for 2D structures epitaxially grown @ 1,3 µm
- Demonstration of optically pumped laser at room temperature for selective epitaxy grown structures @ 1,3µm and 1,55 µm
- Need to be demonstrate : electrically pumped laser for selective epitaxy
- Integration in a Si photonics chip

Thank you for attention

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MEMBER

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