Last update in
Photonics technology
towards edge performance sensors
Live webinar July 6th 2020

NANOELEC.

III-V/Si Hybrid laser large scale integration in CMOS friendly process

Bertrand SZELAG

06/07/2020

Silicon Photonics Building Blocks

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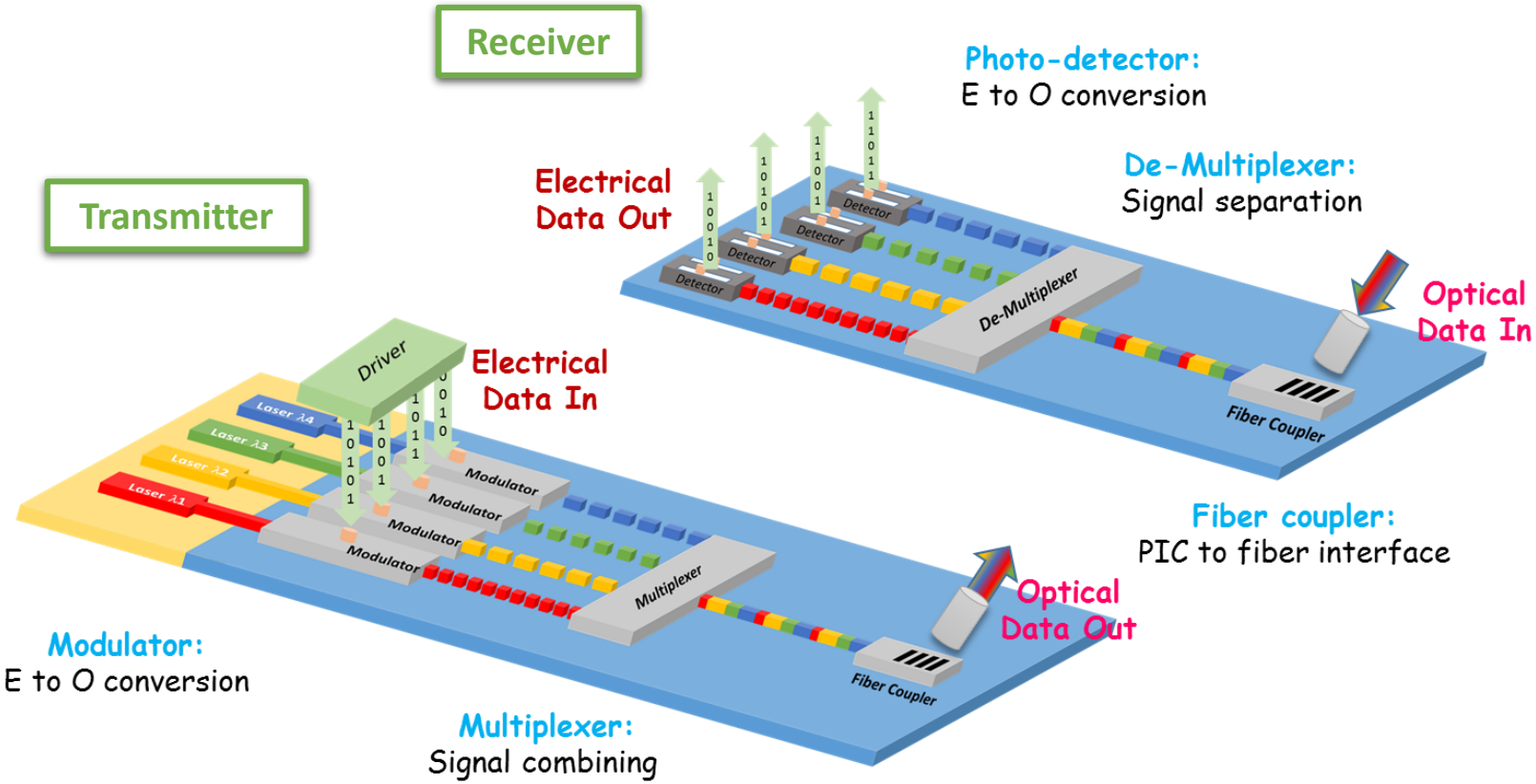
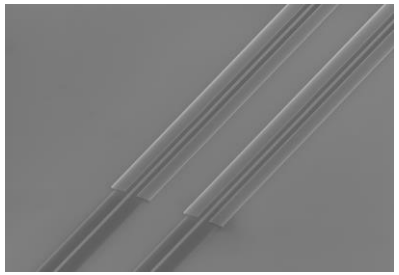
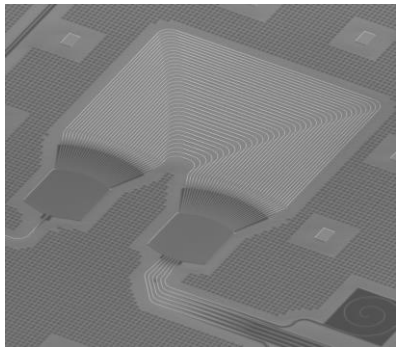
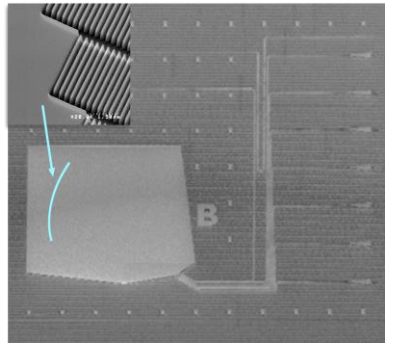
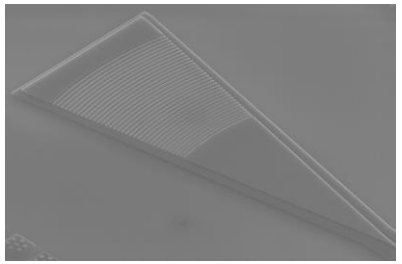
Silicon Photonic Links

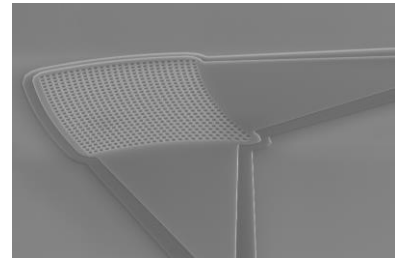


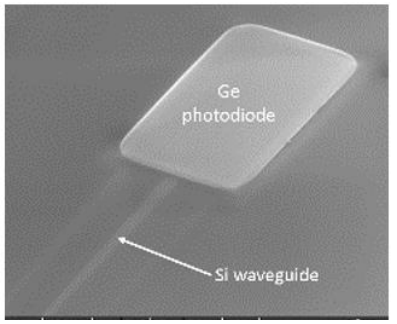






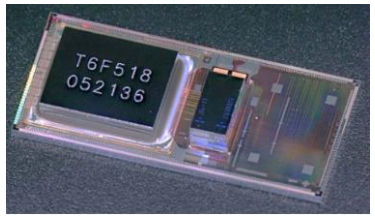






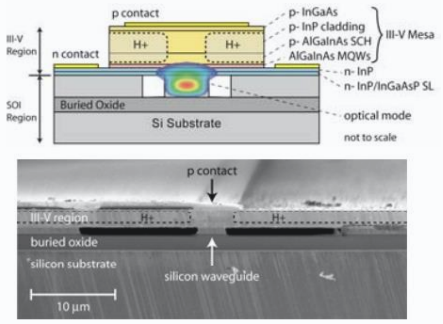
Which light source on silicon ?

Assembly of already processed III-V laser



Luxtera's
silicon photonics Optical Engine
(100G TX+RX PSM-4)

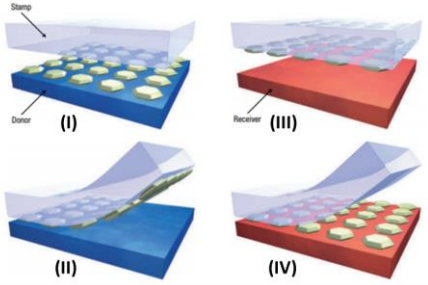
III-V/Si Bonding



J.E. Bowers, et al., *Hybrid Silicon Evanescent Laser in a Silicon-onInsulator Waveguide, OFC (2007)*

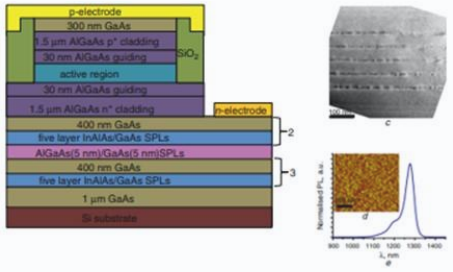
This work

Transfer printing



M. A. Meitl, et al, *Transfer printing by kinetic control of adhesion to an elastomeric stamp, Nature Materials **5**, 33–38 (2006)*

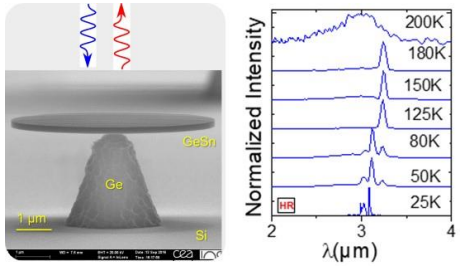
Direct epitaxy of III-V on Si



S.M. Chen, et al, *1.3 µm InAs/GaAs quantum-dot laser monolithically grown on Si substrates operating over 100°C, Electronics letters,* Vol. 50 No. 20 pp. 1467–1468 (2014)

Next talk

Ge(Sn) laser on Si



V. Reboud et al., *Optically pumped GeSn micro-disks with 16% Sn lasing at 3.1 µm up to 180 K, Appl. Phys. Lett. 111, 092101 (2017).*

Direct Bonding vs. Adhesive Bonding

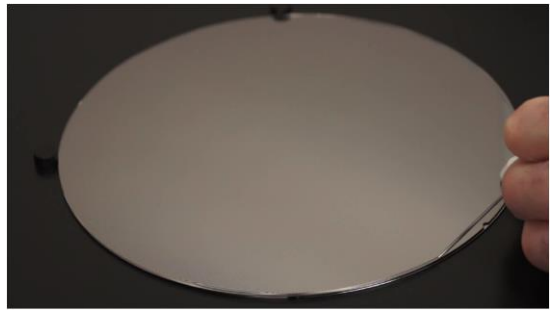
Direct Bonding

- Fast bonding
- Electrical / optical transparency
- No bonding material (degradation, thickness issue)
- Compatible with CMOS BEOL thermal budget
- Surface roughness and cleanness

Direct bonding : **spontaneous** bonding without “thick” liquid material.

Based on:

- intermolecular interactions including Van der Waals forces,
- hydrogen bonds
- strong covalent bonds



Wafer bonding for silicon-on-insulator technologies

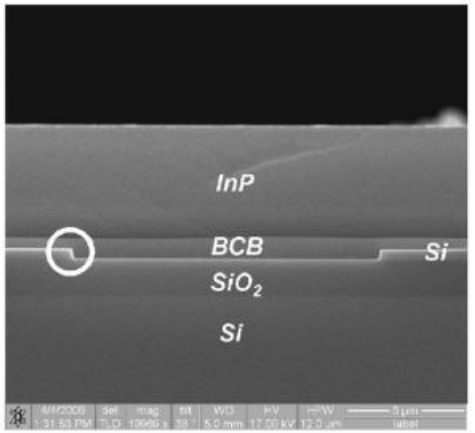
Cite as: Appl. Phys. Lett. **48**, 78 (1986); https://doi.org/10.1063/1.
Submitted: 27 August 1985 . Accepted: 23 Octob

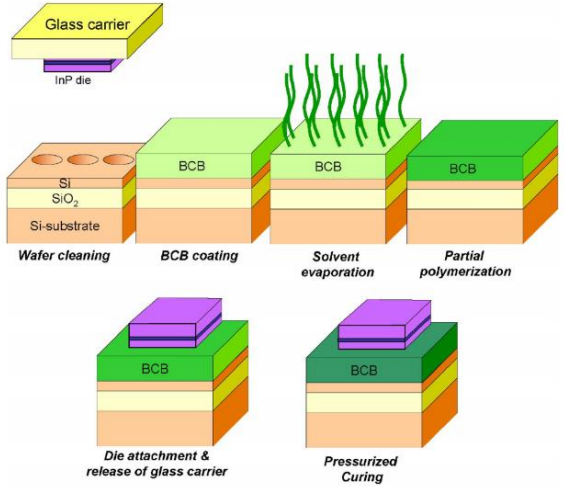
J. B. Lasky

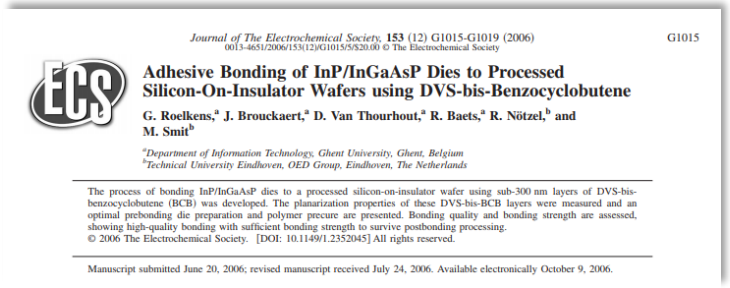
First reports of successful silicon direct bonding

Adhesive Bonding

- Surface roughness and cleanness relaxed requirements
- Post BCB deposition thermal budget < 400°C
- BCB thickness control
- Standard CMOS fab compatibility







Journal of The Electrochemical Society, **153** (12) G1015-G1019 (2006) G1015
0013-4651/2006/153(12)/G1015/5/$20.00 © The Electrochemical Society

Adhesive Bonding of InP/InGaAsP Dies to Processed Silicon-On-Insulator Wafers using DVS-bis-Benzocyclobutene

G. Roelkens,[a] J. Brouckaert,[a] D. Van Thourhout,[a] R. Baets,[a] R. Nötzel,[b] and M. Smit[b]

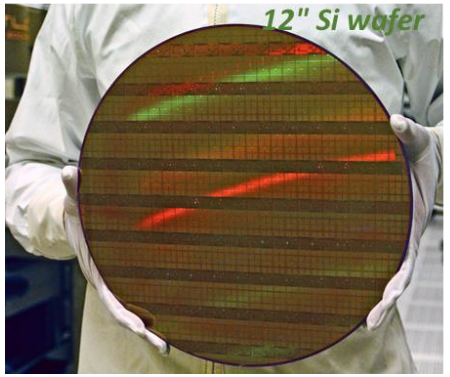
[a]*Department of Information Technology, Ghent University, Ghent, Belgium*
[b]*Technical University Eindhoven, OED Group, Eindhoven, The Netherlands*

The process of bonding InP/InGaAsP dies to a processed silicon-on-insulator wafer using sub-300 nm layers of DVS-bis-benzocyclobutene (BCB) was developed. The planarization properties of these DVS-bis-BCB layers were measured and an optimal prebonding die preparation and polymer precure are presented. Bonding quality and bonding strength are assessed, showing high-quality bonding with sufficient bonding strength to survive postbonding processing.
© 2006 The Electrochemical Society. [DOI: 10.1149/1.2352045] All rights reserved.

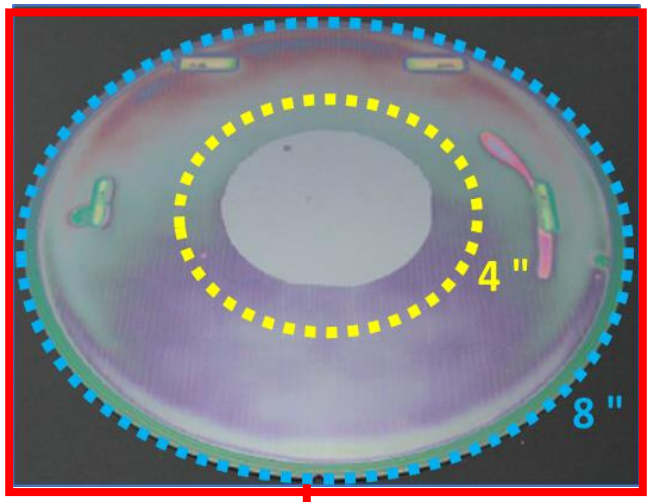
Manuscript submitted June 20, 2006; revised manuscript received July 24, 2006. Available electronically October 9, 2006.

Laser on Si large scale integration: Die Bonding

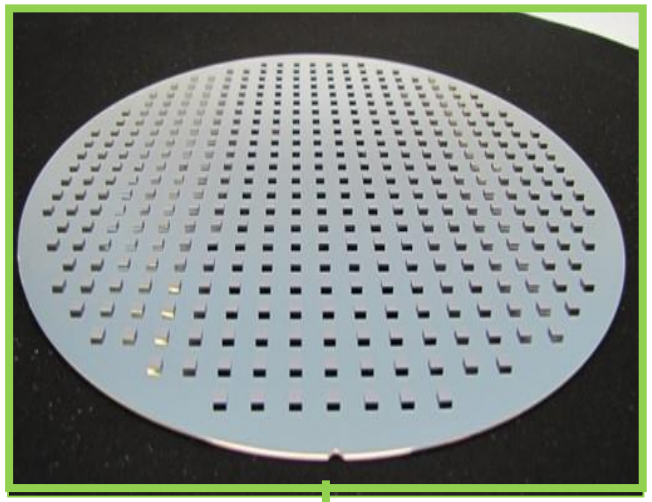
InP based photonics



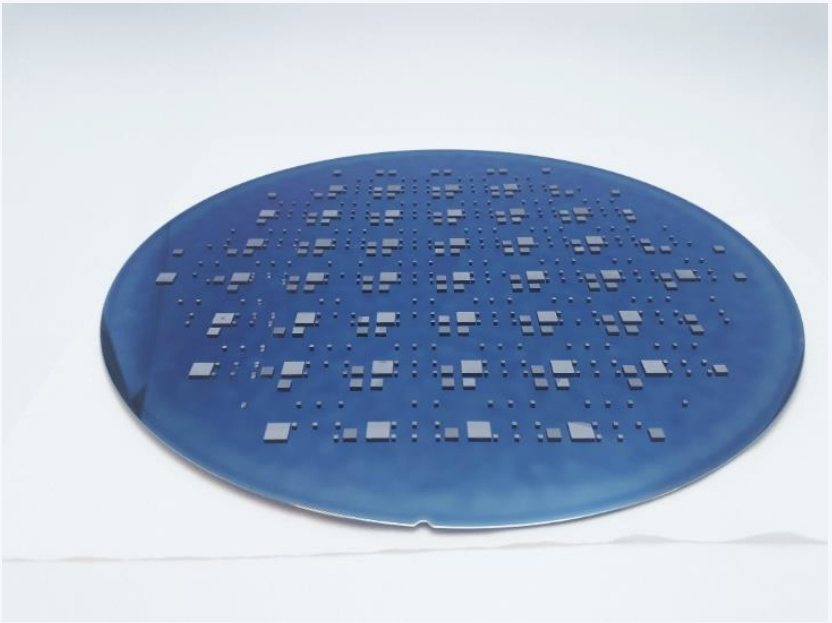
Silicon photonics



Cost advantage of silicon photonics based the use of *CMOS* platforms and large wafer format is no more valid



- Die bonding to cover the full Si wafer
- Localize the III-V material only where it is needed

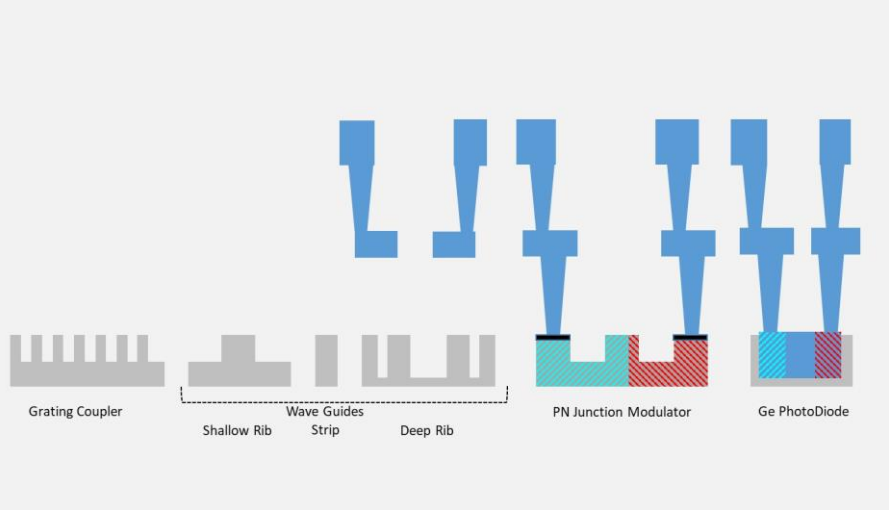


Collective die Bonding with adhesive film

- \+ Process validated for InP die
- \+ Process compatible with die thickness variations up to 50 µm
- \+ Compatible with multidie bonding
- \+ Minimum Die Size 1x1mm²
- \+ Die spacing 400µm
- \+ Scalable to 300mm wafers

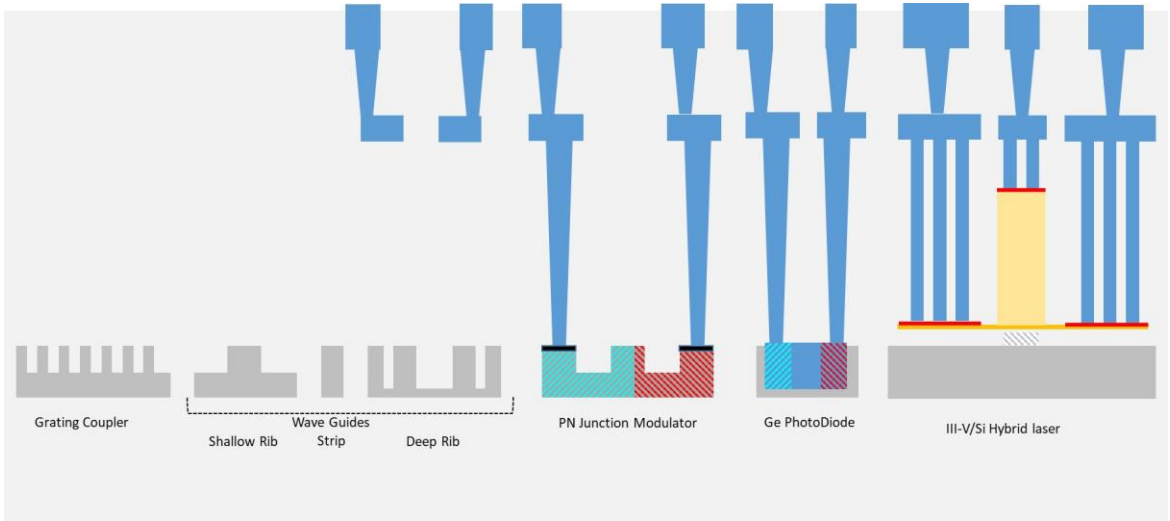
Technology– Laser integration impact

Si Photonic Plateform Core Process



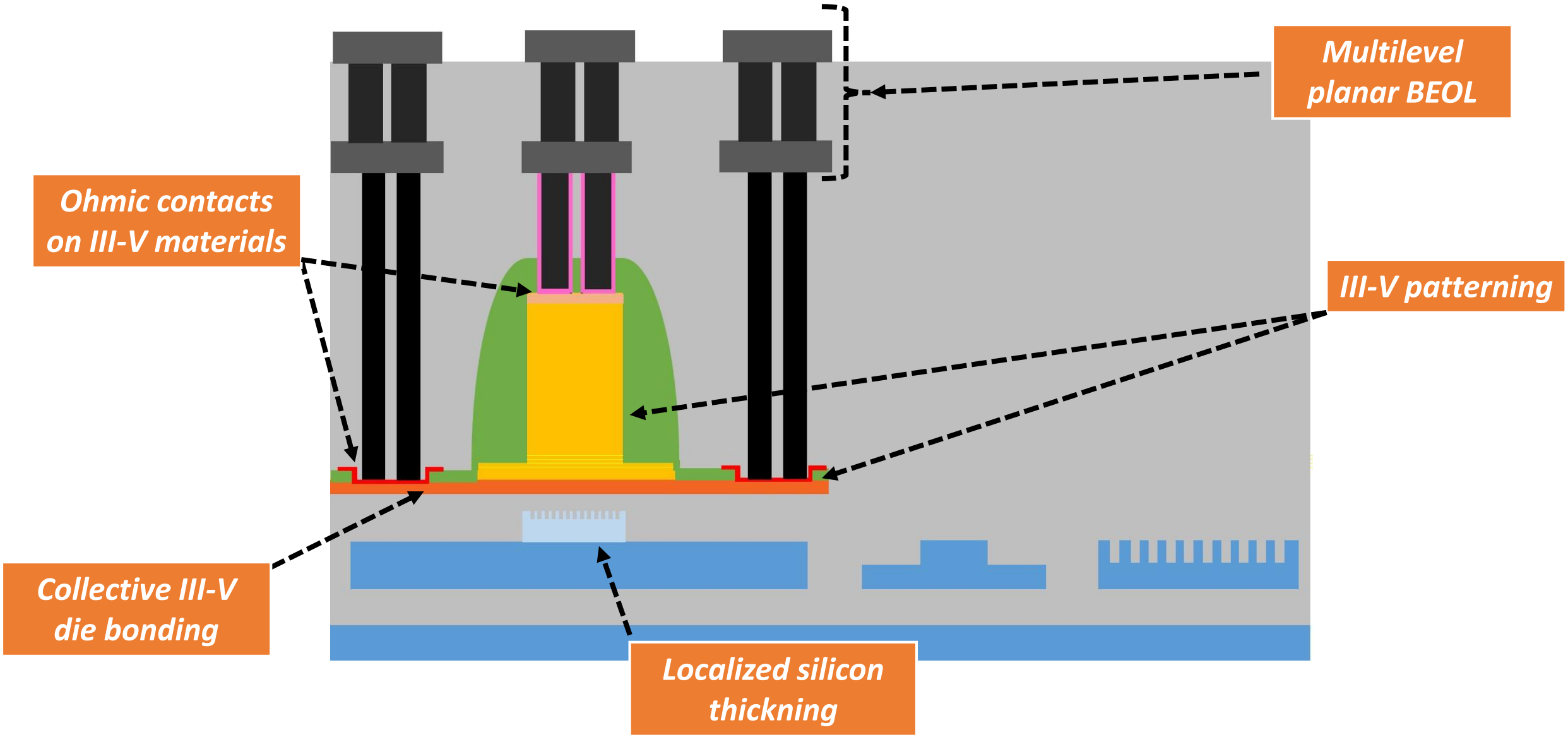
- 310nm SOI – 2µm BOX
- 193nm DUV lithography
- Multilevel silicon patterning
- 8 Implantations levels
- Selective Germanium epitaxy
- Silicide
- Metal heater
- Planarized BEOL
- 2 AlCu routing levels
- UBM for Cu pillar assembly

CMOS Compatible III-V/Si Integrated Laser



- Collective die bonding
- Additional Laser process steps cmos compatible:
  - No noble metals for III-V contacts
  - Conventional patterning steps (no lift-off)
- Thick M1 to Silicium contact module
- Localized Si thickening on 310nm SOI:
  - Damascene process with Si-Amo or selective Si-epi
- Planarized multi-metal level BEOL
- Additional thermal budget due to laser integration < 600°C

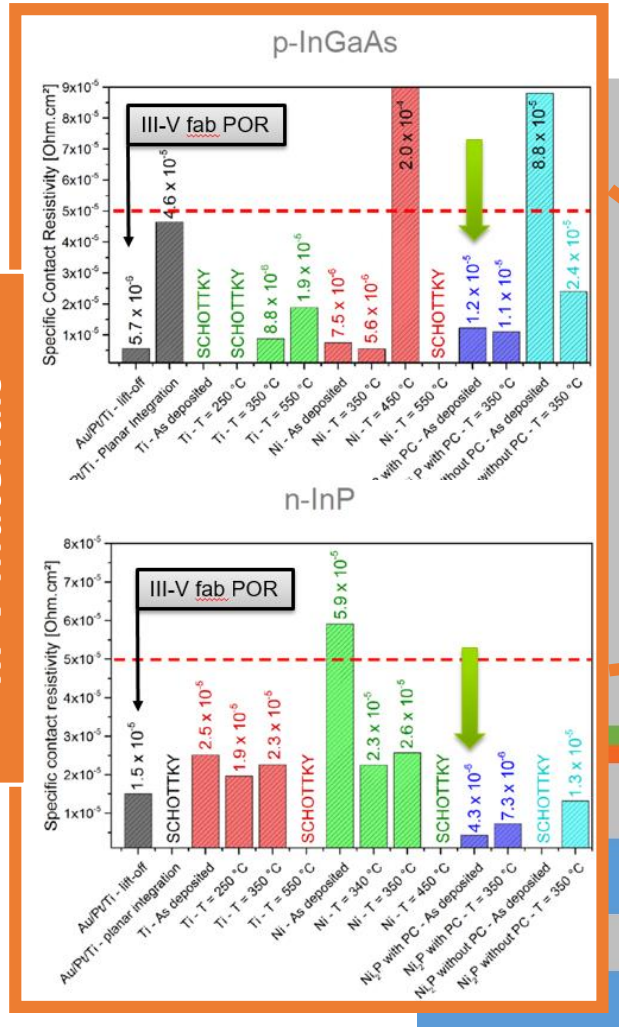
Large scale integration CMOS friendly process



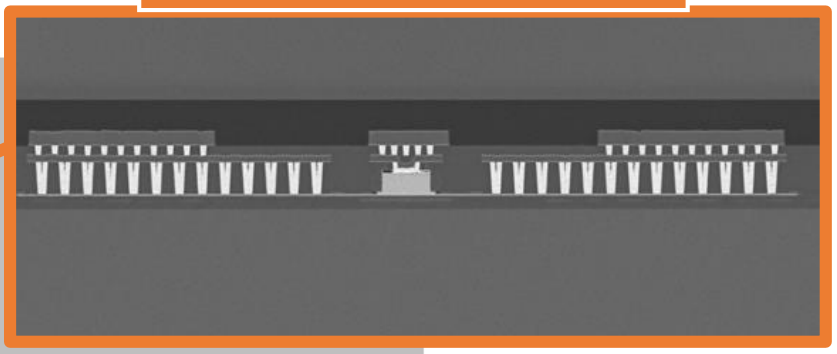
B. Szelag et al., IEDM 2017

Large scale integration CMOS friendly process

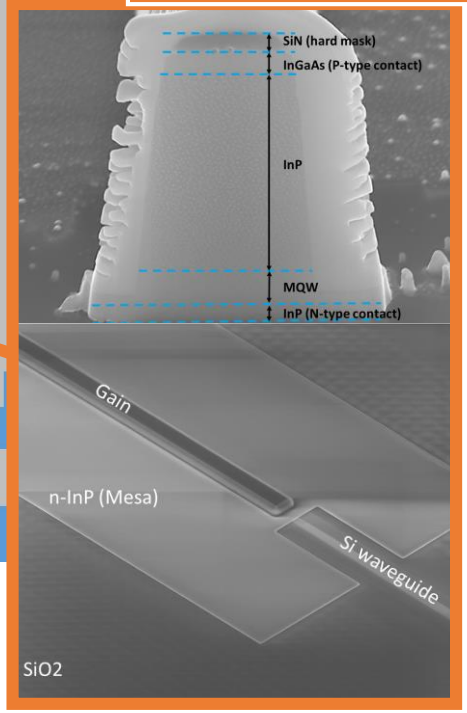
Ohmic contacts on III-V materials

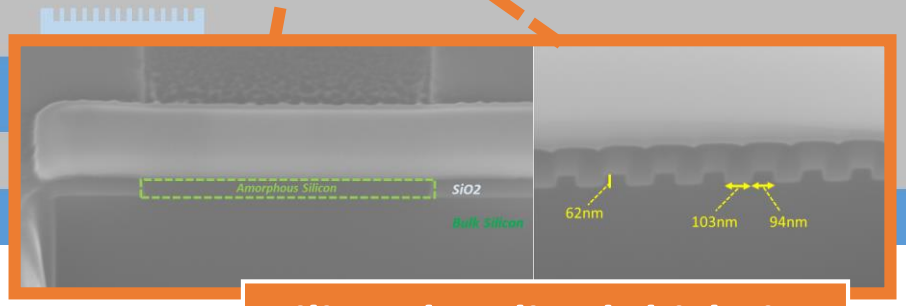


Multilevel planar BEOL



III-V patterning

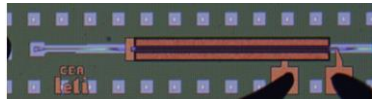


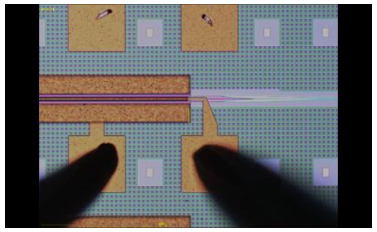


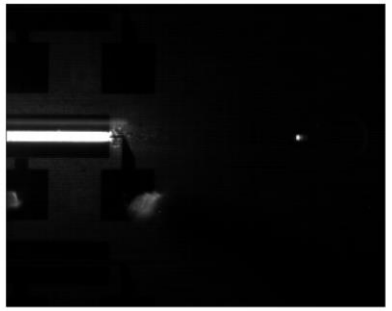
Silicon localized thickning

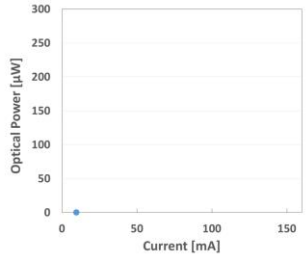
Optical characterization

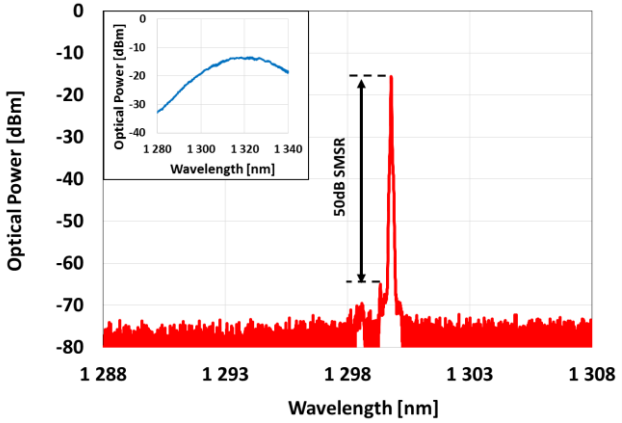
First generation with one metal level – DFB laser example

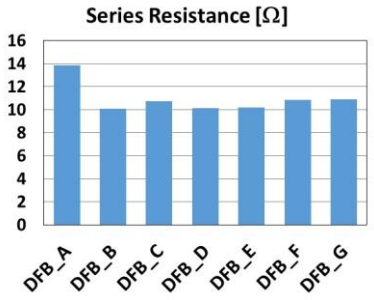


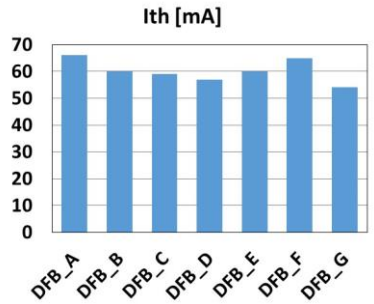




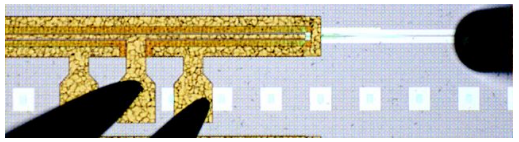


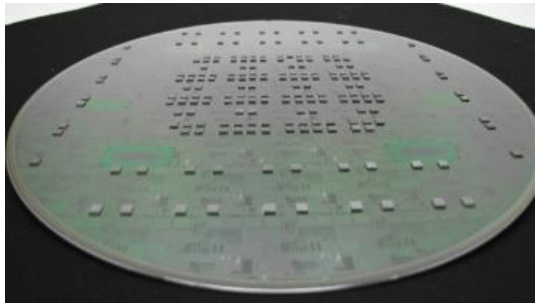


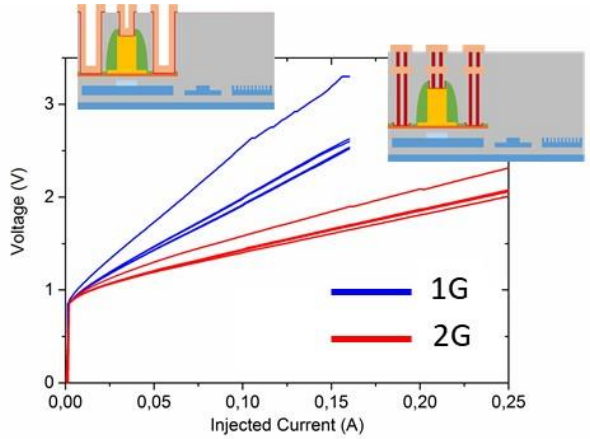


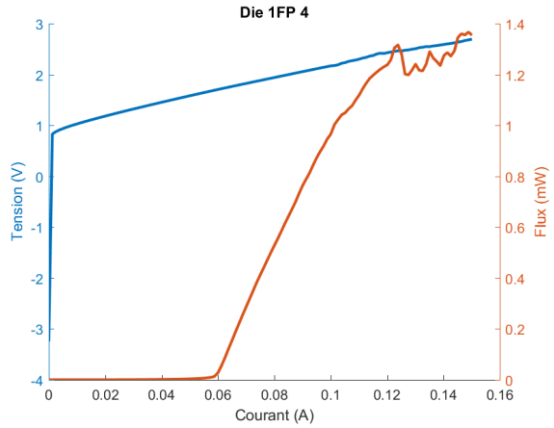


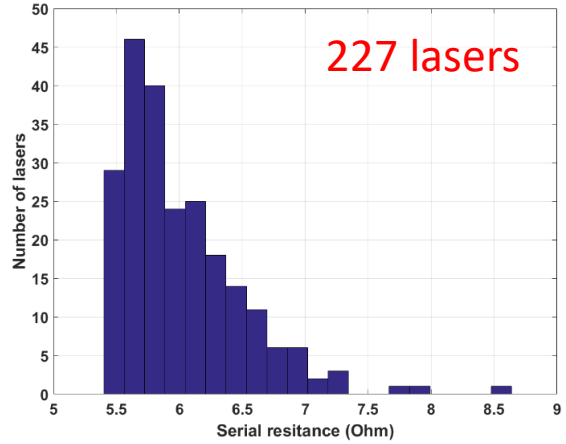
Second generation with two metal levels – FP laser example



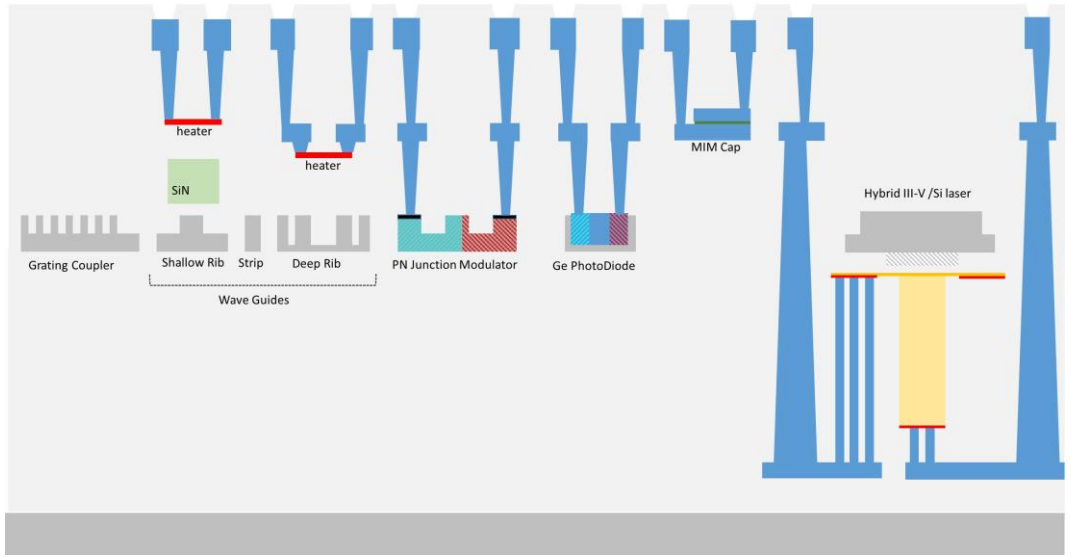






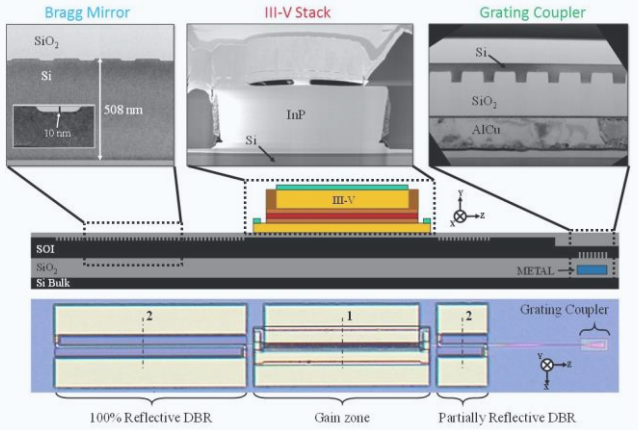


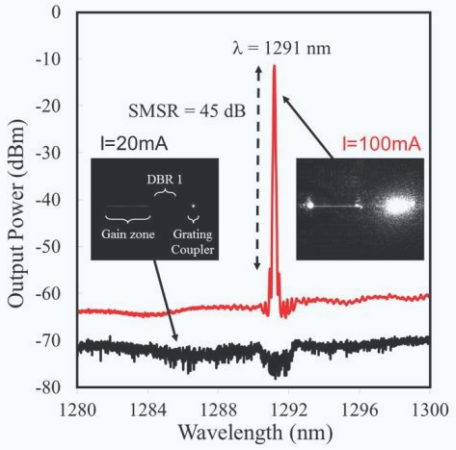
Hybrid laser back side integration concept

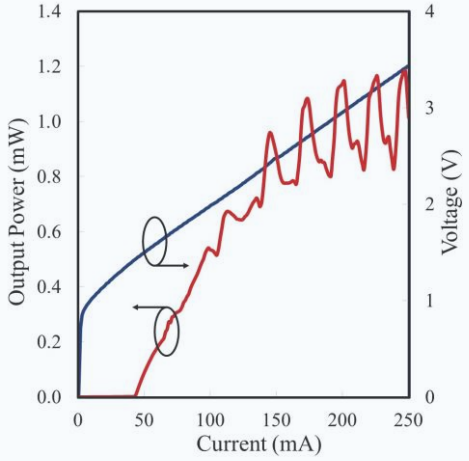


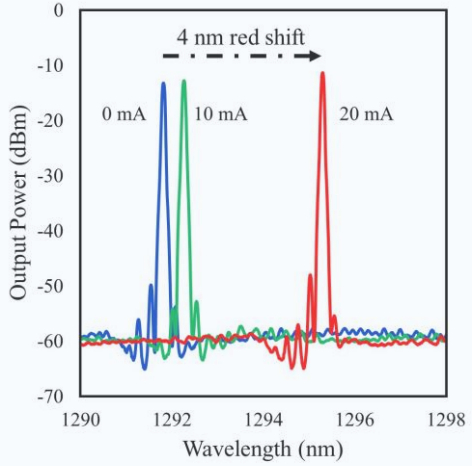
- Integration scheme compatible with any photonic platform
- No impact on the Silicon photonic platform
- Modular integration
- Si photonic platform and laser integration can be done in 2 different fabs
- Only way to have '3D photonic' (SiN or Si level on top of SOI) and laser on the same die
- EIC and Laser @ opposite sides of the PIC

- Demo: Passive + BSI DBR laser done with 100mm process (J. Durel et Al, IEDM 2016)









Conclusion

- The monolithic integration of a fully CMOS compatible hybrid laser on a 200/300mm silicon photonics platform requires new process module developments.

- CEA-LETI have developed a collective die bonding process with adhesive film:
  - Scalable to 300mm wafer
  - Compatible with multi die bonding

- Specific cmos compatible metallization's can be used for large scale integration of laser in CMOS compatible process.

- III-V/Si hybrid laser integration on qualified silicon photonic platform has been demonstrated using CMOS compatible process with planarized BEOL.

- Back side integration is a way to integrate laser without any impact on base line silicon photonic platform.

Acknowledgments

Silicon Photonic Lab members

L. Adelmini
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L. Baud
T. Bria
K. Hassan

LETI's Silicon (and more) technological platform members

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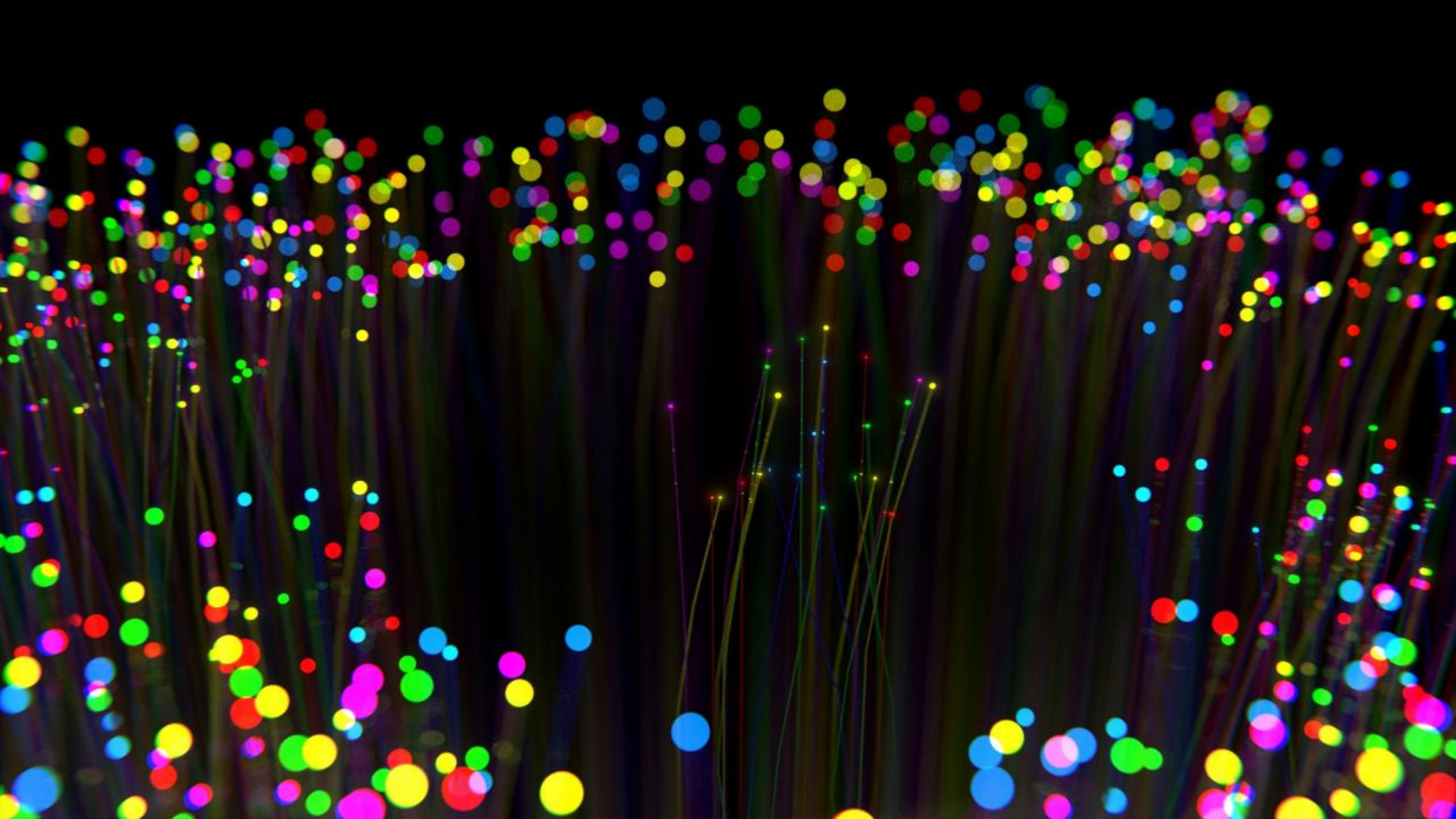
A. Schembri
MC. Roure
C. Jany
B. Montmayeul
L. Sanchez
Ph. Rodriguez
O. Pesenti
R. Crochemore,
S. Dominguez



Thank you for attention

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Last update in

Photonics technology towards edge performance sensors

Live webinar July 6th 2020

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