Last update in

Photonics technology towards edge performance sensors

NANOELEC.

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On Monday, July 6th 2020, 5pm CET

Last update in
Photonics technology towards edge performance sensors
Live webinar July 6th 2020

Ultra-low loss silicon waveguides in a mature photonics technology

Erwine Pargon [1] and Quentin Wilmart [2]

[1] Univ. Grenoble Alpes, CNRS, CEA/LETI-Minatec, Grenoble INP, LTM, Grenoble-France
[2] Univ. Grenoble Alpes, CEA-Leti, Grenoble, France

Outline

I. Hydrogen annealing treatment: a way to minimize scattering loss

By Erwine Pargon (CNRS-LTM)

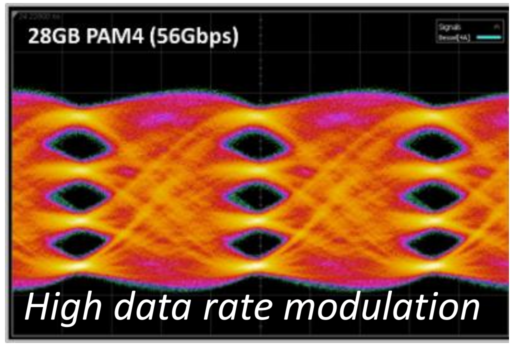
II. Hydrogen annealing treatment: a way to boost Si photonic platform performance

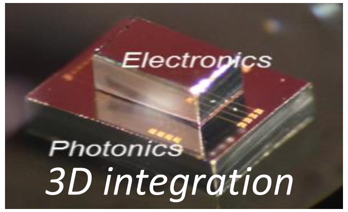
By Quentin Wilmart (CEA-Leti)

Silicon photonics applications at Leti

High-speed interconnects for optical communications

- Telecom
- Datacom (datacenters)
- Computercom (on-chip communications between processors)

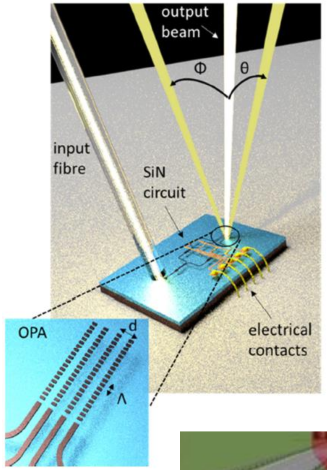




Szelag et al., SSDM, 2018

3D sensing

- Solid state beam steering: optical phase array for LIDAR.
  (using SiN waveguides)

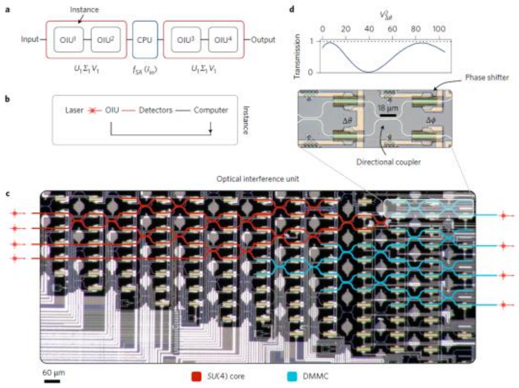


N. A. Tyler et al. Optics Express, Feb. 2019

Neuromorphic photonics

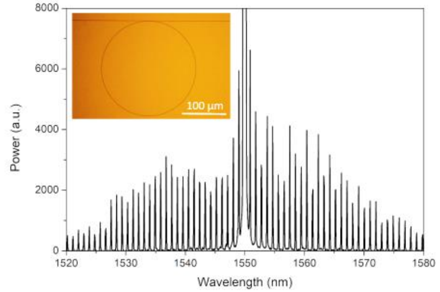
- Neuromorphic computing
- Artificial intelligence

Linear operation (matrix multiplication) with large Mach Zehnder arrays

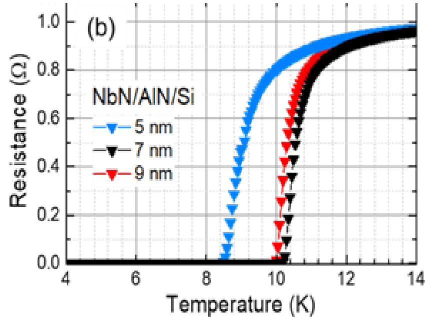


Quantum photonics

- Secure communications
- Q computing



Demonstration of photon entanglement



NbN based superconducting single photon detector

F.A. Sabattoli et al. ICTON 2019

Silicon waveguides

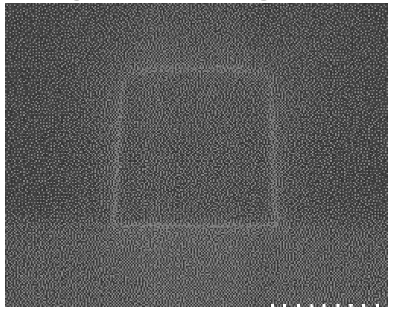
- Silicon wire waveguides based on silicon-on-insulator (SOI) structures are key for highly integrated, ultra small optical devices

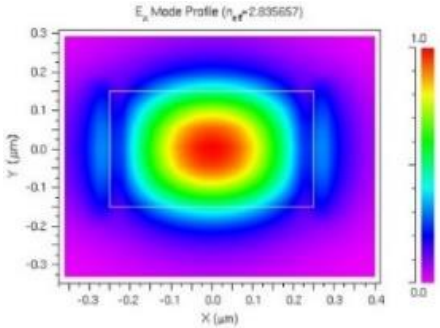
- High index contrats SiO_2/Si:

→ Tight confinement of light
→ Small waveguide
→ Tight bends
→ Dense integration of components on a chip

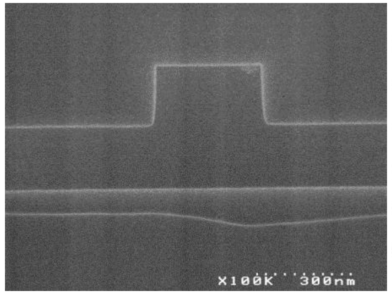
- **But Scattering losses** dominate and compromise the Si platform performance

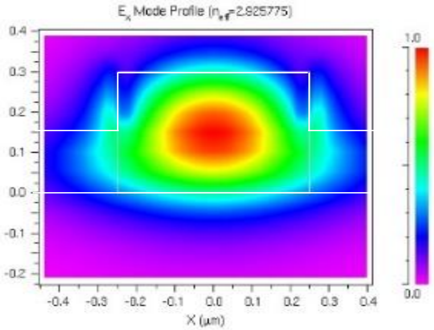
STRIP WG



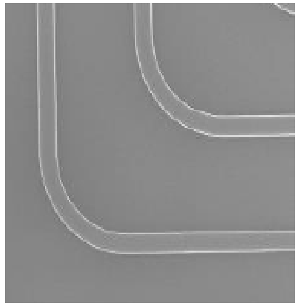


RIB WG

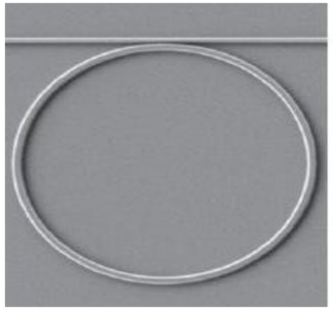




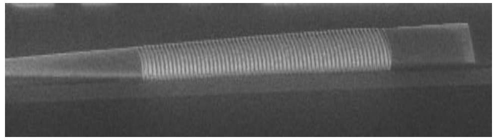
Bend



Ring resonator



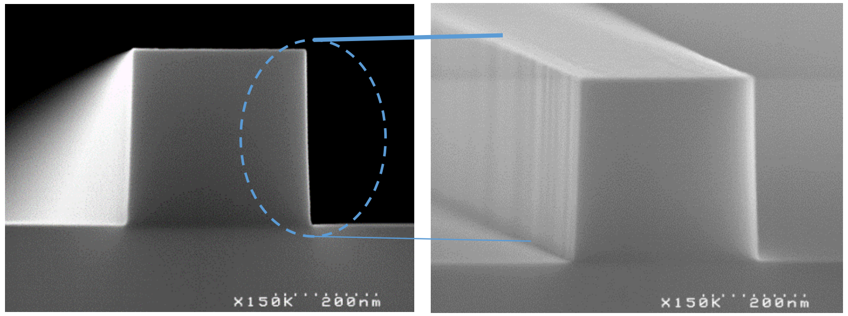
Grating coupler



How to decrease Si WG scattering loss?

- Scattering losses are mainly due to the **sidewalls surface roughness** of Si WG after plasma patterning

Silicon waveguide after plasma etching



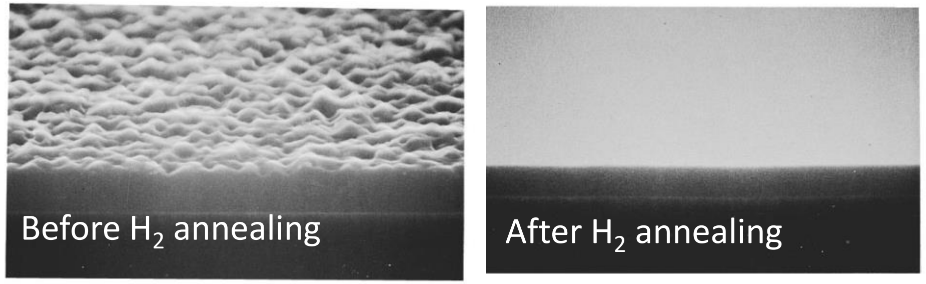
- ✓ Si Line Edge Roughness (LER) **=2,5 nm (**RMS=0.8nm) (with 248nm lithography)
- ✓ **How to improve starting from this?**

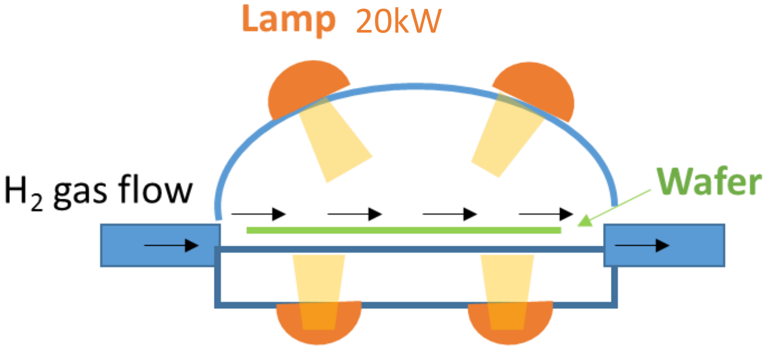
- How about H_2 annealing treatment after Si waveguide patterning?

H_2 annealing leads to Si atomic surface migration

N. Sato, Appl. Phys. Lett. 65, 1924 (1994)

1150°C-80 Torr





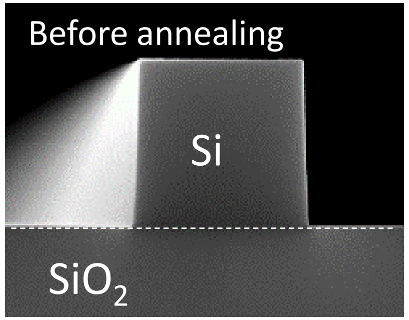
Epitaxy chamber -Epi centura

Process parameters:
- ✓ Temperature (300-1100°C)
- ✓ Pressure (0.5-600Torr)
- ✓ Time

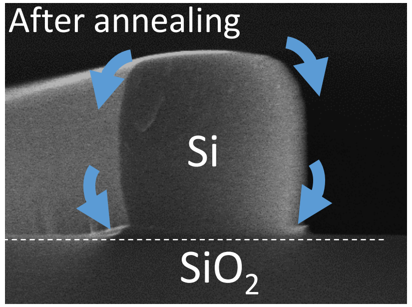
H_2 annealing impact for Strip waveguides

Profile

350*350nm



H_2 annealing
850°C/20Torr/1min

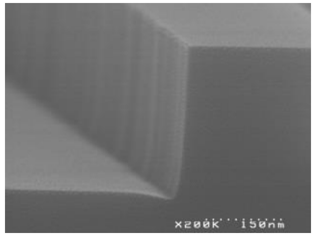


→ Si reflow: Rounded and swelled profile
→ But width preserved

Roughness

AFM on sidewalls

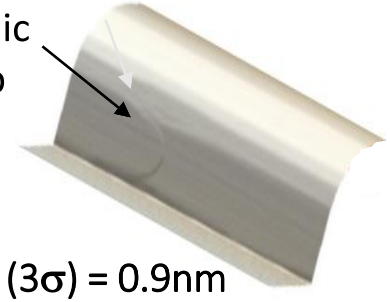
Before annealing



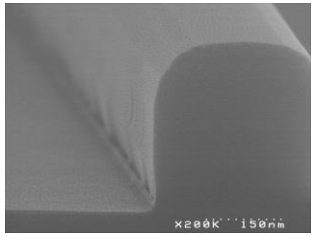
LER (3σ) = 2.5 nm
RMS (σ)= 0.83 nm

64 % LER decrease

Atomic step



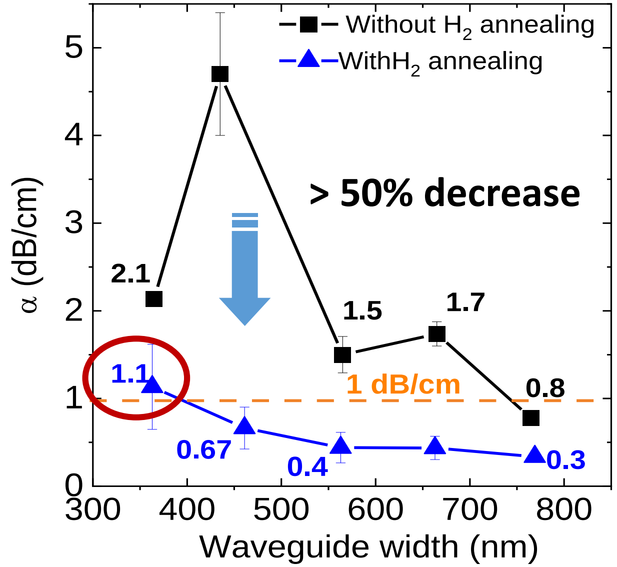
After annealing



LER (3σ) = 0.9nm
RMS (σ)=0.3nm

→ Atomic scale smoothening

Optical Losses @ 1310nm



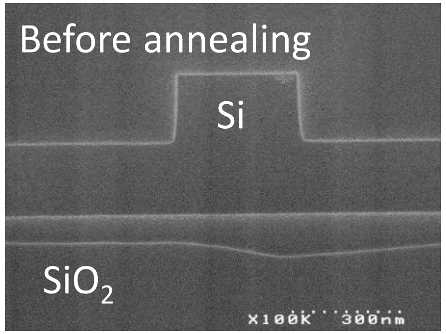
→ Significant optical loss reduction for all waveguide CDs
→ **Record loss@1310nm for 350*350 WG=1.1dB/cm**

C. Bellegarde et al., *IEEE Phot. Technol. Lett.*, 2018

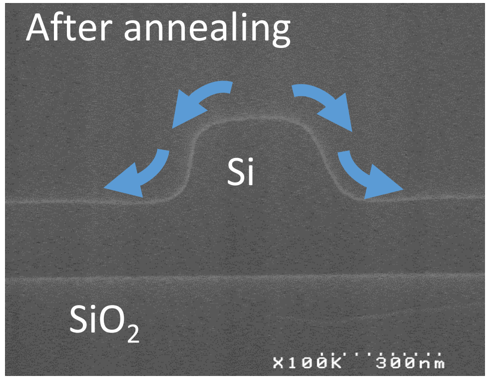
H_2 annealing impact for RIB waveguides

Profile

350*150nm



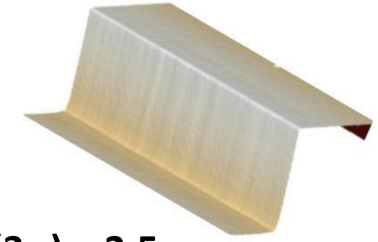
H_2 annealing
850°C/20Torr/1min



→ Significant profile deformation
→ No SiO_2 interface at the bottom to limit the reflow

Roughness

Before annealing



LER (3σ) = 2.5 nm
RMS (σ)= 0.83 nm

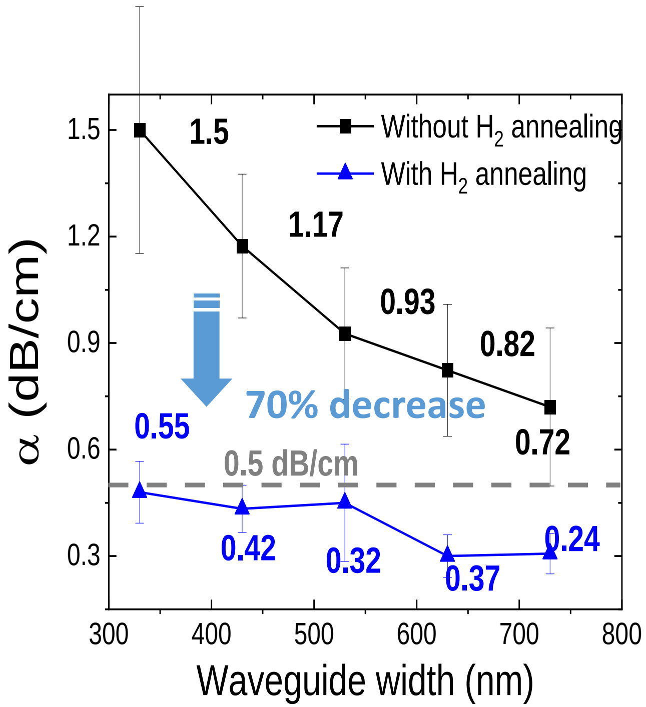
- 70%

After annealing

LER (3σ) = 0.7 nm
RMS (σ)=0.23nm

→More significant roughness decrease compared to STRIP

Optical Losses @ 1310nm

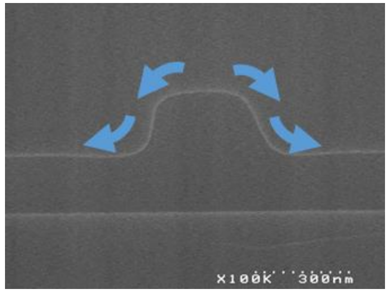


→ Significant optical loss reduction for all waveguide CDs
→ **But the profile deformation and CD increase could be detrimental to other optical passive devices**

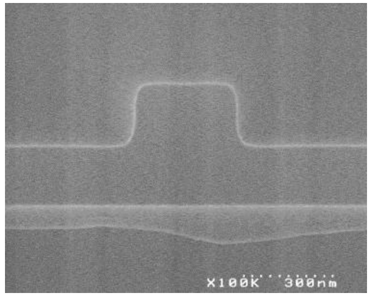
H_2 annealing optimization for RIB

Decrease Temperature
T<850°C

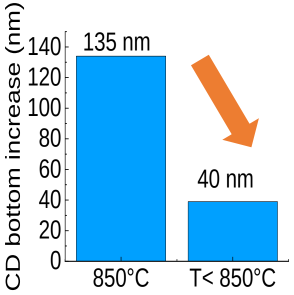
850°C/20Torr/1min
350*150nm

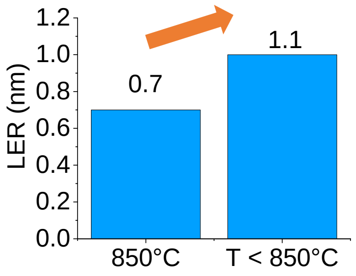


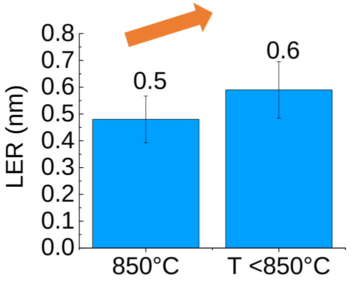
1



- ✓ Better CD control
- ✓ Higher roughness
- ✓ Slight loss increase





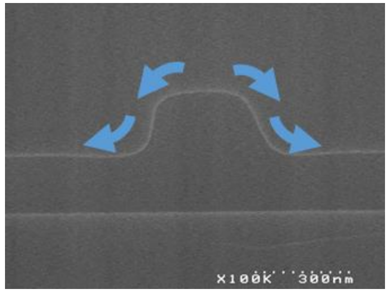


Lower temperature offers a good compromise between profile deformation and loss improvement in RIB, but losses in STRIP are of 1.8dB/cm

H_2 annealing optimization for RIB

Decrease Temperature T<850°C

850°C/20Torr/1min
350*150nm



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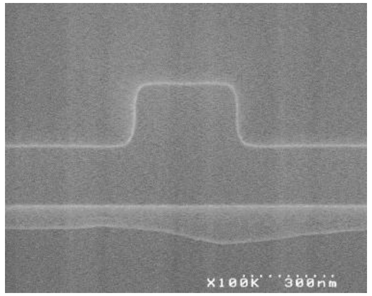
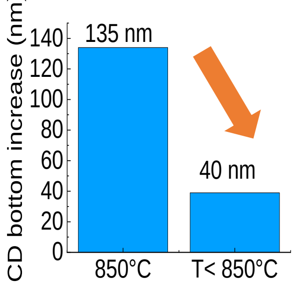
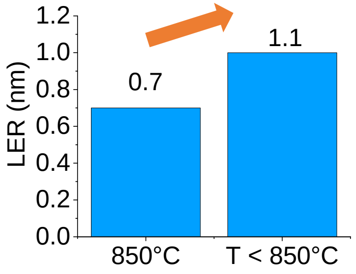


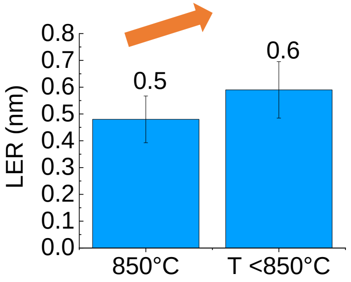
✓ Better CD control



✓ Higher roughness



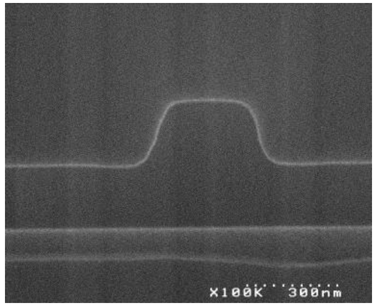
✓ Slight loss increase



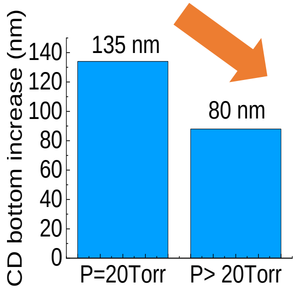
Lower temperature offers a good compromise between profile deformation and loss improvement in RIB, but losses in STRIP are of 1.8dB/cm

2

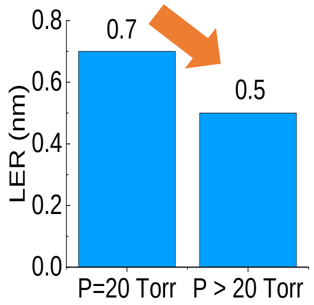
Increase pressure P> 20 Torr



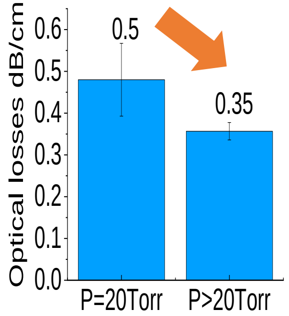
✓ Better CD control



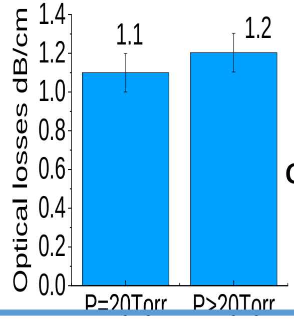
✓ Lower roughness



✓ Lower loss



- ✓ Higher pressure offers the best compromise between RIB profile deformation and optical loss decrease, while maintaining optimal optical losses in STRIP
- ✓ **RIB :α @1310nm= 0.35 dB/cm**
- ✓ **STRIP :α @1310nm= 1.2 dB/cm**



STRIP optical losses

Outline

I. Hydrogen annealing treatment: a way to minimize scattering loss

By Erwine Pargon (CNRS-LTM)

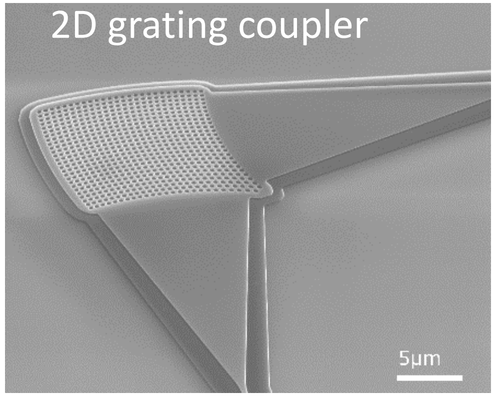
II. Hydrogen annealing treatment: a way to boost Si photonic platform performance

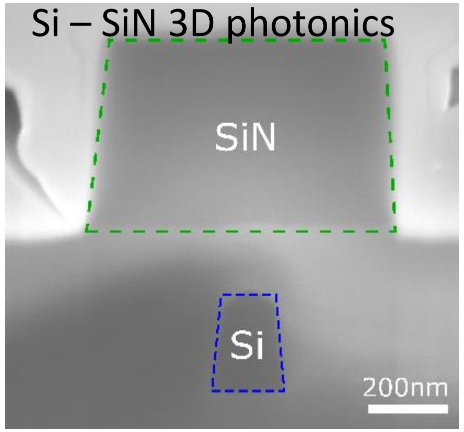
By Quentin Wilmart (CEA-Leti)

LETI's silicon photonics platform

- **200 mm Si photonics platform**
  - Substrates : 8'' SOI 310nm
  - > 200 steps
  - 24 litho levels
  - 40 metro/control steps

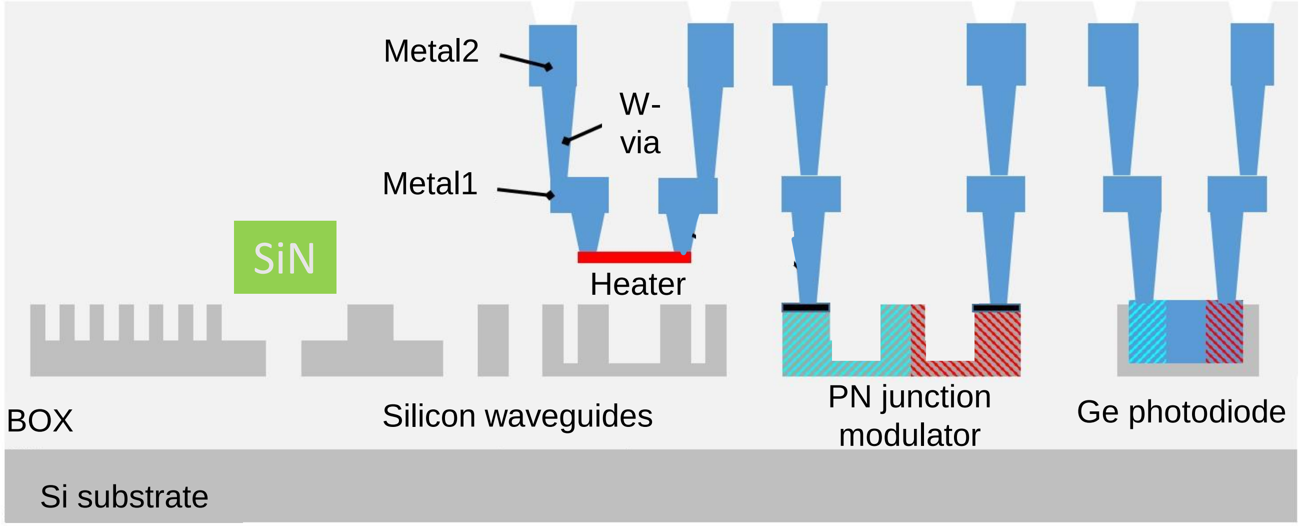
- **Process building blocks**
  - Multilevel silicon patterning
  - PN Silicon junctions
  - Germanium photodetector
  - SiN waveguides
  - Integrated resistance (heater)
  - III-V for integrated hybrid laser
  - Planarized BEOL : 2 AlCu routing levels

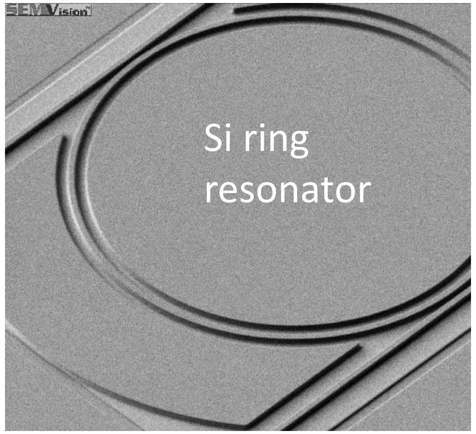


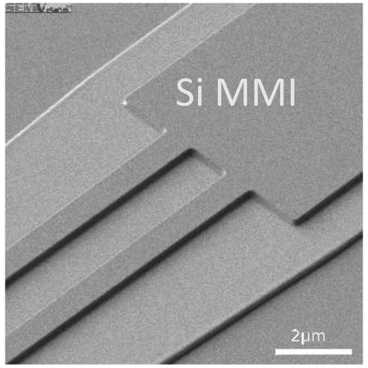


- **Photonic design kit with device library (MPW offer)**

Platform developed for telecom, datacom, sensing and alternative computing



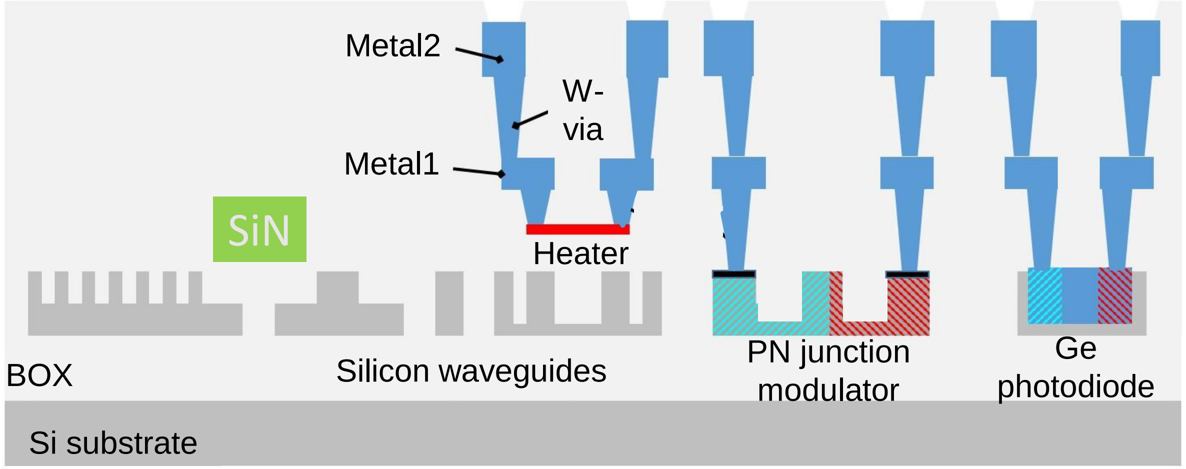




Low loss Si waveguides in the full photonics platform

Hydrogen smoothing annealing applied on the full silicon photonics platform

- Targeting ultra-low loss on 3 types of waveguide (strip, rib and deeprib)
- Si_3N_4 hard mask on top of Si
- Impact on passive components ? (grating couplers, transitions, MMI…)
- Impact on active devices ? (P-N junction for Mach Zehnder modulators - MZM)

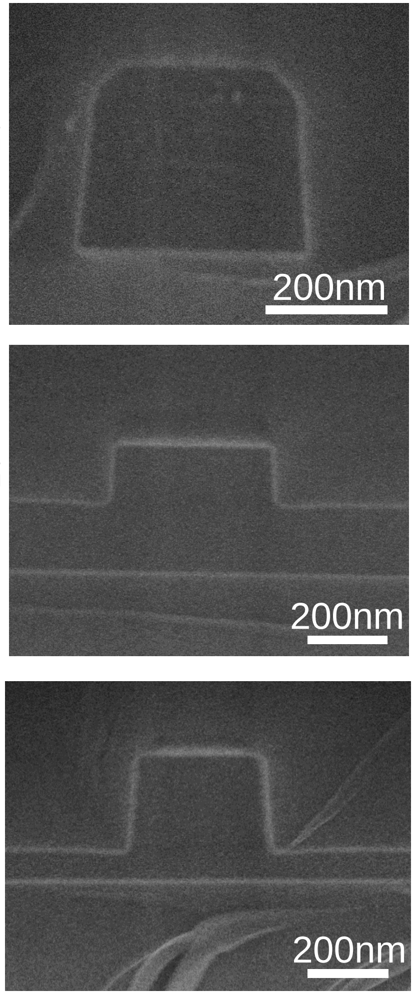


No smoothing

Strip WG

Rib WG

Deeprib
WG
(in MZM)



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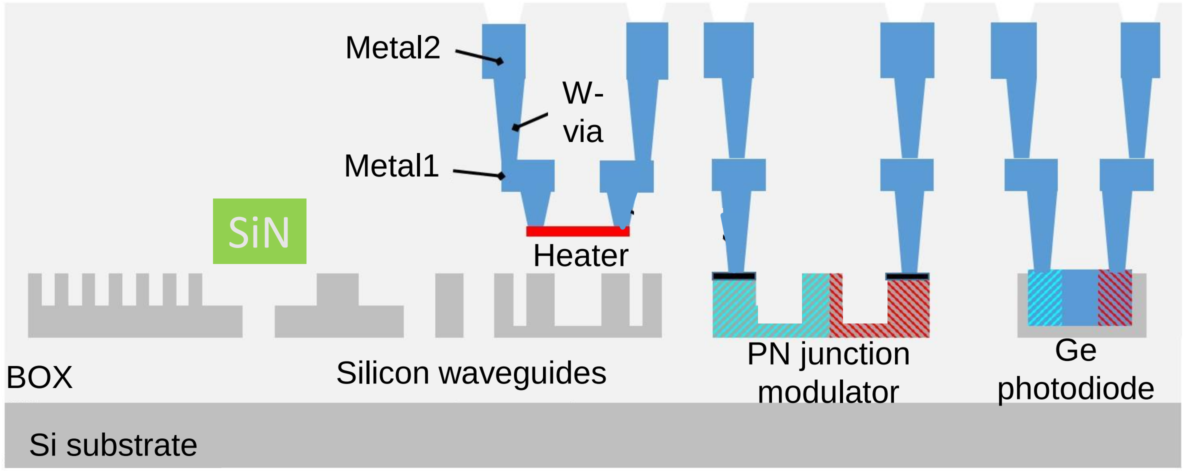
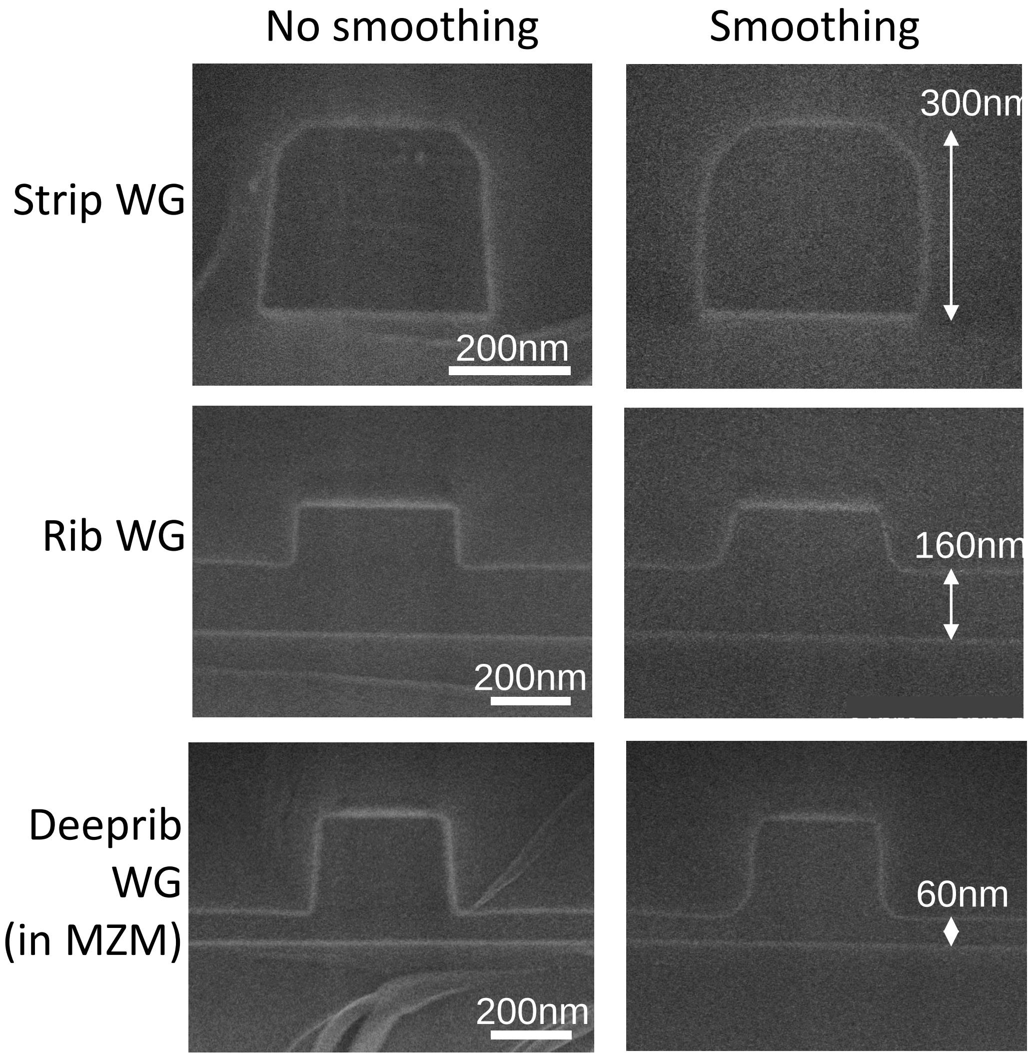
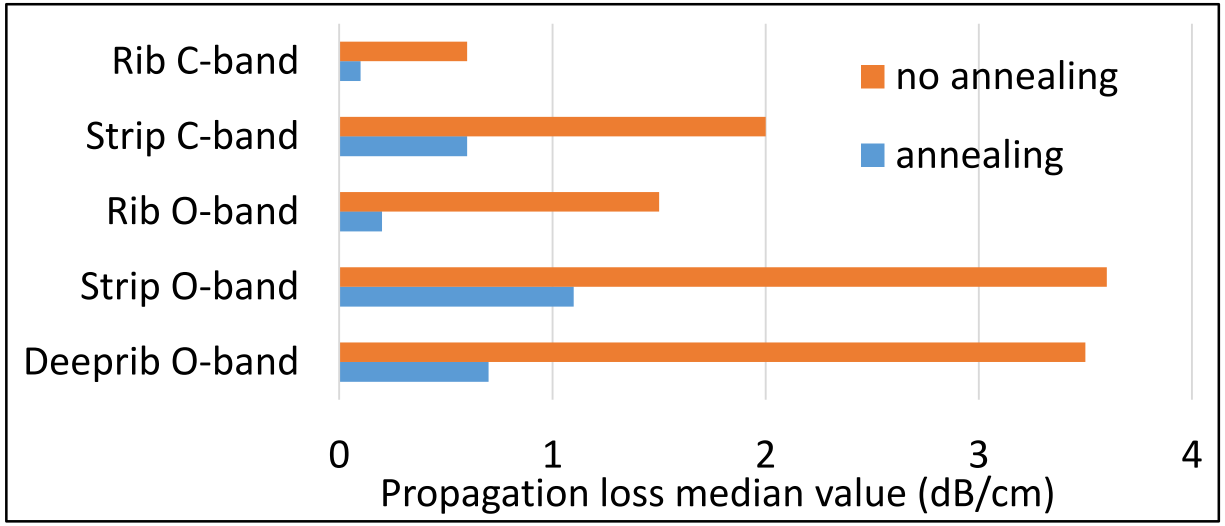




Low loss Si waveguides in the full photonics platform

Photonics technology towards edge performance sensors

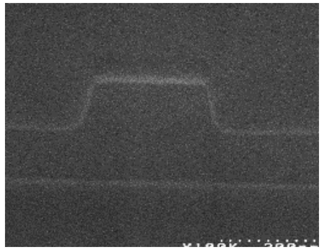
- **Propagation loss measurement**



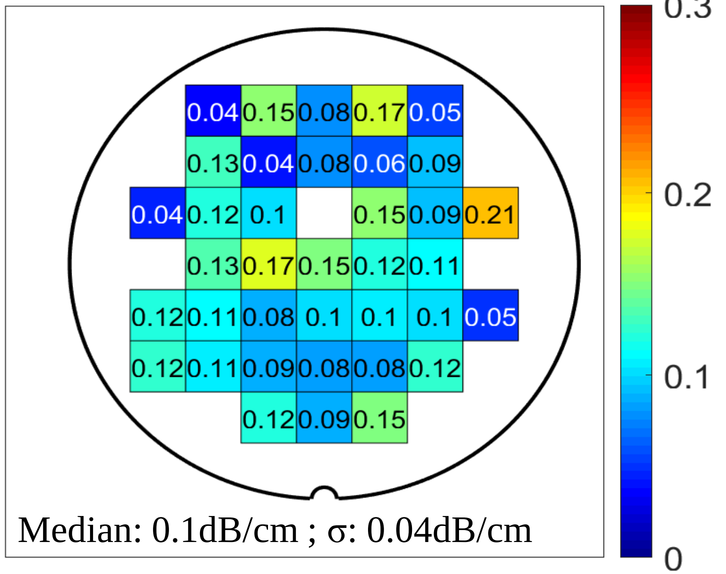
- Efficient sidewall smoothening
- Good wafer uniformity
- Outperform advanced immersion lithography waveguides

0.1dB/cm (rib) ; 1.1dB/cm (strip)
→ State-of-the-art!

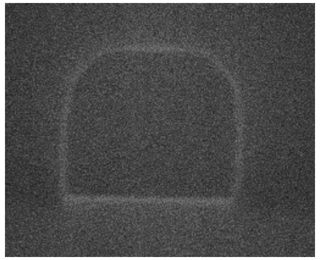
Rib
λ = 1550nm

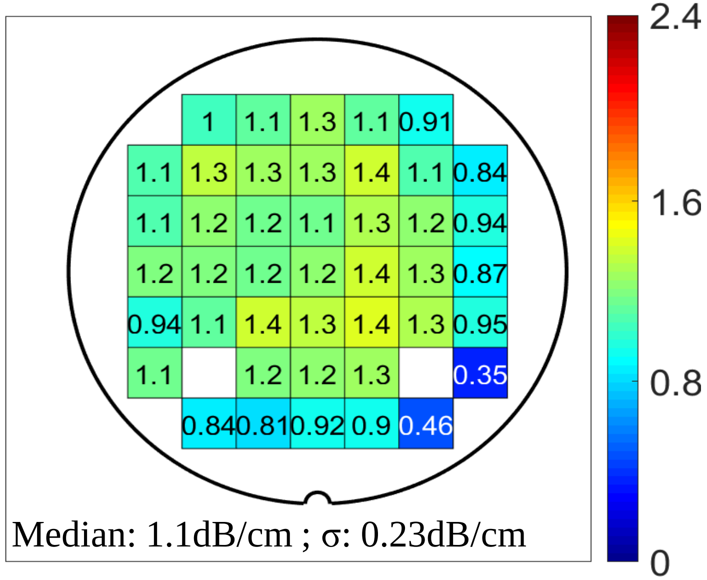


Propagation loss mapping (dB/cm)



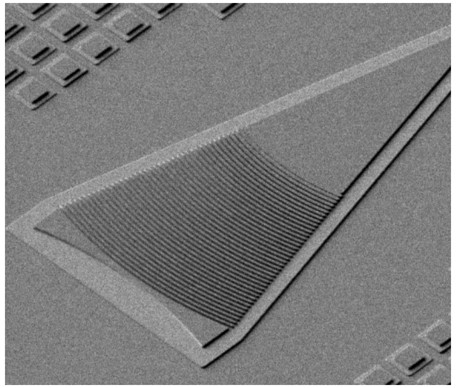
Strip
λ = 1310nm



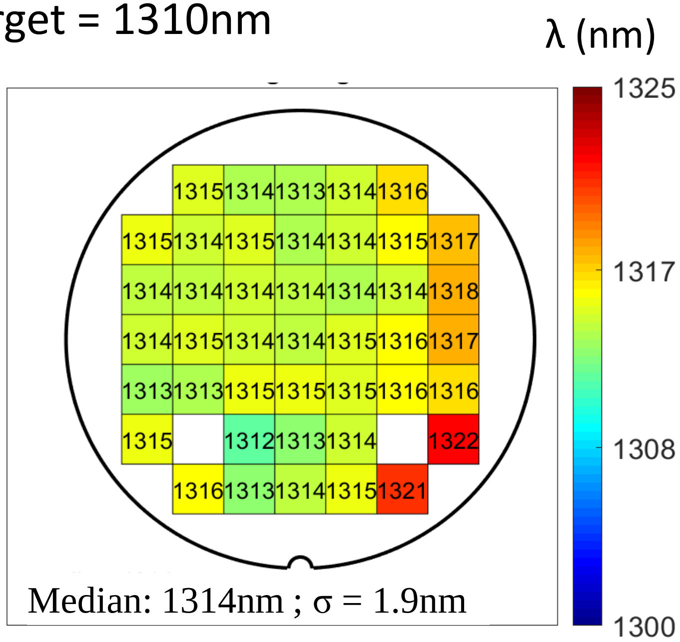


Impact on passive devices

- Grating coupler central wavelength. Target = 1310nm



2-silicon levels apodized grating fiber coupler

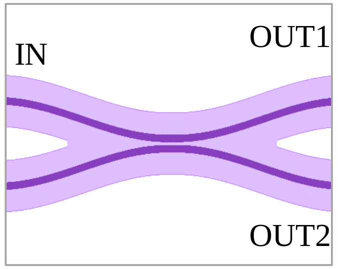


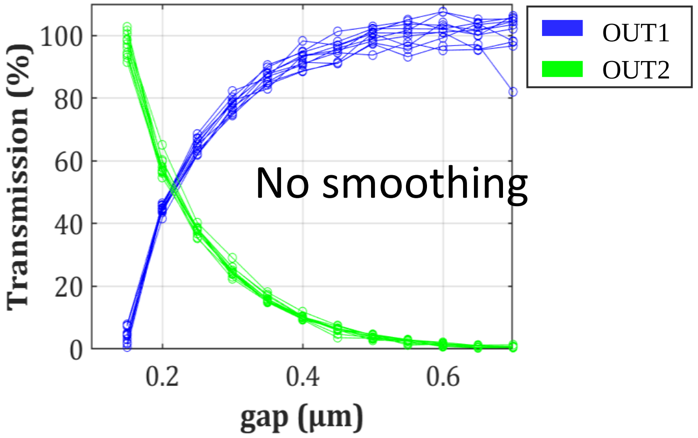
✓ Central wavelength

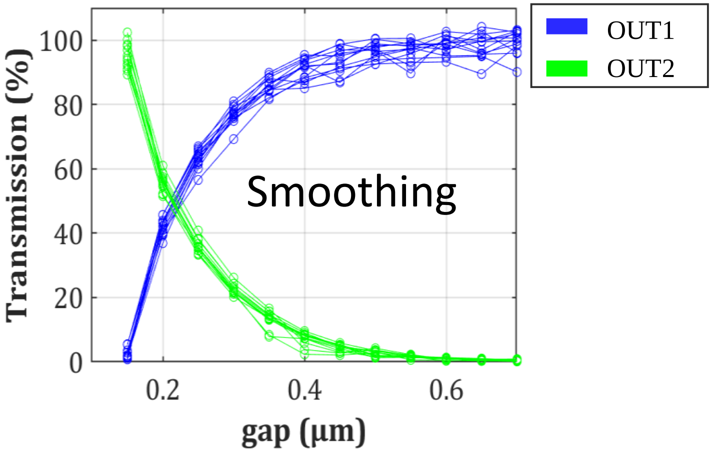
✓ Grating coupler insertion loss = **2dB / grating**

~ no impact of annealing

- Directional coupler transmission @1310nm

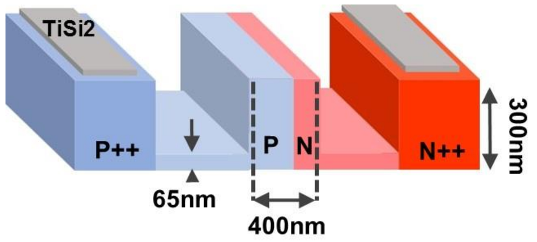


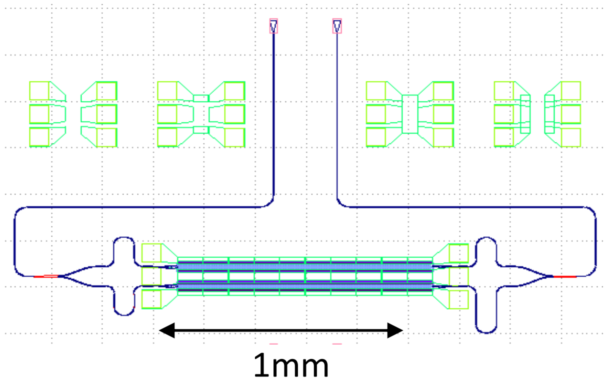


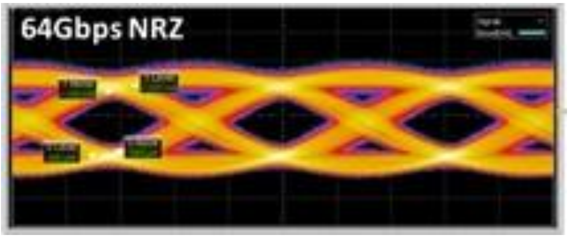


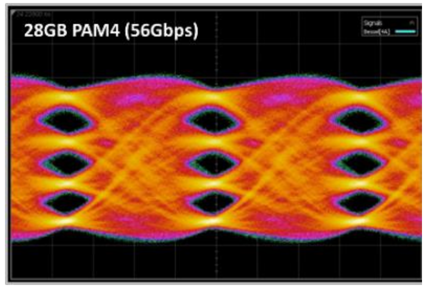
Impact on Mach Zehnder Modulators (MZM)

- Mach Zehnder Modulator based on P-N junction for high data rate transmitter





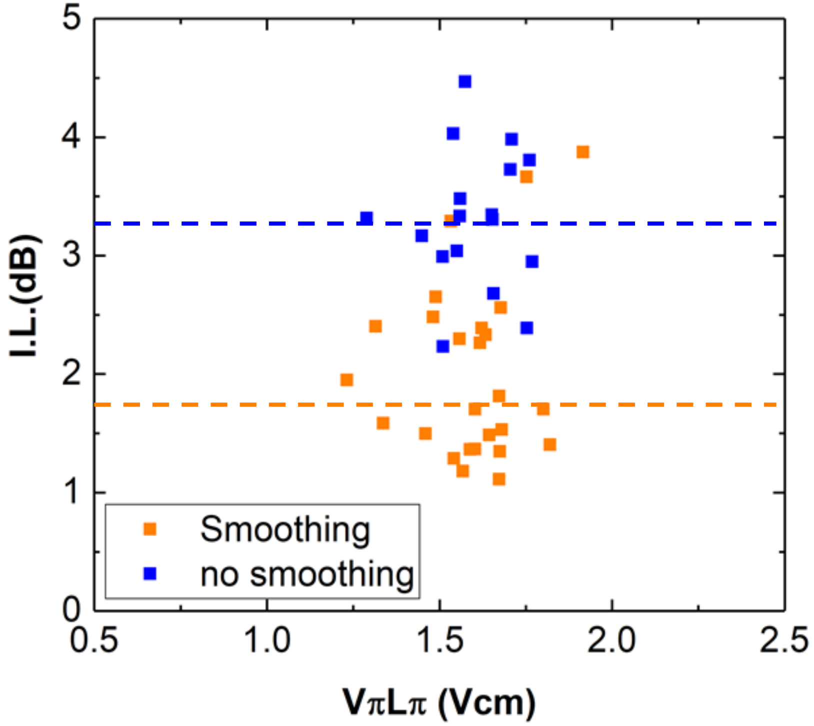




Smoothing annealing on modulators:

- No effect of the smoothing annealing (>800°C) on the P-N junction
- Efficiency preserved ($V_\pi L_\pi$ = 1.6 V.cm with or without annealing)

- **Total loss of MZM reduced by several dBs**
(1.5dB gain with 1mm-long MZM)

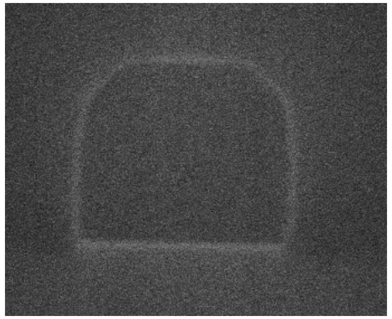


Conclusion

- H_2 smoothing annealing for sidewall roughness reduction
- State-of-the-art propagation losses @ 1310 and 1550 nm

< **1dB/cm** for strip WG ; **0.1dB/cm** for rib waveguide

- Performances of passive and active components of the photonics library are preserved

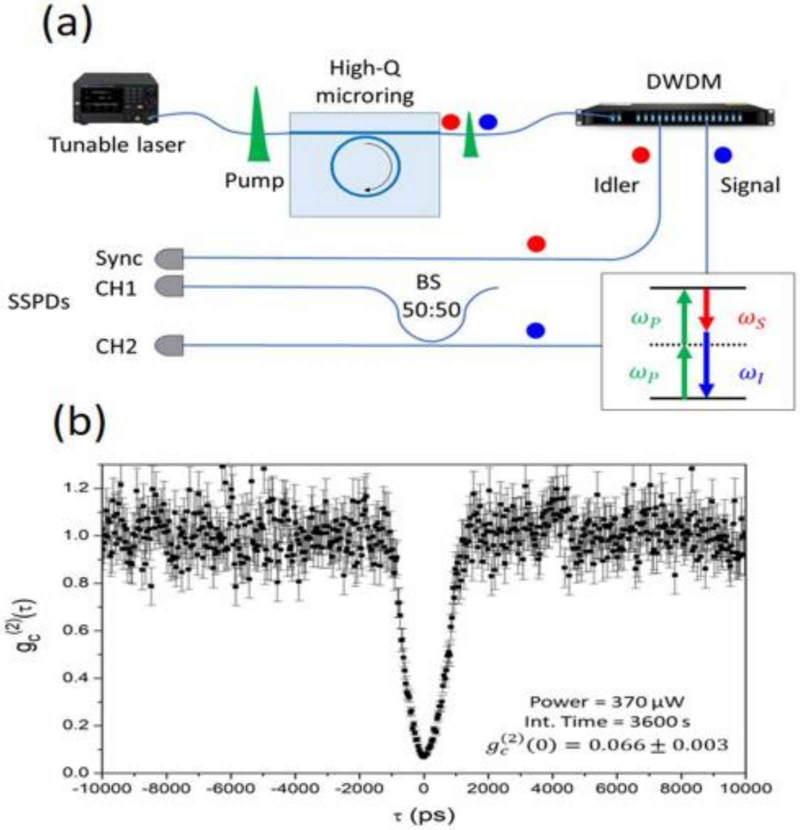


→ dBs power gain in complex circuits (Datacom, LIDAR, neuromorphics…)

Highlight

Low loss is essential for integrated Quantum photonics:

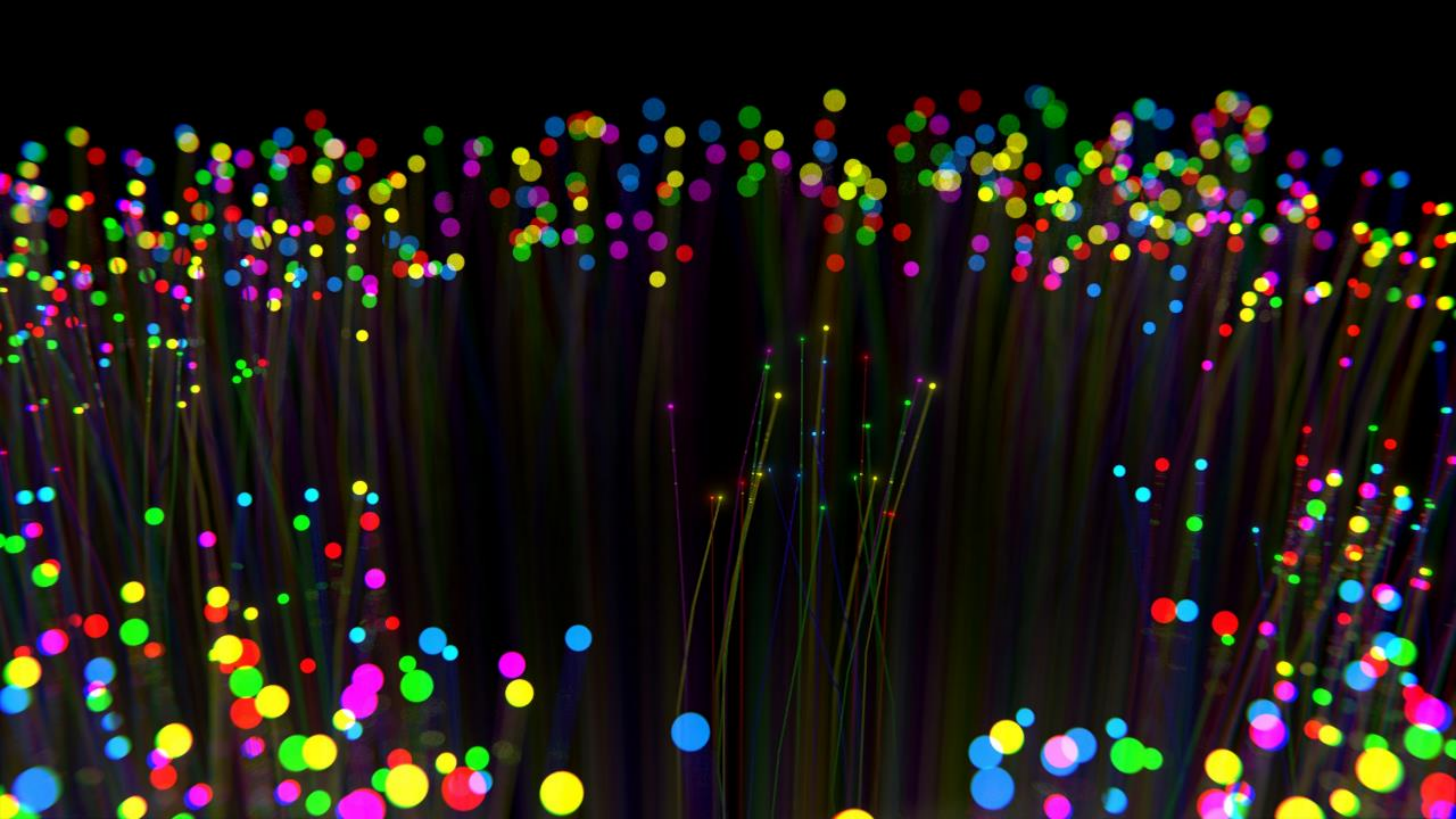
- Entangled photon pair generation in high-Q micro-resonators
- Manipulation of single photons in a large circuit



First results:

F.A. Sabattoli et al. ICTON 2019, “A *Source of Heralded Single Photon Using High Quality Factor Silicon Ring Resonators*”

H. El Dirani et al. GFP 2019, “*Low-Loss Silicon Technology for High-Q Bright Quantum Sources*”



Thank you for attention

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